uClamp0501C



PROTECTION PRODUCTS

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = $8/20\mu s$)	P _{pk}	150	Watts
Maximum Peak Pulse Current (tp = 8/20µs)	l _{pp}	13	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V _{pp}	+/- 20 +/- 15	kV
Operating Temperature	T,	-55 to +125	°C
Storage Temperature	T _{stg}	-55 to +150	°C

Electrical Characteristics (T=25°C)

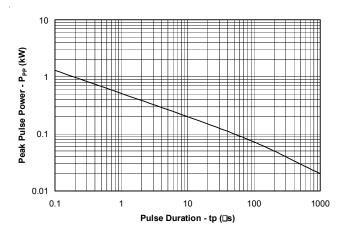
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V _{RWM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA	6			V
Reverse Leakage Current	I _R	V _{RWM} = 5V, T=25°C			1	μA
Clamping Voltage	V _c	I _{PP} = 5A, tp = 8/20µs I/O to Ground			9.8	V
Clamping Voltage	V _c	I _{pp} = 13A, tp = 8/20µs I/O to Ground			11.5	V
Junction Capacitance	C	V _R = 0V, f = 1MHz			50	рF



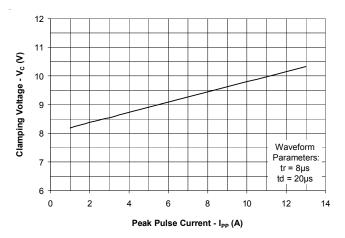
PROTECTION PRODUCTS

Typical Characteristics

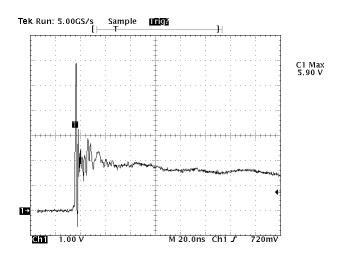
Non-Repetitive Peak Pulse Power vs. Pulse Time



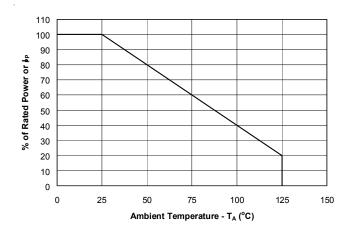
Clamping Voltage vs. Peak Pulse Current



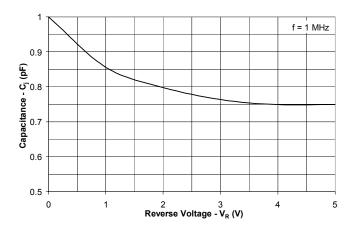
ESD Clamping (8kV Contact Discharge)



Power Derating Curve



Normalized Capacitance vs. Reverse Voltage





PROTECTION PRODUCTS

Applications Information

Device Connection Options

The uClamp0501C has solder bumps located in a 2 x 2 matrix layout on the active side of the device. The bumps are designated as A1, A2, B1, and B2. The line to be protected is connected at bump A2. Bump B1 is connected to ground. Since the device is bidirectional, these connections can be reversed (B1 to protected line, A2 to ground). All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.

Flip Chip TVS

Flip Chip TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting the flip chip TVS. Solder mask defined (SMD) pads produce stress points near the solder mask on the PCB side that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.225 ± 0.010 mm with a solder mask opening of 0.350 ± 0.025 mm. The stencil should be laser cut and electro-polished with a nominal thickness of 0.100 mm.

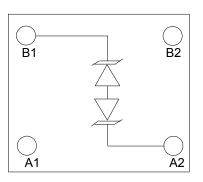
Printed Circuit Board Finish

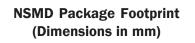
A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

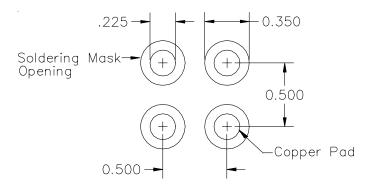
Reflow Profile

The flip chip TVS can be assembled using the reflow requirements for IPC/JEDEC standard J-STD-020B for Sn-Pb eutectic assembly of small body components. During reflow, the component will self-align itself on the pad.

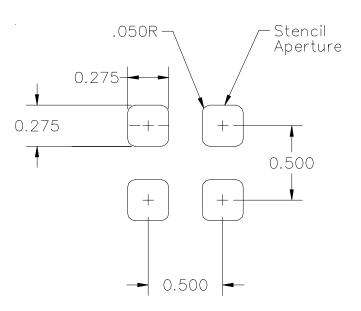
Device Schematic & Pin Configuration





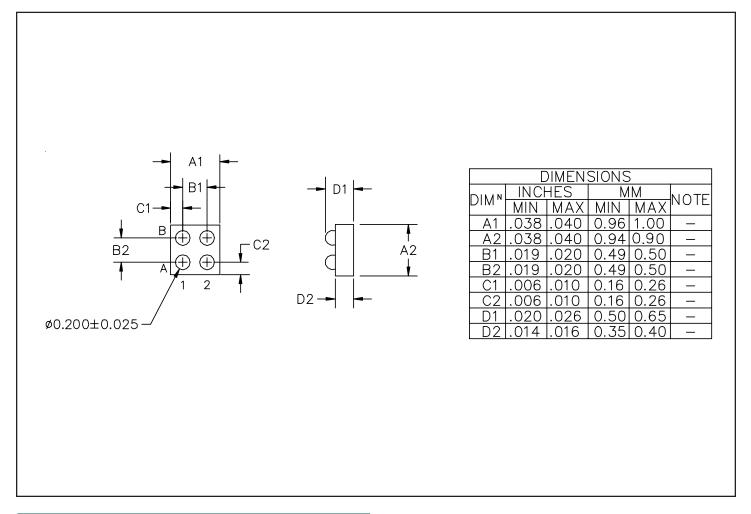




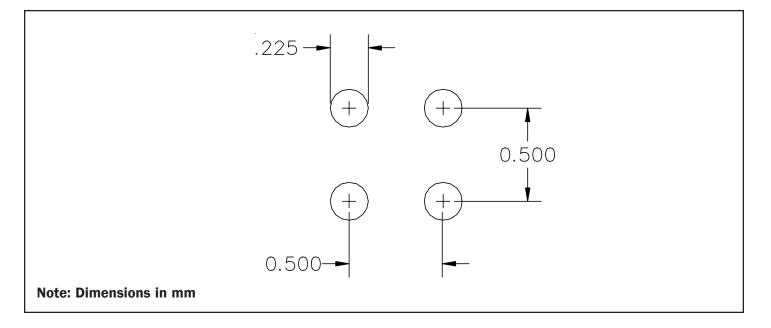




Outline Drawing



Land Pattern





Marking

Α В 2 1

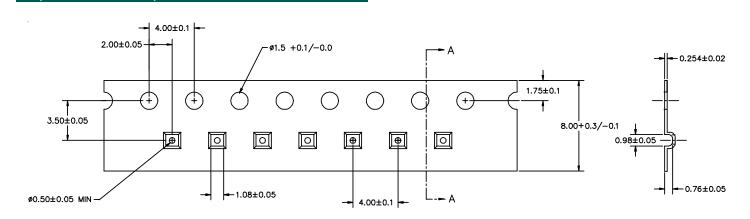
Part Number	Working Voltage	Qty per Reel	Reel Size	
uClamp0501C.WC	5V	3,000	7 Inch	

Ordering Information

2 x 2 Grid Flip Chip TVS (Top View)

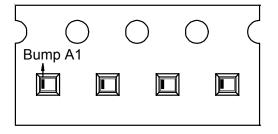
Top Coating: The top (non-bump side) of the device is coated with a white, non-conductive coating. The coating is laser markable and helps prevent die chipping during the PCB assembly process. This material is compliant with UL 94V-0 flammability requirements.

Tape and Reel Specification



1 ALL DIMENSIONS MILLIMETERS.





Device Orientation in Tape

VIEW A-A



Contact Information

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