Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+18	V
I_{OUT}	Output current	± 100	mA
R_{thja}	Thermal resistance junction to ambient DIP8 (1) SO8 (2) TSSOP8 (2)	 85 125 120	°C/W
R_{thjc}	Thermal resistance junction to case DIP8 (1) SO8 (2) TSSOP8 (2)	 41 40 37	°C/W
T_j	Junction temperature	+150	°C
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	Human body model (HBM)(3)	1500	V
	Machine model (MM)(4)	200	
	Charged device model (CDM)(5)	1000	

1. Short-circuits can cause excessive heating. These values are typical and specified for a single layer PCB.
2. Short-circuits can cause excessive heating. These values are typical and specified for a four layers PCB.
3. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
4. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins remain floating.
5. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2 to 16	V
I_{OUT}	Output sink current Output source current	10 50	mA
T_{oper}	Operating free air temperature range TS555C TS555I TS555M	 0 to +70 -40 to +125 -55 to +125	°C

2 Schematic diagrams

Figure 1. Schematic diagram

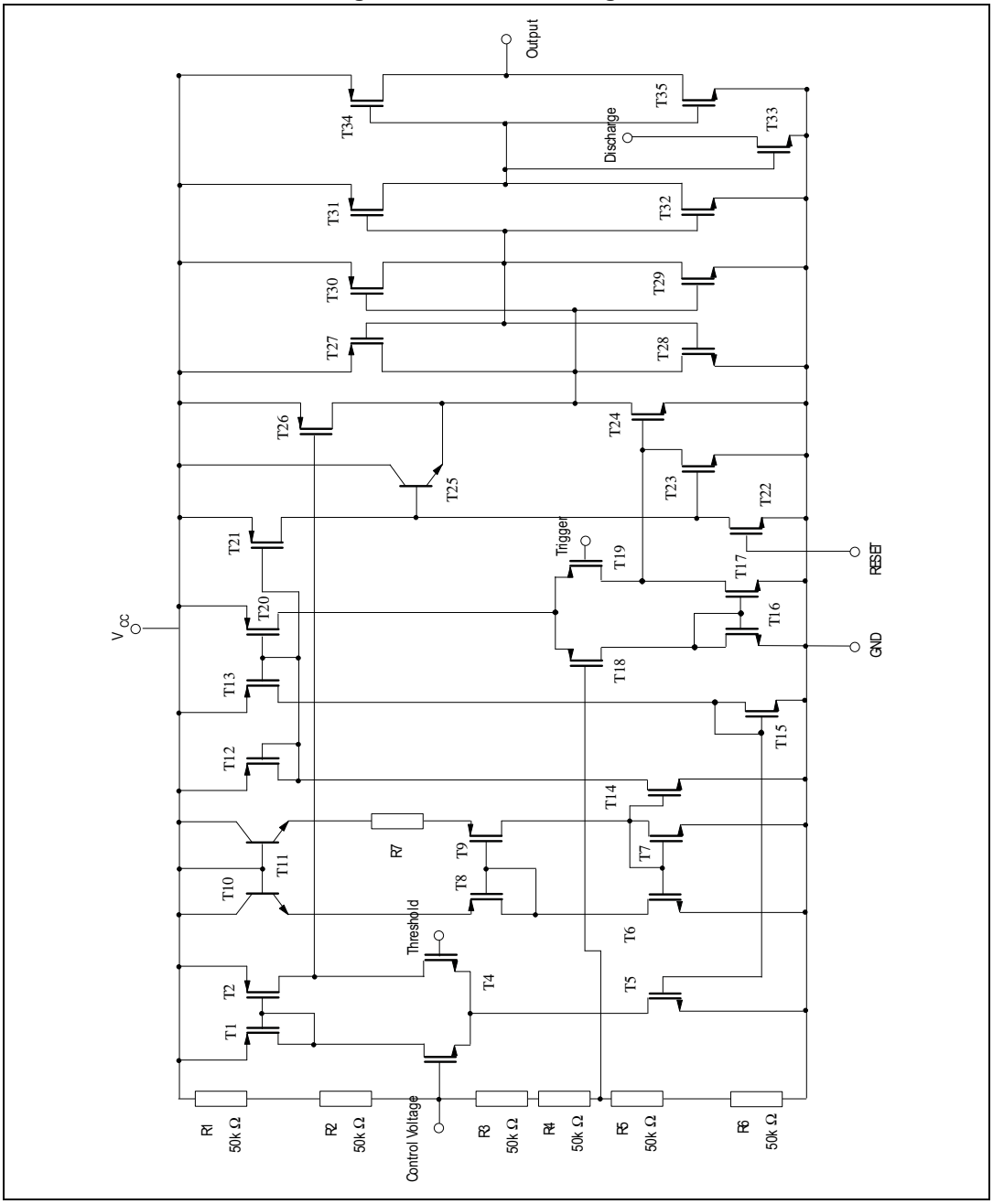


Figure 2. Block diagram

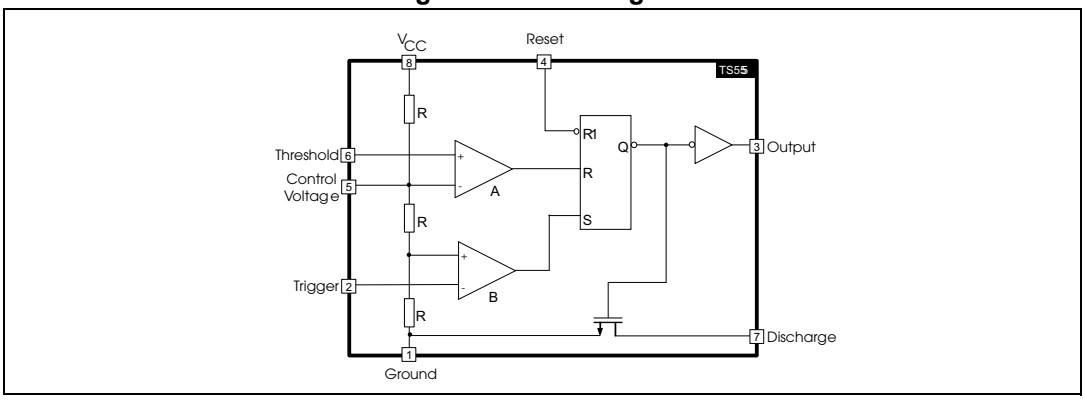


Table 3. Functional table

Reset	Trigger	Threshold	Output
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous state

Note: Low: level voltage ≤ minimum voltage specified
High: level voltage ≥ maximum voltage specified
x: irrelevant

3 Electrical characteristics

Table 4. Static electrical characteristics
V_{CC} = +2 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min.} \leq T_{amb} \leq T_{max}$		65	200 200	µA
V_{CL}	Control voltage level $T_{min.} \leq T_{amb} \leq T_{max}$	1.2 1.1	1.3	1.4 1.5	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 1 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		0.05	0.2 0.25	V
I_{DIS}	Discharge pin leakage current		1	100	nA
V_{OL}	Low level output voltage (I_{sink} = 1 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		0.1	0.3 0.35	V
V_{OH}	High level output voltage (I_{source} = -0.3 mA) $T_{min.} \leq T_{amb} \leq T_{max}$	1.5 1.5	1.9		V
V_{TRIG}	Trigger voltage $T_{min.} \leq T_{amb} \leq T_{max}$	0.4 0.3	0.67	0.95 1.05	V
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		pA
V_{RESET}	Reset voltage $T_{min.} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset current		10		pA

Table 5. Static electrical characteristics
V_{CC} = +3 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min.} \leq T_{amb} \leq T_{max}$		90	230 230	µA
V_{CL}	Control voltage level $T_{min.} \leq T_{amb} \leq T_{max}$	1.8 1.7	2	2.2 2.3	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 1 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		0.05	0.2 0.25	V
I_{DIS}	Discharge pin leakage current		1	100	nA
V_{OL}	Low level output voltage (I_{sink} = 1 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		0.1	0.3 0.35	V
V_{OH}	High level output voltage (I_{source} = -0.3 mA) $T_{min.} \leq T_{amb} \leq T_{max}$	2.5 2.5	2.9		V
V_{TRIG}	Trigger voltage $T_{min.} \leq T_{amb} \leq T_{max}$	0.9 0.8	1	1.1 1.2	V
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		pA
V_{RESET}	Reset voltage $T_{min.} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset current		10		pA

Table 6. Dynamic electrical characteristics
V_{CC} = +3 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Timing accuracy (monostable)(1) R = 10 kΩ, C = 0.1 µF V_{CC} = 2 V V_{CC} = 3 V		 1 1		%
	Timing shift with supply voltage variations (monostable) R = 10 kΩ, C = 0.1 µF, V_{CC} = 3 V ± 0.3 V (1)		0.5		%/V
	Timing shift with temperature (1) $T_{min.} \leq T_{amb} \leq T_{max}$.5		75		ppm/°C
f_{max}	Maximum astable frequency (2) R_A = 470 Ω, R_B = 200 Ω, C = 200 pF		2		MHz
	Astable frequency accuracy (2) R_A = R_B = 1 kΩ to 100 kΩ, C = 0.1 µF		5		%
	Timing shift with supply voltage variations (astable mode) (2) R_A = R_B = 1 kΩ to 100 kΩ, C = 0.1 µF, V_{CC} = 3 to 5 V		0.5		%/V
t_R	Output rise time (C_{load} = 10 pF)		25		ns
t_F	Output fall time (C_{load} = 10 pF)		20	-	ns
t_{PD}	Trigger propagation delay		100		ns
t_{RPW}	Minimum reset pulse width (V_{trig} = 3 V)		350		ns

1. See *Figure 4*
2. See *Figure 6*

Table 7. Static electrical characteristics
V_{CC} = +5 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min.} \leq T_{amb} \leq T_{max}$		110	250 250	µA
V_{CL}	Control voltage level $T_{min.} \leq T_{amb} \leq T_{max}$	2.9 2.8	3.3	3.8 3.9	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 10 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		0.2	0.3 0.35	V
I_{DIS}	Discharge pin leakage current		1	100	nA
V_{OL}	Low level output voltage (I_{sink} = 8 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		0.3	0.6 0.8	V
V_{OH}	High level output voltage (I_{source} = -2 mA) $T_{min.} \leq T_{amb} \leq T_{max}$	4.4 4.4	4.6		V
V_{TRIG}	Trigger voltage $T_{min.} \leq T_{amb} \leq T_{max}$	1.36 1.26	1.67	1.96 2.06	V
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		pA
V_{RESET}	Reset voltage $T_{min.} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset current		10		pA

Table 8. Dynamic electrical characteristics
V_{CC} = +5 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Timing accuracy (monostable) (1) R = 10 kΩ, C = 0.1 µF		2		%
	Timing shift with supply voltage variations (monostable) (1) R = 10 kΩ, C = 0.1 µF,V_{CC} = 5 V ± 1 V		0.38		%/V
	Timing shift with temperature (1) $T_{min.} \leq T_{amb} \leq T_{max}$5		75		ppm/°C
f_{max}	Maximum astable frequency (2) R_A = 470 Ω, R_B = 200 Ω, C = 200 pF		2.7		MHz
	Astable frequency accuracy (2) R_A = R_B = 1 kΩ to 100 kΩ, C = 0.1 µF		3		%
	Timing shift with supply voltage variations (astable mode) (2) R_A = R_B = 10 kΩ, C = 0.1 µF, V_{CC} = 5 to 12 V		0.1		%/V
t_R	Output rise time (C_{load} = 10 pF)		25		ns
t_F	Output fall time (C_{load} = 10 pF)		20	-	ns
t_{PD}	Trigger propagation delay		100		ns
t_{RPW}	Minimum reset pulse width (V_{trig} = 5 V)		350		ns

1. See *Figure 4*
2. See *Figure 6*

Table 9. Static electrical characteristics
V_{CC} = +12 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

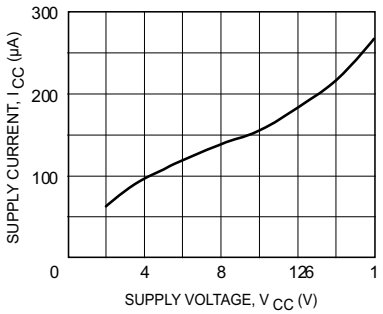
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min.} \leq T_{amb} \leq T_{max}$		170	400 400	µA
V_{CL}	Control voltage level $T_{min.} \leq T_{amb} \leq T_{max}$	7.4 7.3	8	8.6 8.7	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 80 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		0.09	1.5 2.0	V
I_{DIS}	Discharge pin leakage current		1	100	nA
V_{OL}	Low level output voltage (I_{sink} = 50 mA) $T_{min.} \leq T_{amb} \leq T_{max}$		1.2	2 2.8	V
V_{OH}	High level output voltage (I_{source} = -10 mA) $T_{min.} \leq T_{amb} \leq T_{max}$	10.5 10.5	11		V
V_{TRIG}	Trigger voltage $T_{min.} \leq T_{amb} \leq T_{max}$	3.2 3.1	4	4.8 4.9	V
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		pA
V_{RESET}	Reset Voltage $T_{min.} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset current		10		pA

Table 10. Dynamic electrical characteristics
V_{CC} = +12 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Timing accuracy (monostable) (1) R = 10 kΩ, C = 0.1 µF, V_{CC} = +12 V		4		%
	Timing shift with supply voltage variations (monostable) (1) R = 10 kΩ, C = 0.1 µF, V_{CC} = +5 V ±1 V		0.38		%/V
	Timing shift with temperature $T_{min.} \leq T_{amb} \leq T_{max.}$, V_{CC} = +5 V		75		ppm/°C
f_{max}	Maximum astable frequency (2) R_A = 470 Ω, R_B = 200 Ω, C = 200 pF, V_{CC} = +5 V		2.7		MHz
	Astable frequency accuracy $R_A = R_B$ = 1 kΩ to 100 kΩ, C = 0.1 µF, V_{CC} = +12 V		3		%
	Timing shift with supply voltage variations (astable mode) $R_A = R_B$ = 1 kΩ to 100 kΩ, C = 0.1 µF, V_{CC} = 5 to +12 V		0.1		%/V

1. See *Figure 4*
2. See *Figure 6*

Figure 3. Supply current (per timer) versus supply voltage

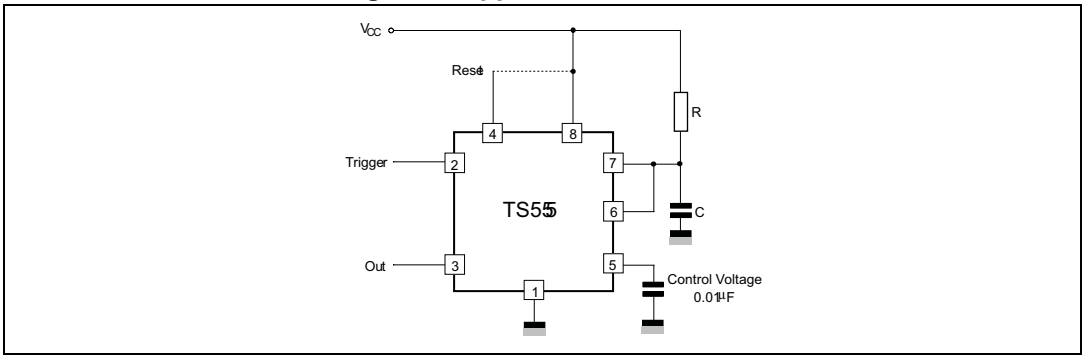


4 Application information

4.1 Monostable operation

In monostable mode, the timer operates like a one-shot generator. The external capacitor is initially held discharged by a transistor inside the timer, as shown in *Figure 4*.

Figure 4. Application schematic



The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R\ x\ C$.

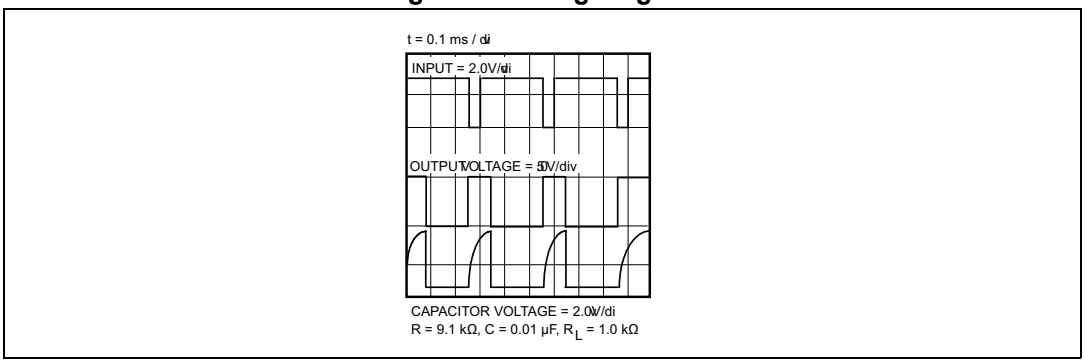
Since the charge rate and threshold level of the comparator are both directly proportional to the supply voltage, the timing interval is independent of the supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle then starts on the positive edge of the reset pulse. While the reset pulse is applied, the output is driven to the LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R\ x\ C$.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. *Figure 5* shows the actual waveforms generated in this mode of operation.

When reset is not used, it should be tied high to avoid any false triggering.

Figure 5. Timing diagram



4.2 Astable operation

When the circuit is connected as shown in *Figure 6* (pins 2 and 6 connected) it triggers itself and runs as a multi-vibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Therefore, the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore frequency, are independent of the supply voltage.

Figure 6. Application schematic

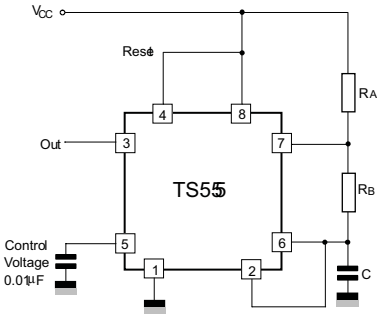


Figure 7 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t1 = 0.693\ (R_A + R_B)\ C$$

The discharge time (output LOW) by:

$$t2 = 0.693\ x\ R_B\ x\ C$$

Thus the total period T is given by:

$$T = t1 + t2 = 0.693\ (R_A + 2R_B)\ C$$

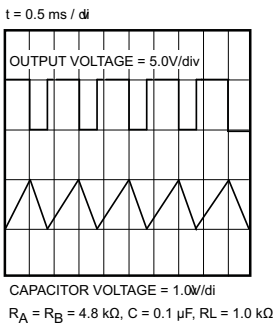
The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(RA + 2RB)C}$$

The duty cycle is given by:

$$D = \frac{RB}{RA + 2RB}$$

Figure 7. Timing diagram



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 DIP8 package information

Table 11. DIP8 package mechanical drawing

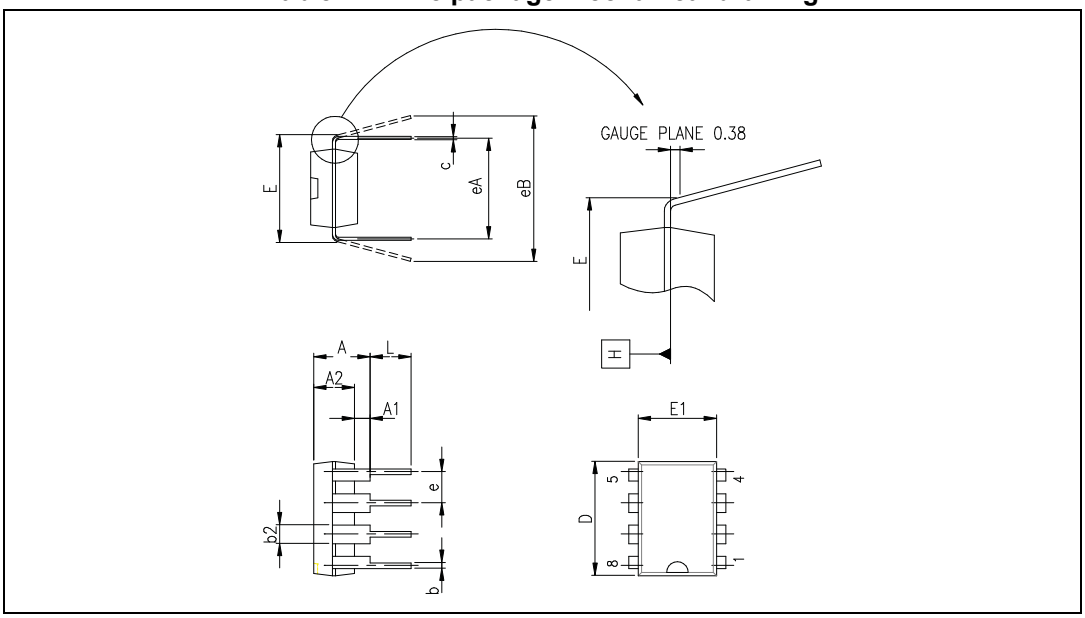


Table 12. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

5.2 SO8 package information

Figure 8. SO8 package mechanical drawing

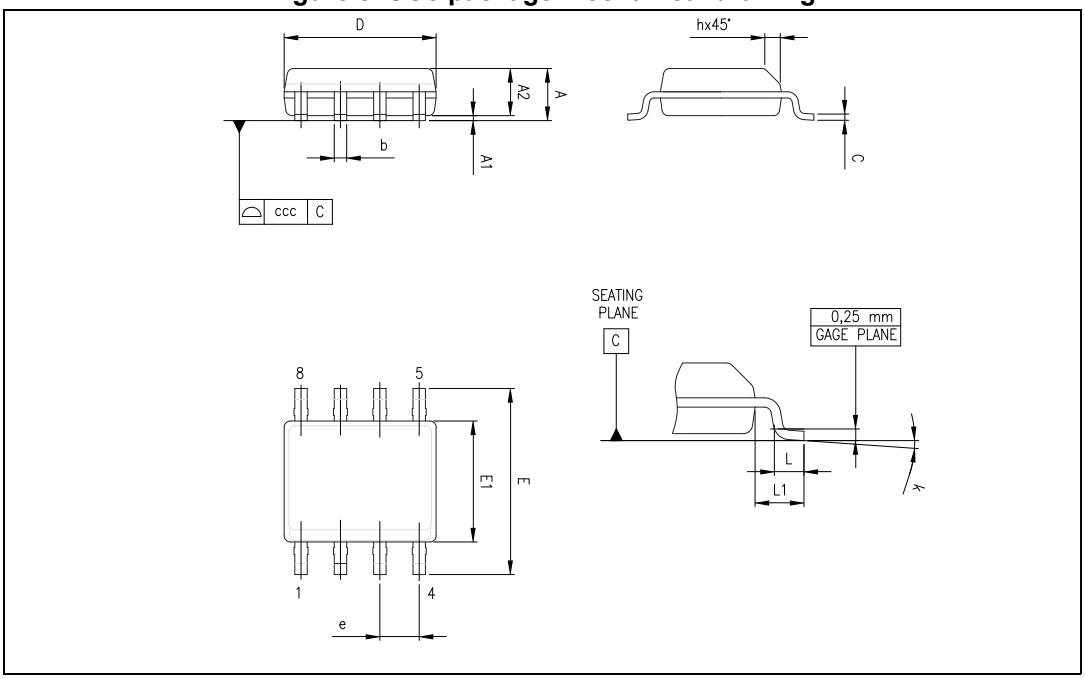


Table 13. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

5.3 TSSOP8 package information

Figure 9. TSSOP8 package mechanical drawing

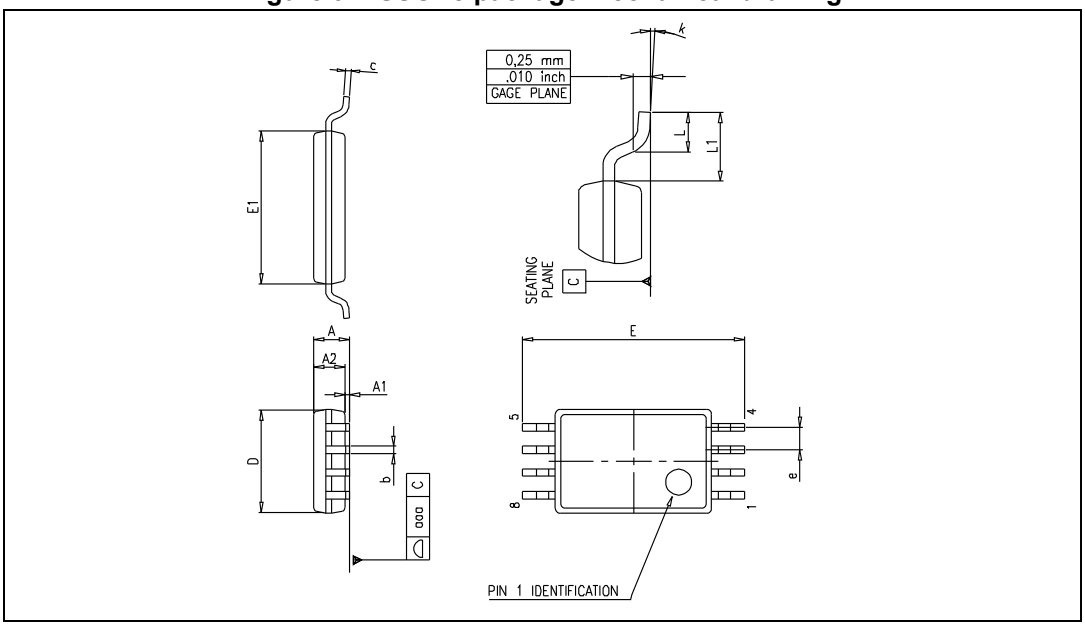


Table 14. TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	

6 Ordering information

Table 15. Ordering information scheme

Example: TS555 C D T TR

Device type

TS555

Temperature range

C = 0 to 70 °C

I = -40 to 125 °C

M = -55 to 125 °C

Package

N = DIP8 (1)

D = SO8 (2)

P = TSSOP8 (2)

Shipping method

T = tape and reel

Blank = tube

Specific requirements

TR = custom

Blank = public

1. Marking = TS555CN, TS555IN
2. Marking = 555C, 555I, 555M

7 Revision history

Table 16. Document revision history

Date	Revision	Changes
01-Feb-2003	1	Initial release.
03-Nov-2008	2	Document reformatted. Added output current, ESD and thermal resistance values in *Table 1: Absolute maximum ratings*. Added output current values in *Table 2: Operating conditions*.
29-Aug-2014	3	*Section 5: Package information*: updated corporate text Replaced *Table 15: Ordering information scheme*