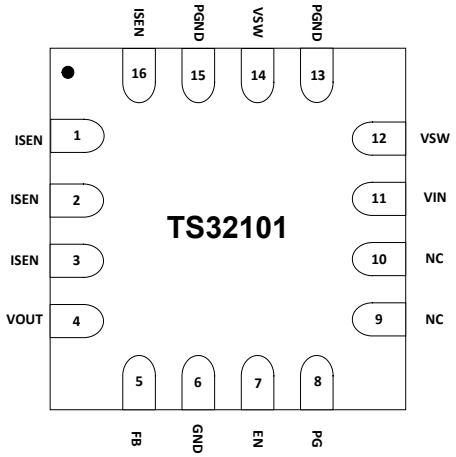
Pinout



Pin Description

Pin #	Pin Name	Pin Function	Description
1	ISEN	Boot Power Stage Output	Connects to current sense resistor becoming current sense (Pin 1,2,3,16 are internally connected)
2	ISEN	Boot Power Stage Output	Connects to current sense resistor becoming current sense
3	ISEN	Boot Power Stage Output	Connects to current sense resistor becoming current sense
4	VOUT	Output Voltage	Connect to the other terminal of current sense resistor, which is the output of the boost regulator
5	FB	Output Voltage Feedback	Feedback point for output voltage
6	GND	GND	Primary ground for the majority of the device except the low-side power FET
7	EN	Enable Input	Tie EN pin high to enable device
8	PG	PG Output	Open-drain output for Power Good
9	N/C	Not Used	Connect to GND
10	N/C	Not Used	Connect to GND
11	VIN	Input Voltage	Connect to input supply and input capacitor.
12	VSW	Switching Voltage Node	Connected to 1.0uH (typical) inductor
13	PGND	Power GND	GND supply for internal low-side FET
14	VSW	Switching Voltage Node	Connected to 1.0uH (typical) inductor
15	PGND	Power GND	GND supply for internal low-side FET
16	ISEN	Boot Power Stage Output	Connects to current sense resistor becoming current sense

Functional Block Diagram

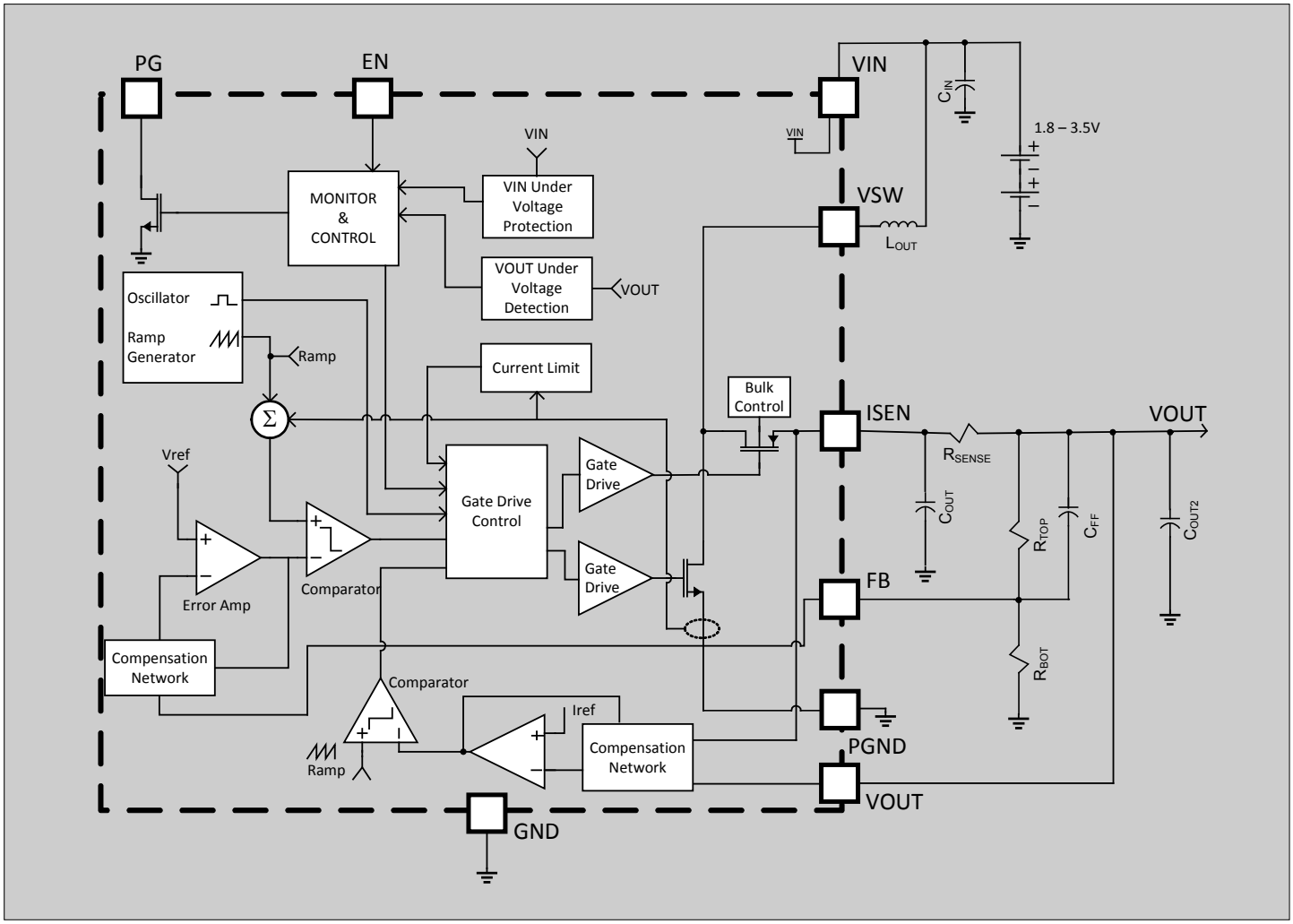


Figure 1: TS32101 Block Diagram

Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted(1, 2)

Parameter	Value	Unit
VIN	-0.3 to 6.0	V
EN, PG, FB	-0.3 to 5.5	V
VSW	-1 to 6.0	V
VOUT, ISEN	-0.3 to 6.0	V
Continuous total power dissipation	See Dissipation Rating Table	
Electrostatic Discharge – Human Body Model	±2k	V
Electrostatic Discharge – Charged Device Model	+/-500	V
Lead Temperature (soldering, 10 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Thermal Resistance Junction to Air (Note 1)	50	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_J	Operating Ambient Temperature Range	-40 to 85	°C
$T_{J\,MAX}$	Maximum Junction Temperature	150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes TQFN-16 in 1 in2 area of 2 oz copper and 25□C ambient temperature.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Input Operating Voltage	1.8	2.4	5.5	V
L_{OUT}	Output Filter Inductor Typical Value (Note 1)		1.0		uH
C_{OUT}	Output Filter Capacitor Typical Value (Note 2)	33	47	100	uF
C_{OUT2}	VOUT2 Filter Capacitor Typical Value (Note 2)	0.1	1		uF
C_{BYPASS}	Input Supply Bypass Capacitor Typical Value (Note 3)	8	10		uF
R_{TOP}	Feedback Divider Resistor Typical Value (Note 4)		1000		kΩ
R_{BOT}	Feedback Divider Resistor Typical Value (Note 4)		330		kΩ

Note 1: For best performance, an inductor with a saturation current rating higher than the maximum input current requirement plus the inductor current ripple. See Inductor Selection section to determine input current and ripple current.

Note 2: For best performance, a low ESR ceramic capacitor should be used.

Note 3: For best performance, a low ESR ceramic capacitor should be used. If CBYPASS is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to CBYPASS.

Note 4: Values shown for 5V output.

Characteristics

Electrical Characteristics, T_A = -40C to 85C, VIN =2.4V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN Supply Voltage						
VIN	Voltage Input		1.75		5.5	V
$I_{IN-STBY}$	Quiescent current Standby Mode	EN = Low, VOUT=0V		5	10	uA
I_{IN-LPM}	Operating Low Power Mode Input Current	Iout = 0 uA		50		uA
VOUT Supply Current						
I_{OUT}	Quiescent current Normal Mode (Note 1)	EN = High, Switching		3		mA
		EN = High, Non-switching		500		uA
$I_{OUT-STBY}$	Quiescent current, stby	EN = Low, Vout=5V		25		uA
I_{OUT}	Output current	EN = High, V_{IN} > 0.7 * Vout		2		A
VIN Under Voltage Lockout (UVLO)						
V_{IN_UV}	VIN Under Voltage Detect Threshold	Increasing Vin		1.5		V
V_{IN-UV_HYST}	VIN Under Voltage Detect Hysteresis			150		mV
OSC						
f_{OSC}	Oscillator Frequency		1.8	2	2.2	MHz
PG Open Drain Output						
V_{PG_THRESH}	Power Good Voltage Detect Threshold	Vout Increasing		90		% V_{OUT}
V_{PG_HYST}	Power Good Voltage Detect Hysteresis			1		% V_{OUT}
I_{OH-PG}	High-Level Output Leakage	V_{PG} = 5.0 V		0.1		uA
V_{OL-PG}	Low-Level Output Voltage	I_{PG} = -1mA			0.4	V
EN Input						
V_{IH}	High Level Input Voltage		1.5			V
V_{IL}	Low Level Input Voltage				0.6	V
V_{HYST}	Input Hysteresis			150		mV
I_{IN-EN}	Input Leakage	V_{EN}=VIN		0.1		uA
		V_{EN}=0V		0.1		uA
Thermal Shutdown						
TSD	Thermal Shutdown Junction Temperature		150	170		C
TSD_{HYST}	TSD Hysteresis			10		C

Note 1: large percentage of supply current due to power FET gate switching losses.

Boost Converter Characteristics

Electrical Characteristics, T_A = -40C to 85C, VIN = 2.4V, VOUT = 5.0V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Boost Regulator: L=1.0uH and C=44uF						
V_{OUT}	Output Voltage		3.0		5.5	V
V_{FB}	Feedback Voltage		1.175	1.2	1.225	V
R_{DSON}	High Side Switch On Resistance	I_{SW} = -1A, T_J=25C		120		mΩ
	Low Side Switch On Resistance	I_{SW} = -1A, T_J=25C		50		mΩ
I_{OCD}	Over Current Detect	LS switch current	3			A
V_{ISEN}	Output Current Threshold Voltage			23		mV
V_{OUT-OV}	VOUT Over Voltage Threshold		101	102	103	%V_{OUT}
$DUTY_{MAX}$	Max Duty Cycle			85		%

Functional Description

The TS32101 is a fully-integrated, low-voltage synchronous boost converter IC based on a highly-efficient switching topology. It is optimized to be powered from NiMH or Li-Ion batteries and includes features to make it suitable for powering portable equipment as an emergency power/ charging source. A 2MHz internal switching frequency yields a good balance between efficiency and the ability to use small, low-cost LC filter components.

Internal Protection Details

Internal Current Limit

The current through the low side switch is sensed on a cycle by cycle basis and if current limit is reached, it will abbreviate the cycle. Current limit is always active when the boost converter is enabled.

Adjustable Output Current Limit

The TS32101 has an adjustable output current limit that is implemented by sensing the voltage across an external resistor placed in series with the output. The voltage across this resistor is continuously monitored with no output current limit occurring until the output current is large enough to produce a voltage drop of 23mV across the sense resistor. If the voltage drop across the sense resistor reaches 23mV the TS32101 will reduce the duty cycle to limit the output current and result in a constant output current limit. This feature can be disabled by connecting the ISEN to VOUT and removal of the sense resistor.

Adjustable Output Voltage

The TS32101 has an adjustable output voltage selected by an external resistor divider in the feedback loop. To change the output voltage, replace resistors RTOP and RBOT with values from the following equation:

$$VOUT = 1.2 * (1 + R_{TOP} / R_{BOT})$$

Power Good

The PG signal provides the ability to monitor fault conditions and power supply sequencing. The PG output is valid high when the TS32101 is enabled, the input voltage is above the VIN under-voltage threshold, the output voltage is above 90% of the desired value, and the device is not in thermal shutdown.

The PG output can be utilized for power supply sequencing. When the device is operating normally and the output voltage is above 90% of the desired value, the PG output will be high. A 100us deglitch timer is used to insure that the PG signal does not respond to noise or transients.

Thermal Shutdown

If the temperature of the die exceeds 150C (typical), the VSW outputs will tri-state to protect the device from damage. The PG and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 140C (typical), the device will attempt to start up again. If the device reaches 150C, the shutdown/restart sequence will repeat. The PG output will be pulled low in this condition.

Output Over Voltage Protection

The TS32101 has an output over voltage protection circuit which prevents the device from reaching a dangerously high voltage under sudden light load conditions. The typical Overvoltage detection threshold is 102% of Vout.

Output Voltage Disable

When the enable pin of the TS32101 is low, not only is switching disabled, but the output is isolated from the input. This functionality is maintained whether the output node is at a higher or a lower potential than the input voltage.

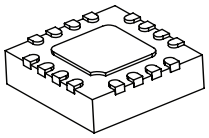
Low Power Mode

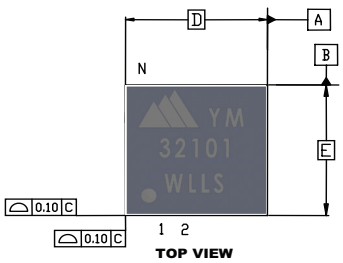
When the output current is low the TS32101 will detect and automatically enter low power mode. In low power mode, switching stops when the output is slightly above the regulation point and the device enters a sleep state. The sleep state continues until the output drops slightly below the regulation point. At this point, switching will resume and if the load current is increased enough to prevent the output from going above the regulation point, low power mode is exited.

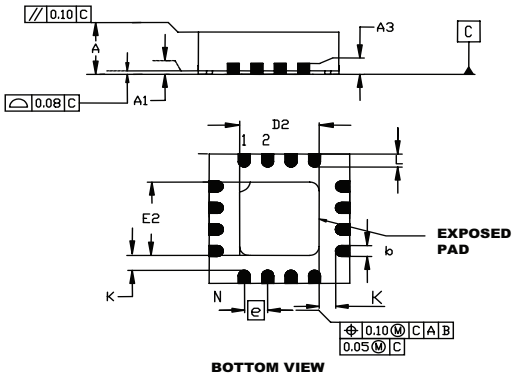
External Components

The internal compensation is optimized for a 47uF output capacitor and a 1.0uH inductor. To keep the output ripple low, a low ESR (less than 35mOhm) ceramic capacitor is recommended.

Package Mechanical Drawings (all dimensions in mm)

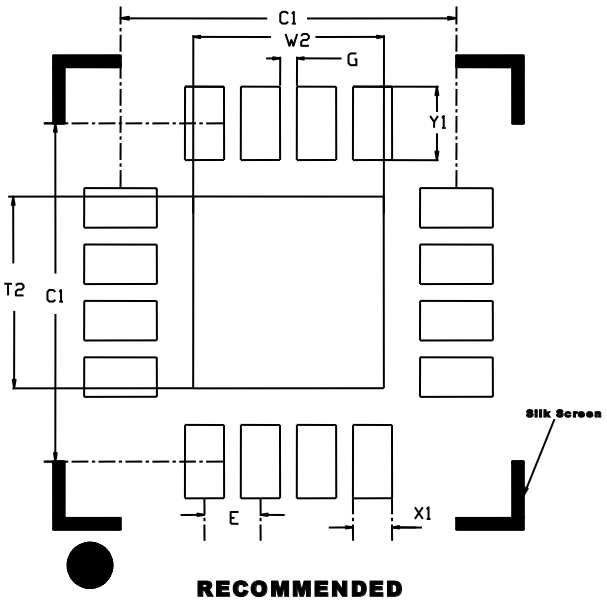






	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.55	1.70	1.80
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-

Recommended PCB Land Pattern



DIMENSIONS IN MILLIMETERS

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	1.70
Contact Pad Spacing	C1	-	3.00	-
Contact Pad Spacing	C2	-	3.00	-
Contact Pad Width (X16)	X1	-	-	0.35
Contact Pad Length (X16)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

Notes:
Dimensions and tolerances per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact values shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information only.

Packaging Information

Pb-Free (RoHS): The TS32101 devices are fully compliant for all materials covered by European Union Directive 2002/95/EC, and meet all IPC-1752 Level 3 materials declaration requirements.

MSL, Peak Temp: The TS32101 family has a Moisture Sensitivity Level (MSL) 1 rating per JEDEC J-STD-020D. These devices also have a Peak Profile Solder Temperature (Tp) of 260°C.

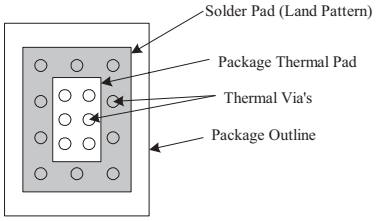
Ordering Information

TS32101-QFNR

Application Using A Multi-Layer PCB

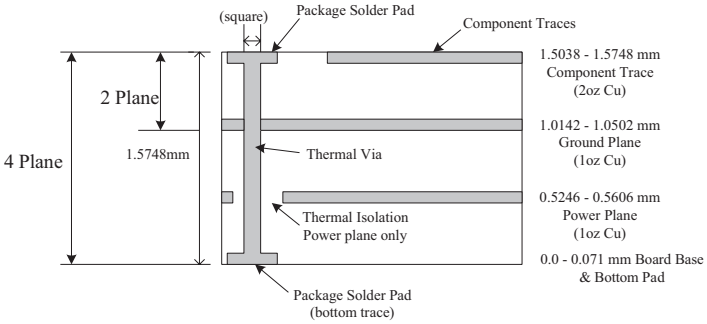
To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

The following are guidelines for mounting the exposed pad IC on a Multi-Layer PCB with ground a plane.

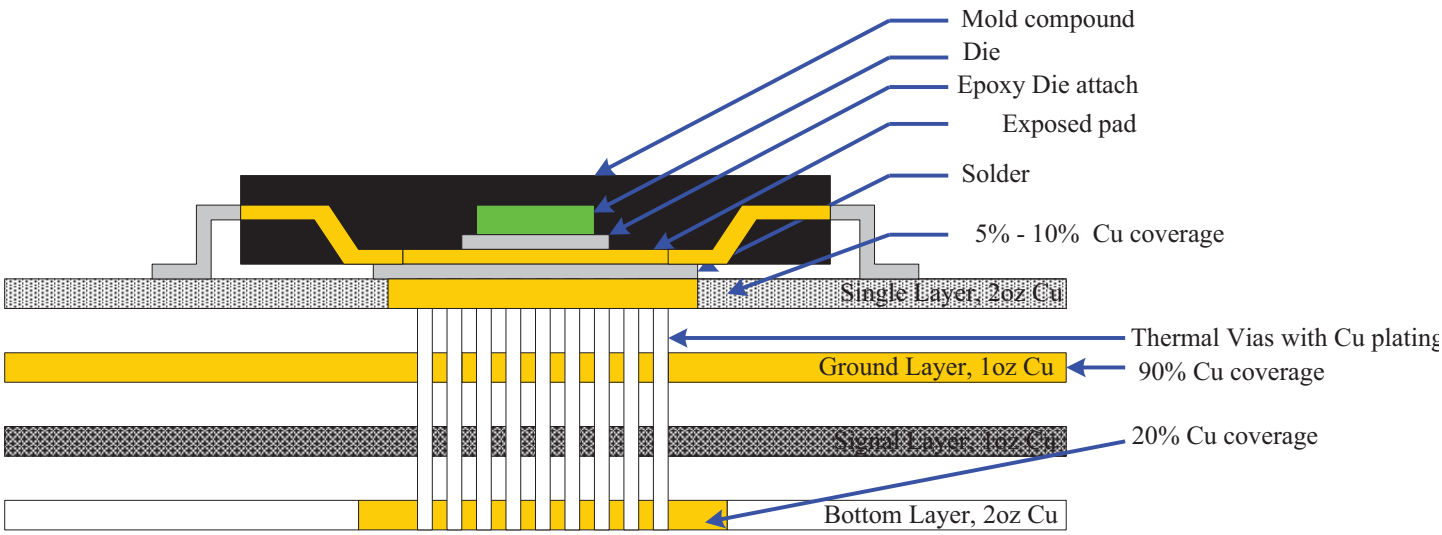


Package and PCB Land Configuration
For a Multi-Layer PCB

JEDEC standard FR4 PCB Cross-section:



Multi-Layer Board (Cross-sectional View)

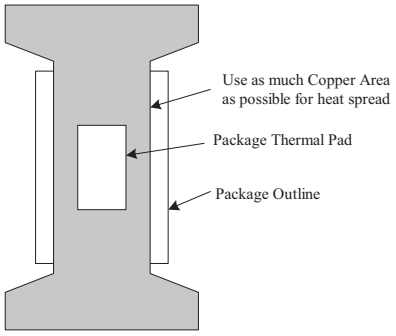


Note: NOT to Scale

In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, thickness of copper, etc.

The above drawing is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators may have to be de-rated for ambient temperatures above 85C. The de-rate value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

Application Using A Single Layer PCB



Layout recommendations for a Single Layer PCB: utilize as much Copper Area for Power Management. In a single layer board application the thermal pad is attached to a heat spreader (copper areas) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above it is advisable to use as much copper traces as possible to dissipate the heat.

IMPORTANT:

If the attachment method is NOT implemented correctly, the functionality of the product is not guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

Contact Information

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