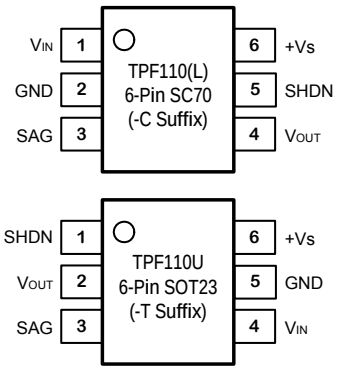
Order Information

Order Number	Marking Information	Operating Temperature Range	Package	Transport Media, Quantity
TPF110-CR	F0YW (1)	-40 to 85°C	6 Lead SC70	7" Tape and Reel, 3,000pcs
TPF110U-TR	F0UYW (1)	-40 to 85°C	6 Lead SOT23	7" Tape and Reel, 3,000pcs
TPF110L-CR	F0LYW (1)	-40 to 85°C	6 Lead SC70	7" Tape and Reel, 3,000pcs

Note: (1). 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

Pin configuration (Top View)



Pin	Pin Name	Function
1	V_{IN}	Input Voltage.
2	GND	Ground.
3	SAG	Feedback Connection.
4	V_{OUT}	Output Voltage.
5	SHDN	Shut-down.
6	$+V_S$	Positive Power Supply.

Absolute Maximum Ratings[Note]

Parameters		Value	Unit
Power Supply, V_{DD} to GND		6.0	V
PD	Power Dissipation, TA = 25°C, 6-Lead SC70	300	mW
V_{IN}	Input Voltage	V_{DD} + 0.3V to GND - 0.3V	
I_{OUT}	Output Current	65	mA
T_J	Maximum Junction Temperature	150	°C
T_A	Operating Temperature Range	–45 to 85	°C
T_{STG}	Storage Temperature Range	–65 to 150	°C
TL	Lead Temperature (Soldering, 10 sec)	300	°C
θ_{JA}	6-Lead SC70	430	°C/W

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Electrical Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Electrical Specifications						
V_{DD}	Supply Voltage Range		2.85		5.5	V
$I_{DD(ON)}$	Quiescent Current (I_Q) (1)	TPF110: V_{DD}=3.3V, V_{IN}=500mV, EN=V_{DD}, no load		3.9	4.9	mA
		TPF110: V_{DD}=5.0V, V_{IN}=500mV, EN=V_{DD}, no load		5.1	6.3	mA
		TPF110L: V_{DD}=3.3V, V_{IN}=500mV, EN=V_{DD}, no load		1.9	2.8	mA
		TPF110L: V_{DD}=5.0V, V_{IN}=500mV, EN=V_{DD}, no load		2.9	3.9	mA
$I_{DD(OFF)}$	Disabled Current	V_{DD}=3.3V, EN=0		0.5	1.5	μA
		V_{DD}=5.0V, EN=0		1.5	3	μA
V_{OLS}	Output Level Shift Voltage	V_{IN} = 0V, no load, input referred	53	80	124	mV
V_{CLAMP}	Input Voltage Clamp	I_{IN} = -100μA	-40	0	+40	mV
$I_{CLAMP-CHG}$	Clamp Charge Current	V_{IN} = V_{CLAMP} - 200mV	-1.5	-1.7		mA
$I_{CLAMP-DCHG}$	Clamp Discharge Current	V_{IN} = 500mV	1.5	2.0	5.1	μA
R_{IN}	Input Impedance	0.5V < V_{IN} < 1.0V	0.5	3		MΩ
AV	Voltage Gain	V_{IN}=0.5V, 1V and 2V R_L = 150Ω to GND	5.9	6.01	6.025	dB
A_{SAG}	SAG Correction DC Gain to V_{OUT}	SAG open		2.25		V/V
PSRR	Power Supply Rejection Ratio	ΔV_{DD} = 3.3V to 3.6V		61		dB
		ΔV_{DD} = 5.0V to 5.5V, 50Hz, V_{IN}=0.7V		67		dB
V_{OH}	Output Voltage High Swing	V_{IN} = 3V, R_L = 150Ω to GND		3.18		V
V_{OL}	Output Voltage Low Swing	V_{IN} = -0.3V, R_L =75Ω		0.05		V
I_{SC}	Short-circuit current	V_{IN} =2V, output to GND through 10Ω	65			mA
		V_{IN}=100mV, output short to V_{DD}	65			mA
V_{IL}	Disable Threshold	V_{DD} = 3.0V to 5.5V			0.8	V
V_{IH}	Enable Threshold	V_{DD} = 3.0V to 5.5V	1.6			V
R_{OUT}	Output Impedance	EN = 0V DC		12		kΩ
		EN = 0V, f = 4.5MHz		5.8		kΩ

Note: (1). 100% tested at T_A=25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AC Electrical Specifications						
f_{-1dB}	-1dB Bandwidth(2)	R_L=150Ω	7.6	8.2	9.1	MHz
f_{-3dB}	-3dB Bandwidth(2)	R_L=150Ω	7.8	9	10.5	MHz
Att_{27MHz}	Stop Band Attenuation (2)	f = 27MHz	38.2	57.2	73.6	dB
SR	Slew Rate	2V output step, 80% to 20%		38		V/μs
dG	Differential Gain	Video input range 1V		0.4	1.2	%
dP	Differential Phase	Video input range 1V		0.7	1.5	°
THD	Total Harmonic Distortion	TPF110: f=1MHz, V_{OUT}=1.4V_{PP}	0.03	0.1	0.2	%
		TPF110L: f=1MHz, V_{OUT}=1.4V_{PP}		0.2		%
D/DT	Group Delay Variation	f = 100kHz, 5MHz		5.4		ns
t_{PD}	Propagation Delay	Maximum delay from input to output: 100kHz to 4.43MHz	54	80.7	127	ns
	Input-to-Output Isolation (Disabled)	f = 1MHz, V_{IN}=0.7V_{PP}	-89	-96		dB
SNR	Signal-to-Noise Ration	f= 100kHz to 4.43MHz	65	68		dB
t_{ON}	Enable Time	V_{IN} = 500mV, V_{OUT} to 1%		1000		ns
t_{OFF}	Disable Time	V_{IN} = 500mV, V_{OUT} to 1%		45		ns
CLG	Chroma-Luma-Gain(2)	400kHz to 3.58MHz and 4.43MHz		0.18	0.8	dB
CLD	Chroma-Luma-Delay	400kHz to 3.58MHz and 4.43MHz		9.2	31	ns
t_F	Falling Time	2.5V_{STEP}, 80% - 20%		25		ns
t_R	Rising Time	2.5V_{STEP}, 20% - 80%		22		ns

Note: (2). Guaranteed by design.

Typical Performance Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

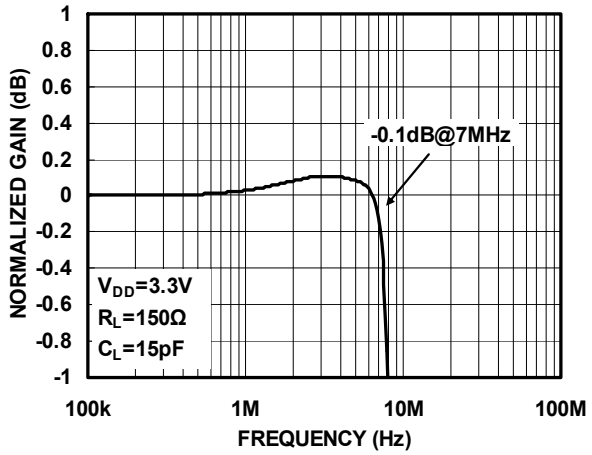


Figure1. Small-Scale Frequency Response

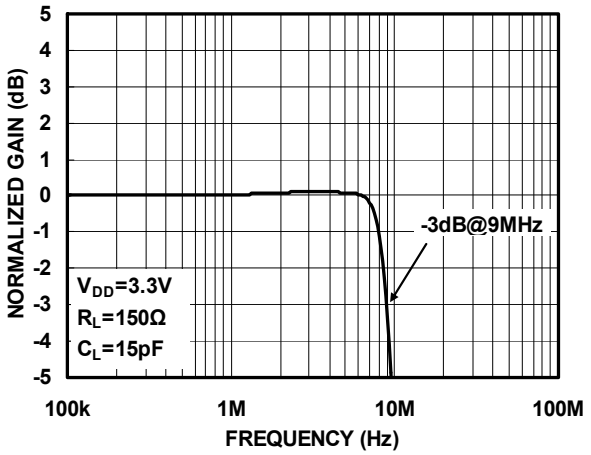


Figure2. Large-Scale Frequency Response

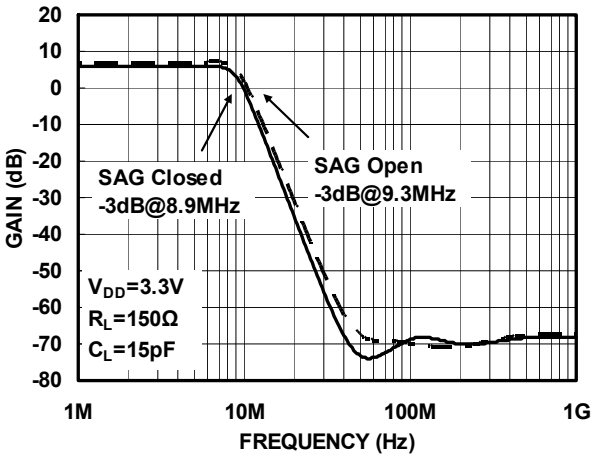


Figure3. Gain Vs. Frequency

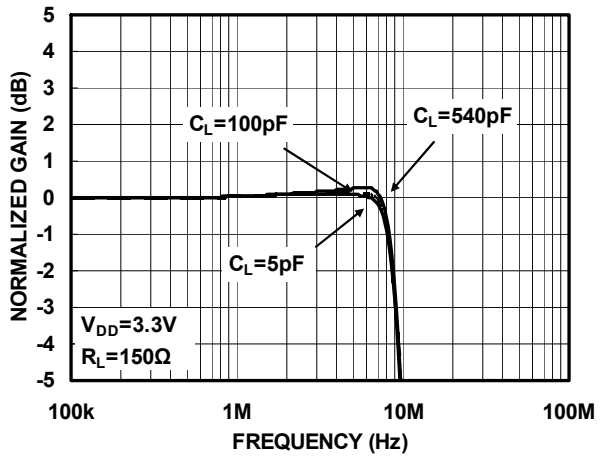


Figure4. Gain Vs. Frequency With C_{LOAD}

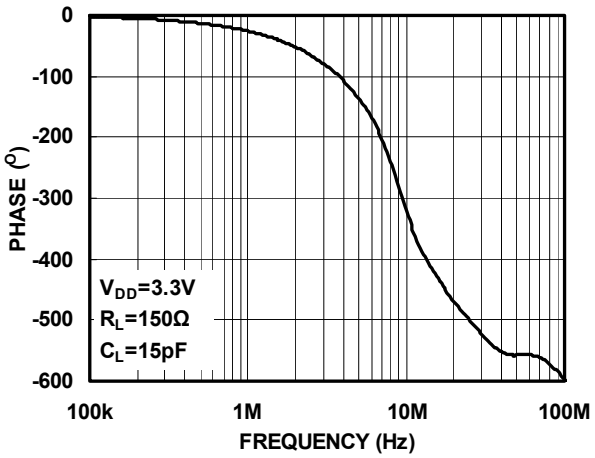


Figure5. Phase Vs. Frequency

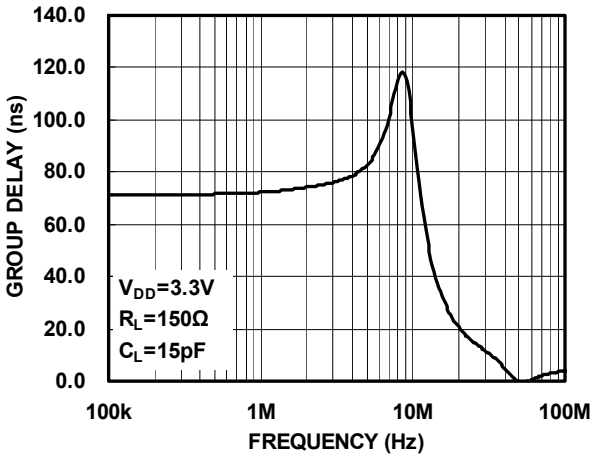


Figure6. Group Delay vs Frequency

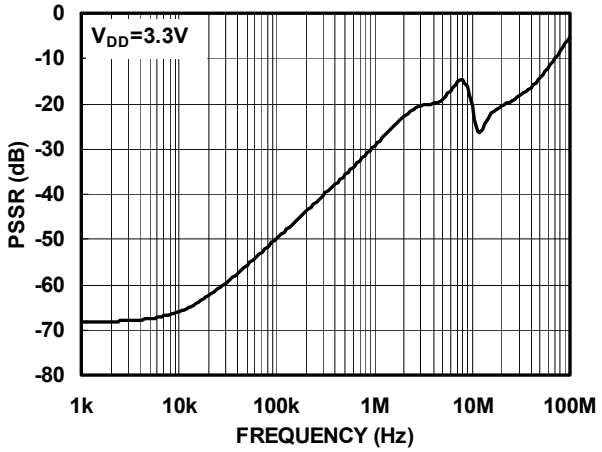


Figure7. PSRR Vs. Frequency

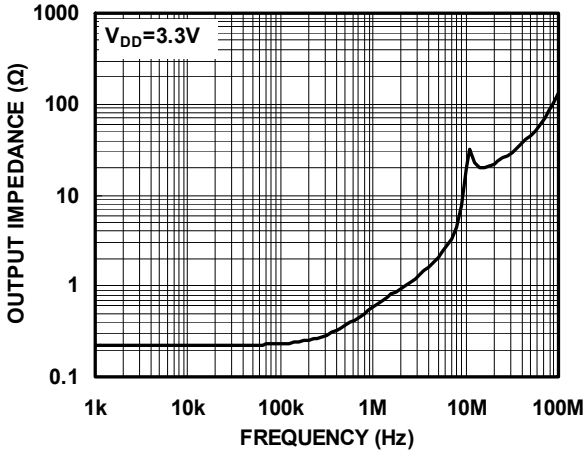


Figure8. Output Impedance Vs. Frequency

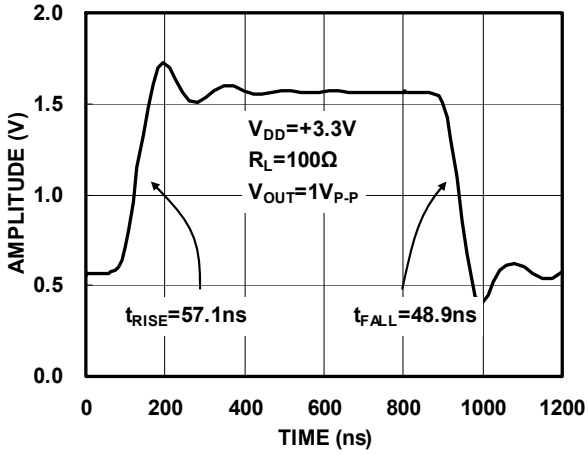


Figure9. Large-Signal Pulse Response Vs. Time

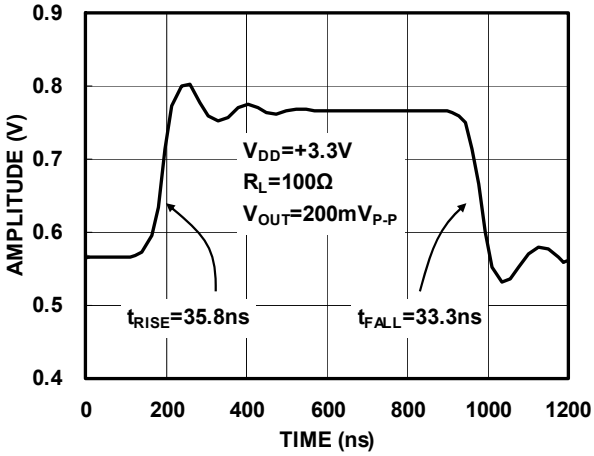


Figure10. Large-Signal Pulse Response Vs. Time

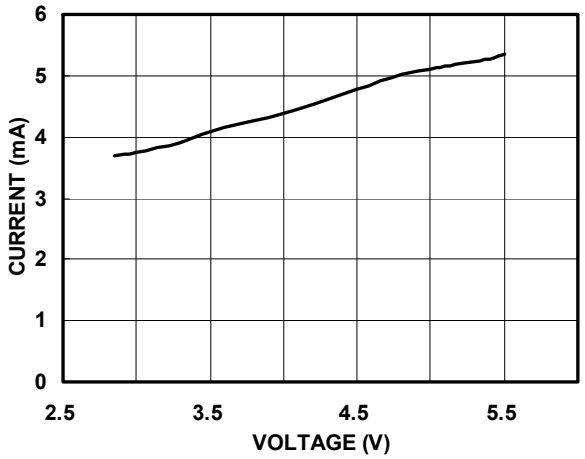


Figure11. Quiescent Current Vs. Power Supply Voltage

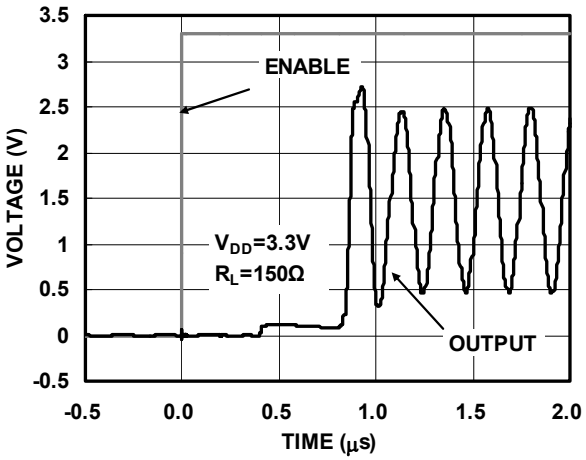


Figure12. Enable Response Time

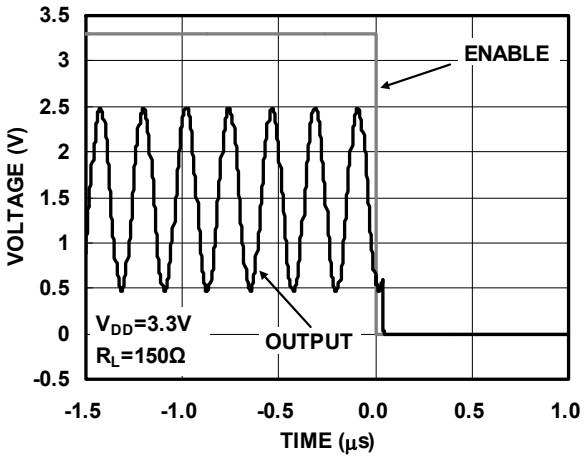


Figure13. Disable Response Time

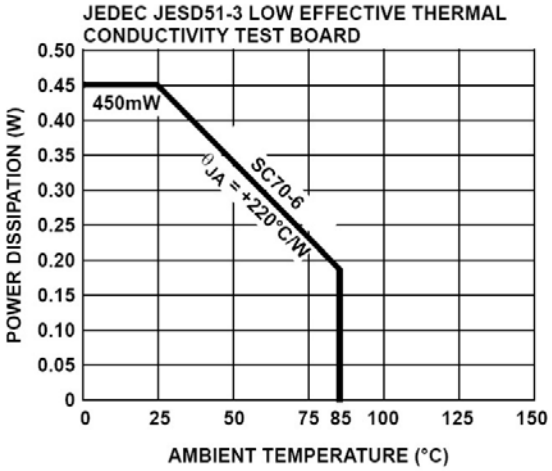


Figure14. Package Power Dissipation Vs. Ambient Temperature

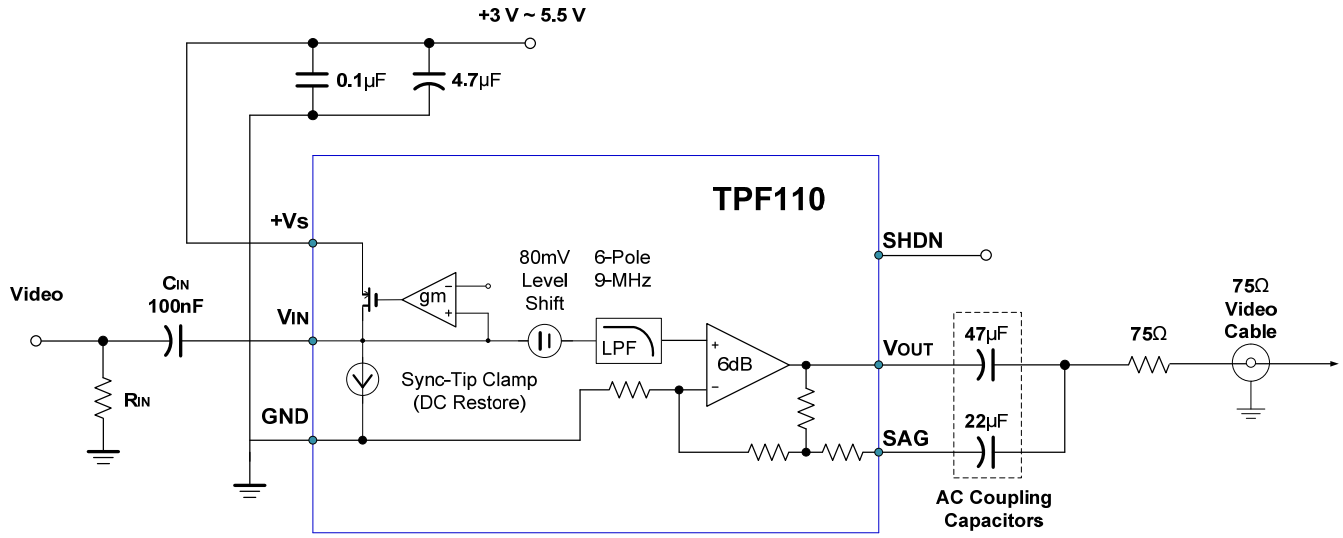


Figure15. Typical Application

Application Information

The TPF110/TPF110L is a single supply rail-to-rail output amplifier achieving a -3dB bandwidth of around 9MHz and slew rate of about 38V/µs while demanding only 3.85mA of supply current. This part is ideally suited for applications with specific micro power consumption and high bandwidth demands. As the performance characteristics above and the features described below, the TPF110/TPF110L is designed to be very attractive for portable composite video applications.

The TP110/TP110L features a sync clamp, low pass function, and SAG network at the output facilitating reduction of typically large AC coupling capacitors. See Figure 15.

Internal Sync Clamp

The typical embedded video DAC operates from a ground referenced single supply. This becomes an issue because the lower level of the sync pulse output may be at a 0V reference level to some positive level. The problem is presenting a 0V input to most single supply driven amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degrading the video image. A larger positive reference

may offset the input above its positive range.

The TPF110/TPF110L features an internal sync clamp and offset function to level shift the entire video signal to the best level before it reaches the input of the amplifier stage. These features are also helpful to avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The simplified block diagram of the TPF110/TPF110L in Page-1.The AC coupled video sync signal is pulled negative by a current source at the input of the comparator amplifier. When the sync tip goes below the comparator threshold the output comparator is driven negative, The PMOS device turns on clamping sync tip to near ground level. The network triggers on the sync tip of video signal.

Low Pass Filter--Sallen Key

The Sallen Key is a classic low pass configuration. This provides a very stable low pass function, and in the case of the TPF110/TPF110L, a six-pole roll-off at around 9MHz. The six-pole function is accomplished with an RC low pass network placed in series with and before the Sallen Key.

Output Couple

TPF110/TPF110L output could support both “AC Couple” and “DC Couple”, if use “AC Couple”, this capacitor is typically between 220-μF and 1000-μF, although 470-μF is common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document.

The TPF110/TPF110L internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, thereby saving board space and additional expense for capacitors. This makes the TPF110/TPF110L extremely attractive for portable video applications. Additionally, this solution completely eliminates the issue of field tilt in the lower frequency. The trade off is greater demand of supply current. Typical load current for AC coupled is around 1mA, compared to typical 6.6mA used when DC coupling.

Output Drive Capability and Power Dissipation

With the high output drive capability of the TPF110/TPF110L, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area. The maximum power dissipation allowed in a package is determined according to Equation:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where：
T_{JMAX} = Maximum junction temperature
T_{AMAX} = Maximum ambient temperature
Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or: for sourcing:

$$PD_{MAX} = V_s \times I_{SMAX} + (V_s - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

Where：
V_S = Supply voltage
I_{SMAX} = Maximum quiescent supply current
V_{OUT} = Maximum output voltage of the application
R_{LOAD} = Load resistance tied to ground

By setting the two PDMAX equations equal to each other, we can solve the output current and RLOAD to avoid the device overheat.

Power Supply Bypassing Printed Circuit Board Layout

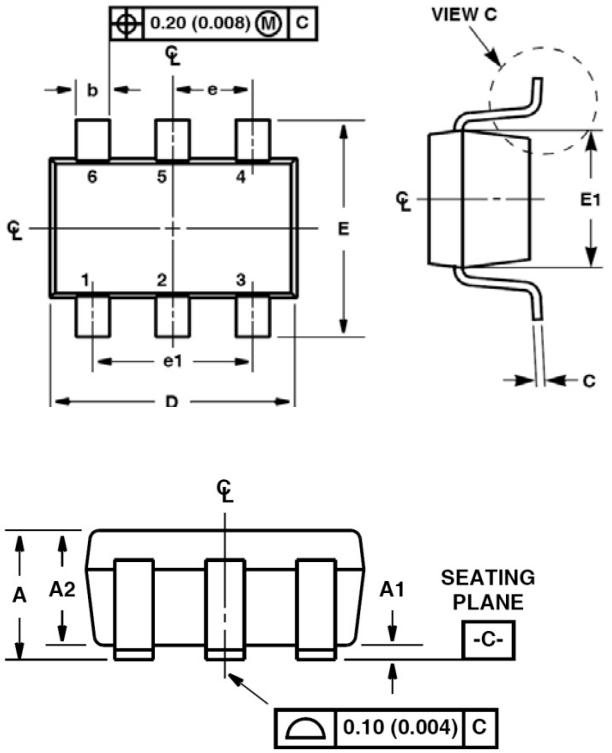
As with any modern operational amplifier, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor from VS+ to GND will suffice.

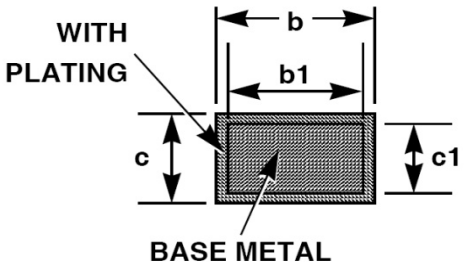
VIDEO FILTER DRIVER SELECTION GUIDE

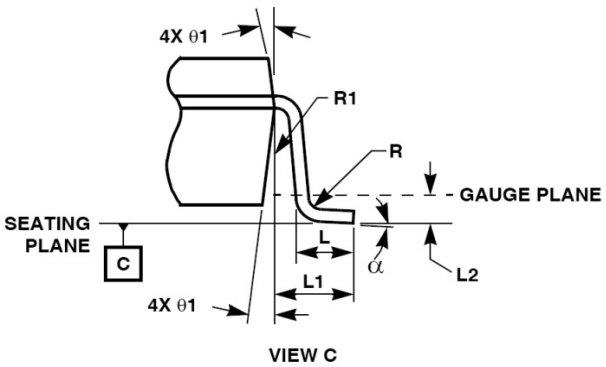
P/N	Product Description	Channel	-3dB Bandwidth	Package
TPF111	Low power, 1 channel 6th order 9MHz	1-SD	9MHz	SC70-5 SO-8
TPF113	Low power 3 channel, 6th-order 9MHz SD video filter	3-SD	9MHz	SO-8
TPF114	Low power 4 channel, 6th-order 9MHz SD video filter	4-SD	9MHz	MSOP-10 TSSOP-14
TPF116	Low power 4 channel, 6th-order 9MHz SD video filter for CVBS, SVIDEO	6-SD	9MHz	TSSOP-14
TPF123	3 channel 6th-order 13.5MHz, 960H/720H-CVBS video filter or Y'Pb'Pr 480P/576P video filter	3-ED	13.5MHz	SO-8
TPF133	Low power 3 channel, 6th-order 36MHz HD video filter	3-HD	36MHz	SO-8
TPF134	Low power 3 channel, 6th-order 36MHz HD video filter and 1 channel SD video filter	1-SD& 3-SD	9MHz 36MHz	MSOP-10 TSSOP-14
TPF136	Low power 3 channel, 6th-order 36MHz HD video filter and 3 channel SD video filter	3-SD& 3-HD	9MHz 36MHz	TSSOP-20
TPF143	Low power 3 channel, 6th-order 72MHz Full HD video filter	3-FHD	72MHz	SO-8
TPF144	Low power 3 channel, 6th-order 72MHz Full HD video filter and 1 channel SD video filter	1-SD& 3-FHD	9MHz 72MHz	MSOP-10 TSSOP-14
TPF146	Low power 3 channel, 6th-order 72MHz Full HD video filter and3 channel SD video filter	3-SD& 3-FHD	9MHz 72MHz	TSSOP-20
TPF153	Low power 3 channel, 6th-order 220MHz Full HD video filter	3-CH	220MHz	SO-8

封装信息

Small Outline Transistor Plastic Packages (SC70-6)







6 LEAD OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.039	0.80	1.00	-
A1	0.001	0.004	0.025	0.10	-
A2	0.034	0.036	0.85	0.90	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	-
c	0.004	0.008	0.10	0.20	6
c1	0.004	0.006	0.10	0.15	6
D	0.073	0.085	1.85	2.15	3
E	0.084BSC		2.1 BSC		-
E1	0.045	0.053	1.15	1.35	3
e	0.0256Ref		0.65 Ref		-
e1	0.0512Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.016 Ref		04.00 Ref		-
L2	0.006 BSC		0.15 BSC		-
N	6		6		5
R	0.04	-	0.10	-	-
α	0°	8°	0°	8°	-

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO203AB.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

IMPORTANT NOTICE

"PRELIMINARY" PRODUCT INFORMATION DESCRIBES PRODUCTS THAT ARE IN PRODUCTION, BUT FOR WHICH FULL CHARACTERIZATION DATA IS NOT YET AVAILABLE.

3PEAKIC MICROELECTRONICS CO. LTD BELIEVES THAT THE INFORMATION CONTAINED IN THIS DOCUMENT IS ACCURATE AND RELIABLE. HOWEVER, THE INFORMATION IS SUBJECT TO CHANGE WITHOUT NOTICE AND IS PROVIDED “AS IS” WITHOUT WARRANTY OF ANY KIND (EXPRESS OR IMPLIED). CUSTOMERS ARE ADVISED TO OBTAIN THE LATEST VERSION OF RELEVANT INFORMATION TO VERIFY, BEFORE PLACING ORDERS, THAT INFORMATION BEING RELIED ON IS CURRENT AND COMPLETE. ALL PRODUCTS ARE SOLD SUBJECT TO THE TERMS AND CONDITIONS OF SALE SUPPLIED AT THE TIME OF ORDER ACKNOWLEDGMENT, INCLUDING THOSE PERTAINING TO WARRANTY, INDEMNIFICATION, AND LIMITATION OF LIABILITY. NO RESPONSIBILITY IS ASSUMED BY 3PEAKIC MICROELECTRONICS CO. LTD FOR THE USE OF THIS INFORMATION, INCLUDING USE OF THIS INFORMATION AS THE BASIS FOR MANUFACTURE OR SALE OF ANY ITEMS, OR FOR INFRINGEMENT OF PATENTS OR OTHER RIGHTS OF THIRD PARTIES. THIS DOCUMENT IS THE PROPERTY OF 3PEAKIC MICROELECTRONICS CO. LTD AND BY FURNISHING THIS INFORMATION, 3PEAKIC MICROELECTRONICS CO. LTD GRANTS NO LICENSE, EXPRESS OR IMPLIED UNDER ANY PATENTS, MASK WORK RIGHTS, COPYRIGHTS, TRADEMARKS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS. 3PEAKIC MICROELECTRONICS CO. LTD OWNS THE COPYRIGHTS ASSOCIATED WITH THE INFORMATION CONTAINED HEREIN AND GIVES CONSENT FOR COPIES TO BE MADE OF THE INFORMATION ONLY FOR USE WITHIN YOUR ORGANIZATION WITH RESPECT TO 3PEAKIC MICROELECTRONICS CO. LTD INTEGRATED CIRCUITS OR OTHER PRODUCTS OF 3PEAKIC MICROELECTRONICS CO. LTD. THIS CONSENT DOES NOT EXTEND TO OTHER COPYING SUCH AS COPYING FOR GENERAL DISTRIBUTION, ADVERTISING OR PROMOTIONAL PURPOSES, OR FOR CREATING ANY WORK FOR RESALE.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). 3PEAKIC MICROELECTRONICS CO. LTD PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF 3PEAKIC MICROELECTRONICS CO. LTD PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND INCLUSION DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY DISCLAIMS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF 3PEAKIC MICROELECTRONICS CO. LTD PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY 3PEAKIC MICROELECTRONICS CO. LTD, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

THE LOGO DESIGNS OF 3PEAKIC MICROELECTRONICS CO. LTD ARE TRADEMARKS OF DESIGNS. ALL OTHER BRAND AND PRODUCT NAMES IN THIS DOCUMENT MAY BE TRADEMARKS OR SERVICE MARKS OF THEIR RESPECTIVE OWNERS.

Contact information:

USA: 635 W. Alma School Road, Suite102

Chandler, USA.

AZ 85234

Shanghai-China: Room 401-407 No.1278 Keyuan Road,

Zhangjiang High-tech Park, Pudong New District,

Shanghai, China

Zip Code: 201203

Suzhou-China: Suite 304, Building B2, Creative Industrial Park,

No.328 Xinghu Street, Industrial Park,

Suzhou, Jiangsu Province, China

Zip Code: 215123