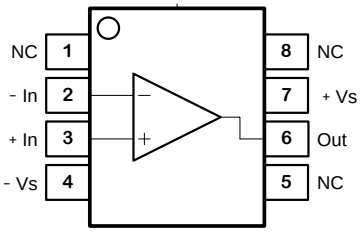
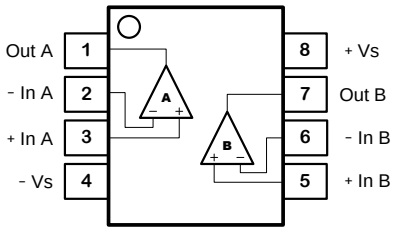
Pin Configuration (Top View, continued)

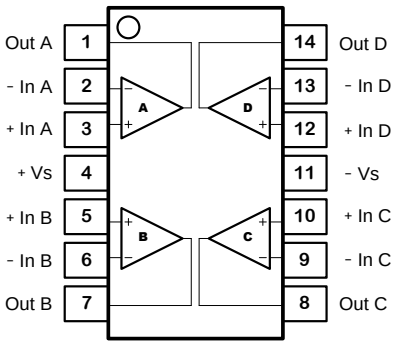
TP5531
8-Pin SOIC
(-S Suffix)



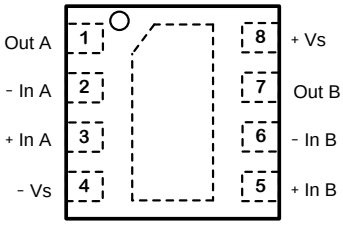
TP5532
8-Pin SOIC/MSOP
(-S and -V Suffixes)



TP5534
14-Pin SOIC/TSSOP
(-S and -T Suffixes)



TP5532
8-Pin DFN
(-F Suffixes)



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP5531	TP5531-TR	SOT23-5	Tape and Reel, 3,000	E31T
	TP5531-CR	SC70-5 (SOT353)	Tape and Reel, 3,000	31C
	TP5531-SR	SOIC-8	Tape and Reel, 4,000	TP5531
TP5531U	TP5531U-TR	SOT23-5	Tape and Reel, 3,000	E31U
	TP5531U-CR	SC70-5	Tape and Reel, 3,000	31V
TP5532	TP5532-SR	SOIC-8	Tape and Reel, 4,000	TP5532
	TP5532-FR	DFN-8 2*2	Tape and Reel, 3,000	532
	TP5532-VR	MSOP-8	Tape and Reel, 3,000	TP5532
TP5534	TP5534-SR	SOIC-14	Tape and Reel, 2,500	TP5534
	TP5534-TR	TSSOP-14	Tape and Reel, 3,000	TP5534

Absolute Maximum Ratings Note 1

Supply Voltage: 6V
Input Voltage: ..... ……V^- – 0.2 to V^+ + 0.2
Input Current: +IN, –IN Note 2..... ±20mA
Output Short-Circuit Duration Note 3..... Indefinite
Current at Supply Pins……..... ±50mA

Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	2	kV

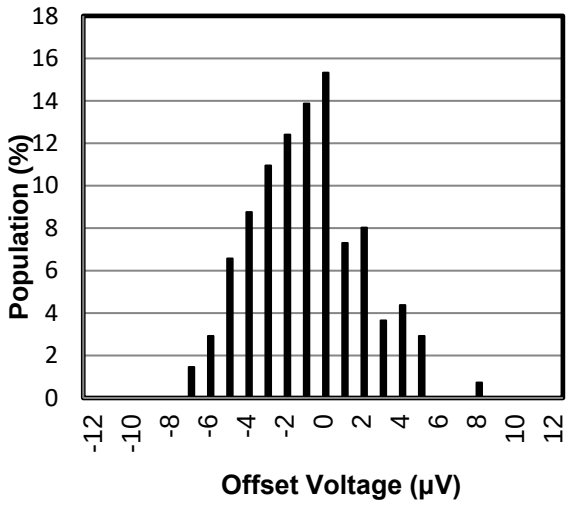
Electrical Characteristics

At T_A = 27°C, V_S = 5V, R_L = 10kΩ, V_{CM} = V_{DD}/2, unless otherwise noted.

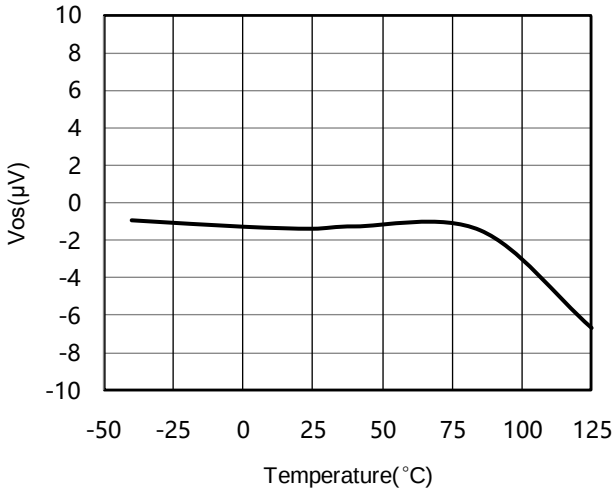
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_S	Supply Voltage Range		1.8		5.5	V
I_Q	Quiescent current per amplifier	TP5531		45	65	μA
		TP5532/TP5534		42	60	μA
V_{OS}	Input Offset Voltage	V_{CM} = 2.5V	-10	1	10	μV
		V_{CM} = 0.05 to 4.95V	-20		20	μV
		V_S = 1.8V, V_{CM} = 0.9V	-20		20	μV
dV_{OS}/dT	vs temperature			0.008	0.05	μV/°C
PSRR	vs power supply	Vs = 3V to 5V	100	120		dB
V_n	input voltage noise, f=0.01Hz to 1Hz			0.4		$μV_{pp}$
	input voltage noise, f=0.1Hz to 10Hz			1.1		$μV_{pp}$
e_n	Input voltage noise density, f=1kHz			55		nV/√Hz
C_{IN}	Input capacitor, Differential			3		pF
	Input capacitor, Common-Mode			2		pF
I_B	Input Bias Current			±50		pA
	Over temperature			±800		pA
I_{OS}	Input offset current			±100		pA
V_{CM}	Common-mode voltage range		(V-) – 0.1		(V+)+0.1	V
CMRR	Common-mode rejection ratio	V_{CM}=0.5 to 4.5V	100	120		dB
V_O	Output Voltage Swing from rail	R_L=10kΩ		10	25	mV
I_{SC}	Short-circuit current			±60		mA
GBWP	Unity Gain Bandwidth	C_L=100pF		350		kHz
SR	Slew rate	G=+1, CL=100pF		0.16		V/μs
t_{OR}	Overload recovery time	G=-10		60		μs
t_S	Settling time to 0.01%	C_L=100Pf, G=+1, 5V Step		40		μs
A_{VOL}	Open-Loop Voltage Gain	(V-)+100mV<V_O<(V+)-100mV, R_L = 100kΩ	100	120		dB
$θ_{JA}$	Thermal Resistance Junction to Ambient	SC70-5 (SOT353)		250		°C/W
		SOT23-5		200		
		MSOP-8		210		
		SOIC-8		158		
		SOIC-14		83		
		TSSOP-14		100		

Typical Performance Characteristics

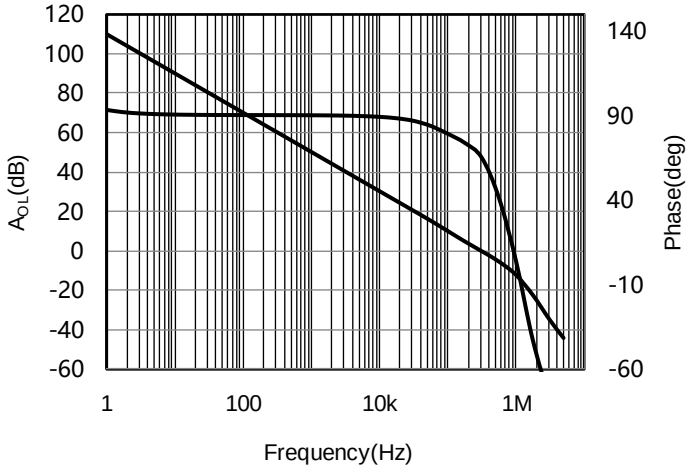
Offset Voltage Distribution



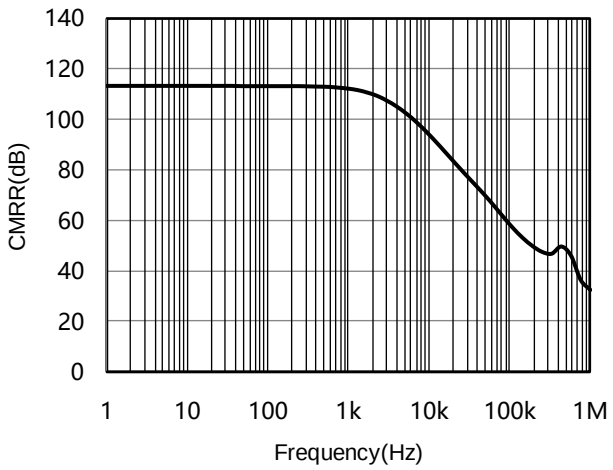
Offset Voltage vs TEMPERATURE



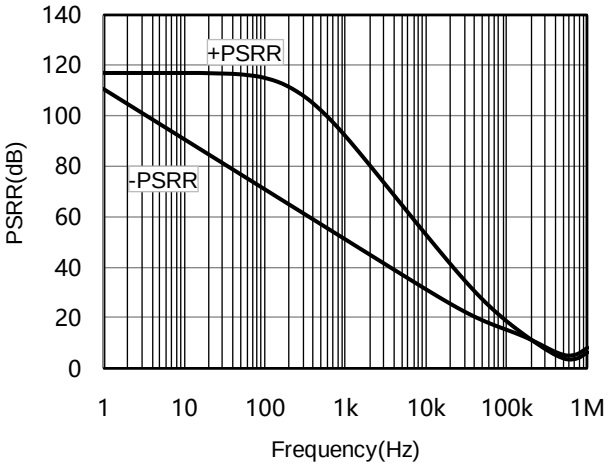
OPEN-LOOP GAIN vs FRENQUENCY



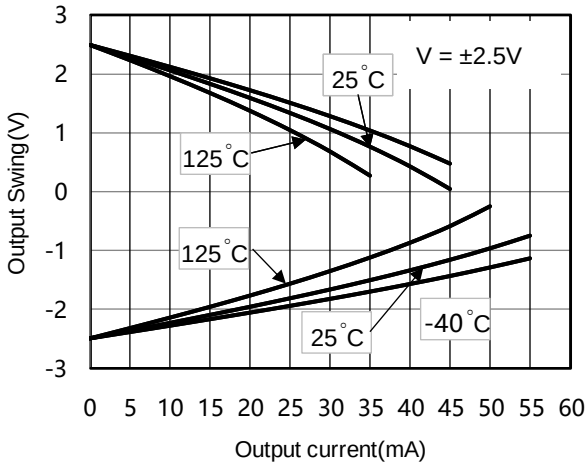
CMRR vs FREQUENCY



PSRR vs FREQUENCY

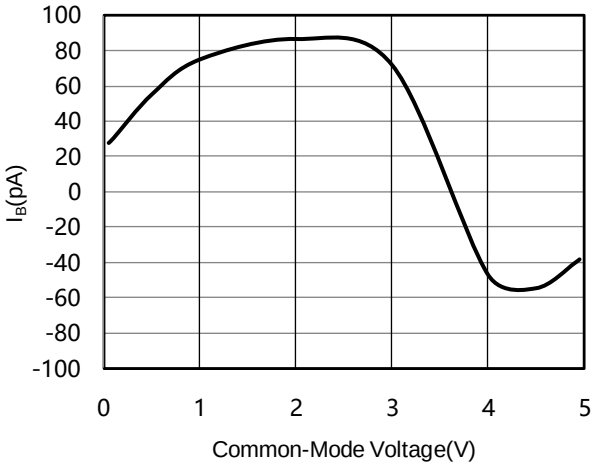


OUTPUT SWING vs LOAD CURRENT

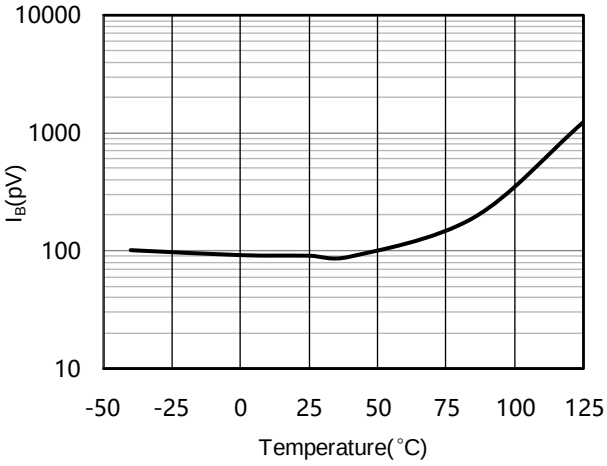


Typical Performance Characteristics(continue)

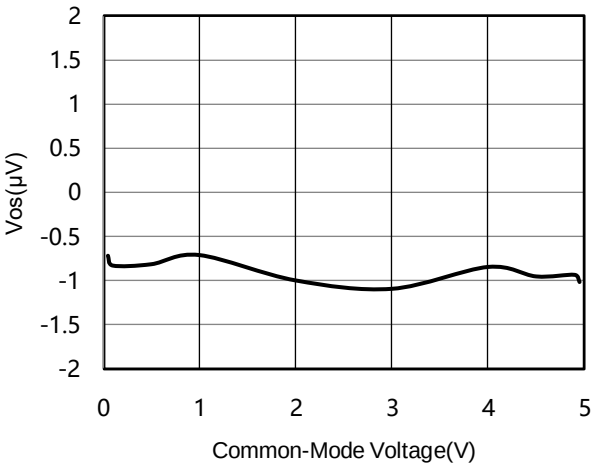
IB vs COMMON-MODE VOLTAGE



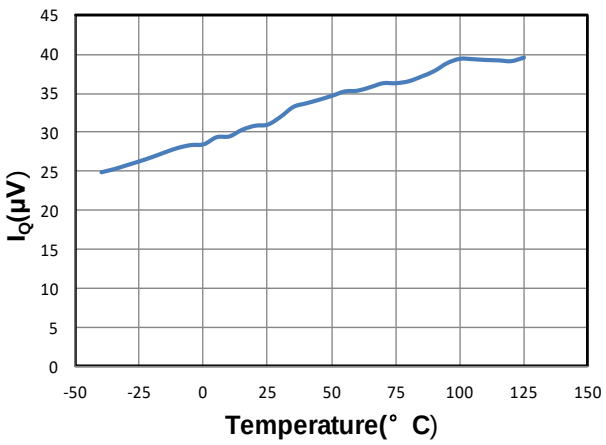
INPUT BIAS vs TEMPERATURE



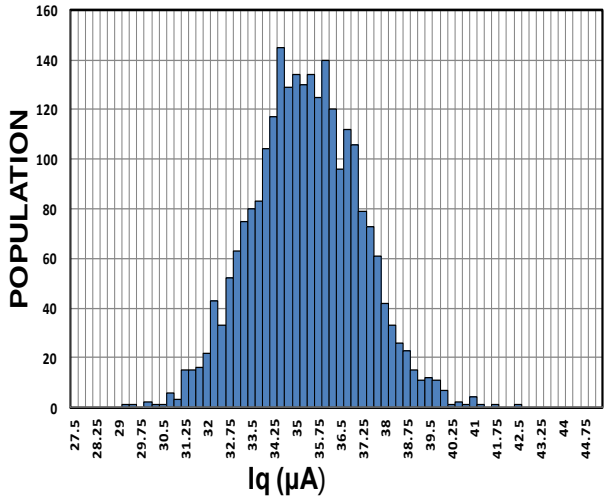
Vosvs COMMON-MODE VOLTAGE



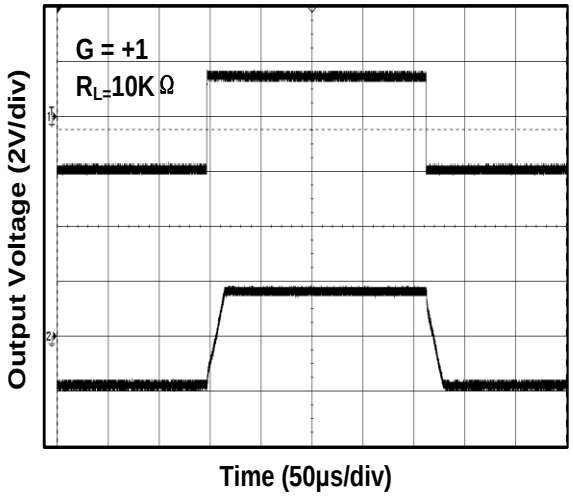
QUIESCENT CURRENT vs TEMPERATURE



Quiescent Current Distribution

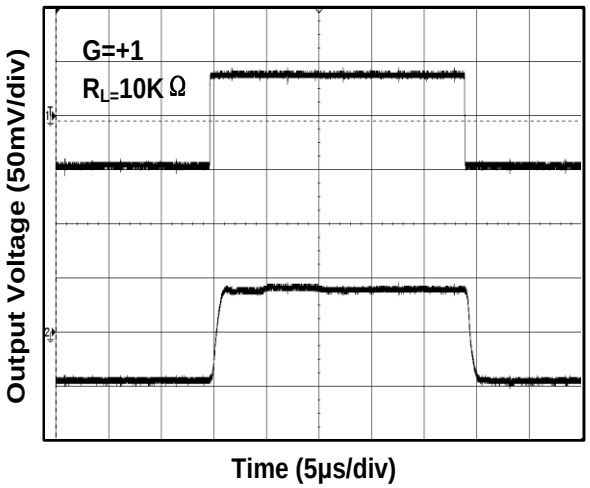


Large-Scale Step Response

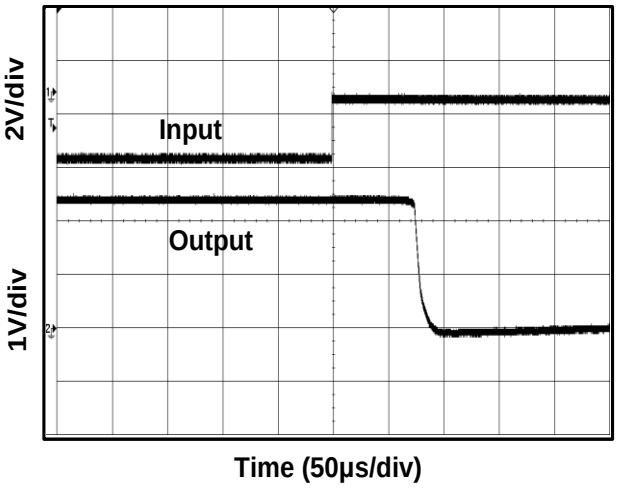


Typical Performance Characteristics(continue)

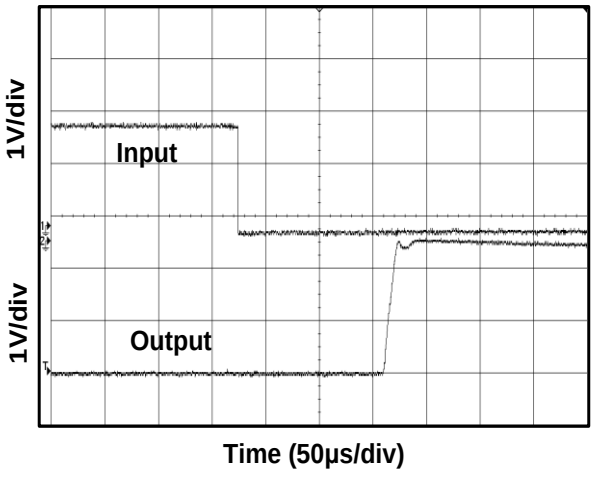
Small-Scale Step Response



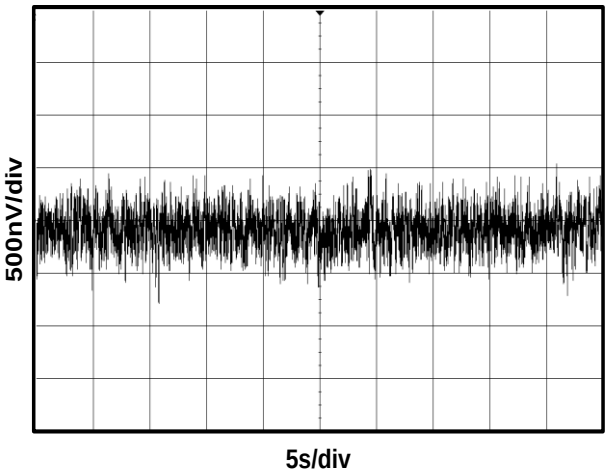
Positive Over-Voltage Recovery



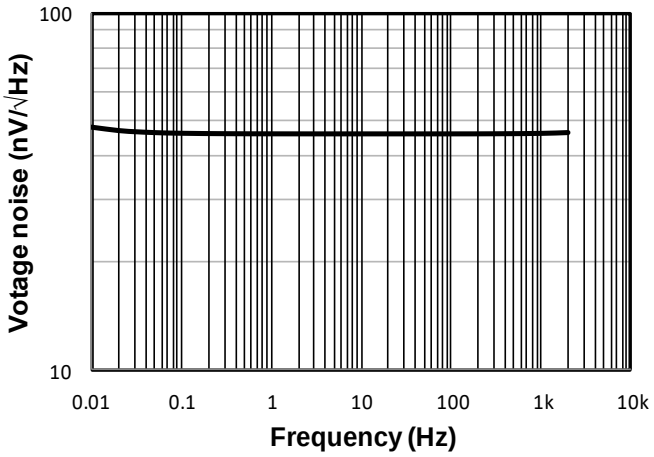
Negative Over-Voltage Recovery



0.1Hz TO 10Hz NOISE

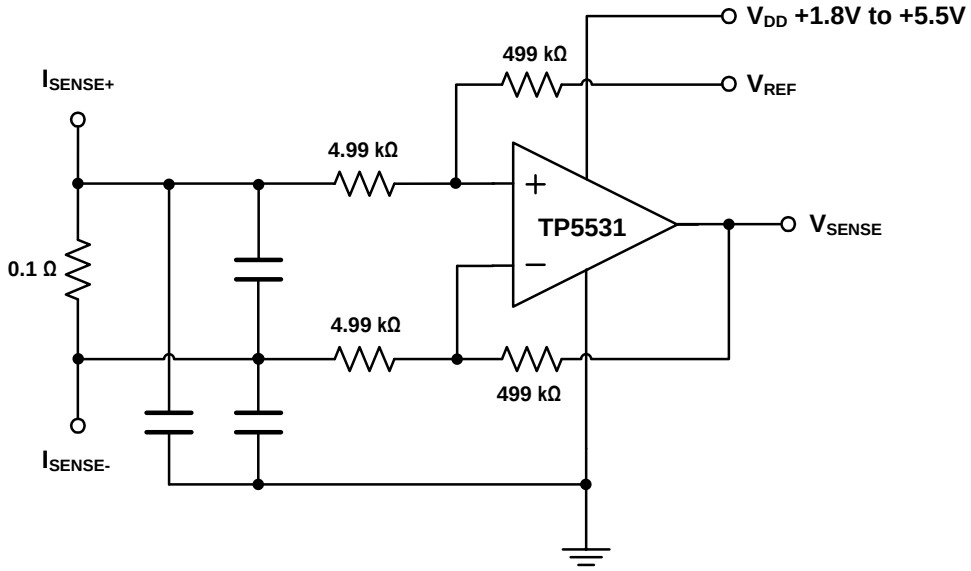


VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

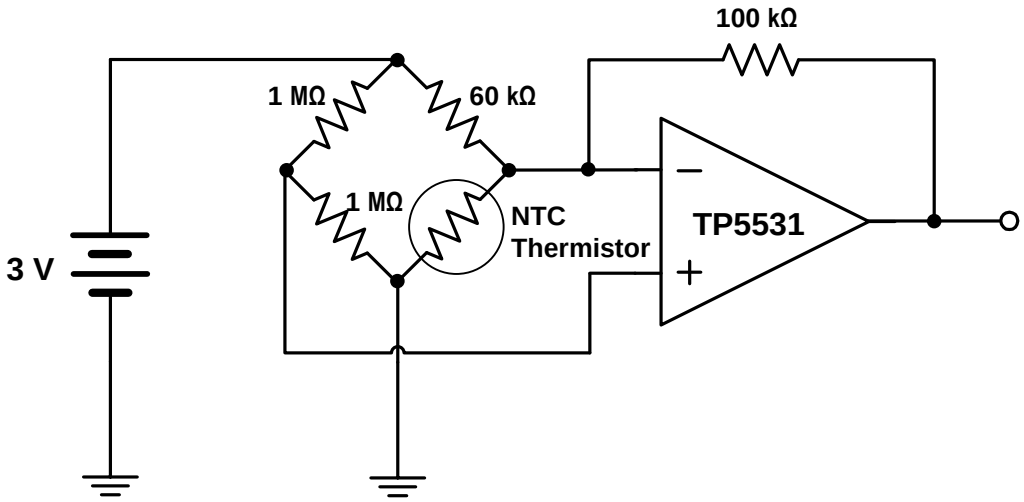


Typical Applications

Bi-Directional Current Sense Amplifier



Thermistor Measurement



Pin Functions

-IN: Inverting Input of the Amplifier.

+IN: Non-Inverting Input of Amplifier.

OUT: Amplifier Output. The voltage range extends to within mV of each supply rail.

V+ or +V_S: Positive Power Supply. Typically the voltage is from 1.8V to 5.5V. Split supplies are possible as long as the voltage between V+ and V– is between 1.8V and 5.5V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V- or -V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 1.8V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible.

Operation

The TP553x series op amps are zero drift, rail-to-rail operation amplifiers that can be run from a single-supply voltage. They use an auto-calibration technique with a time-continuous 350 kHz op amp in the signal path while consuming only 42 μA of supply current per channel. This amplifier is zero-corrected with an 120 kHz clock. Upon power-up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

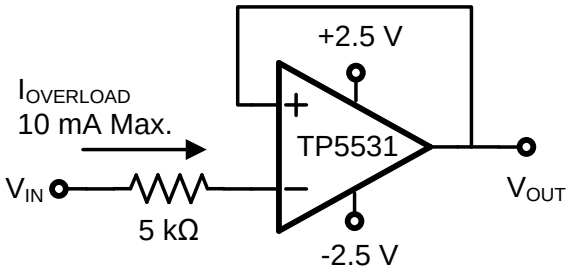
Applications Information

Rail-To-Rail Input And Output

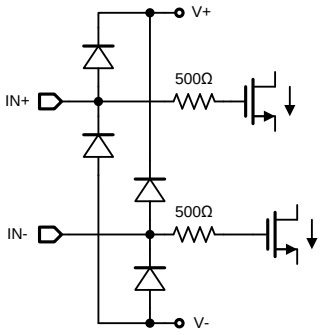
The TP553x series op amps feature rail-to-rail input and output with a supply voltage from 1.8V to 5.5 V. This allows the amplifier inputs to have a wide common mode range (50mV beyond supply rails) while maintaining high CMRR (130dB) and maximizes the signal to noise ratio of the amplifier by having the V_{OH} and V_{OL} levels be at the V+ and V- rails, respectively.

Input Protection

The TP553x series op amps have internal ESD protection diodes that are connect between the inputs and supply rail. When either input exceeds one of the supply rails by more than 300mV, the ESD diodes become forward biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. Thus an external series resistor must be used to ensure the input currents never exceed 10mA.



Current-limiting resistor required if input voltage exceeds supply rails by >0.5V.



INPUT ESD DIODE CURRENT LIMITING-UNITY GAIN

Low Input Referred Noise

Flicker noise, as known as 1/f noise, is inherent in semiconductor devices and increases as frequency decreases. So at lower frequencies, flicker noise dominates, causing higher degrees of error for sub-Hertz frequencies or dc precision application.

The TP553x series amplifiers are chopper stabilized amplifiers, the flicker noise is reduced greatly because of this technique. This reduction in 1/f noise allows the TP553x to have much lower noise at dc and low frequency compared to standard low noise amplifier.

Residual Voltage Ripple

The chopping technique can be used in amplifier design due to the internal notch filter. Although the chopping related voltage ripple is suppressed, higher noise spectrum exists at the chopping frequency and its harmonics due to residual ripple.

So if the frequency of input signal is nearby the chopping frequency, the signal maybe interfered by the residue ripple. To further suppress the noise at the chopping frequency, it is recommended that a post filter be placed at the output of the amplifier.

Broad Band and External Resistor Noise Considerations

The total broadband noise output from any amplifier is primarily a function of three types of noise: input voltage noise from the amplifier, input current noise from the amplifier, and thermal (Johnson) noise from the external resistors used around the amplifier. These noise sources are not correlated with each other and their combined noise can be summed in a root sum squared manner. The full equation is given as:

$$e_n\ total = [e_n^2 + 4kTR_s + (i_n \times R_s)^2]^{1/2}$$

Where:

e_n= the input voltage noise density of the amplifier.

i_n= the input current noise of the amplifier.

R_S= source resistance connected to the noninverting terminal.

k= Boltzmann’ s constant (1.38×10^{-23}J/K). T= ambient temperature in Kelvin (K).

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{n,rms} = e_n\ total \times \sqrt{BW}$$

The input voltage noise density (en) of the TP553x is 55 nV/√Hz, and the input current noise can be neglected. When the source resistance is 190 kΩ, the voltage noise contribution from the source resistor and the amplifier are equal. With source resistance greater than 190 kΩ, the overall noise of the system is dominated by the Johnson noise of the resistor itself.

High Source Impedance Application

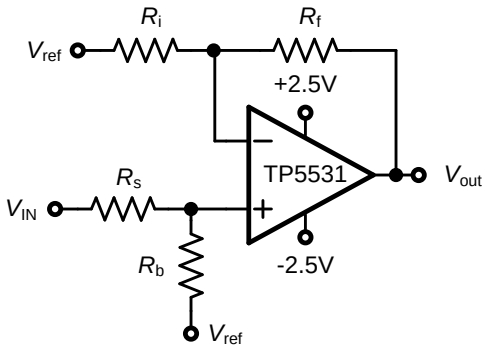
The TP553x series op amps use switches at the chopper amplifier input, the input signal is chopped at 125 kHz to reduce input offset voltage down to 10μV. The dynamic behavior of these switches induces a charge injection current to the input terminals of the amplifier. The charge injection current has a DC path to ground through the resistances seen at the input terminals of the amplifier. Higher input impedance causes an apparent shift in the input bias current of the amplifier.

Because the chopper amplifier has charge injection currents at each terminal, the input offset current will be larger than standard amplifiers. The I_{OS} of TP553x are 150pA under the typical condition. So the input impedance should be

balanced across each input. The input impedance of the amplifier should be matched between the IN+ and IN- terminals to minimize total input offset current. Input offset currents show up as an additional output offset voltage, as shown in the following equation:

$$v_{os,total} = v_{os} - R_f \times I_{os}$$

For a gain configure using 1MΩ feedback resistor, a 150pA total input offset current will have an additional output offset voltage of 0.15mV. By keeping the input impedance low and balanced across the amplifier inputs, the input offset current effect will be suppressed efficiently.



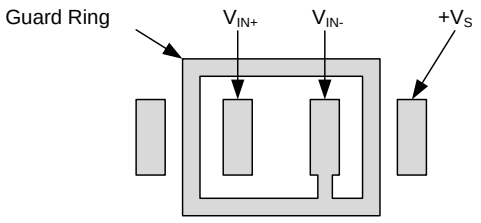
Circuit Implication for reducing Input offset current effect

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 2 for Inverting Gain application.

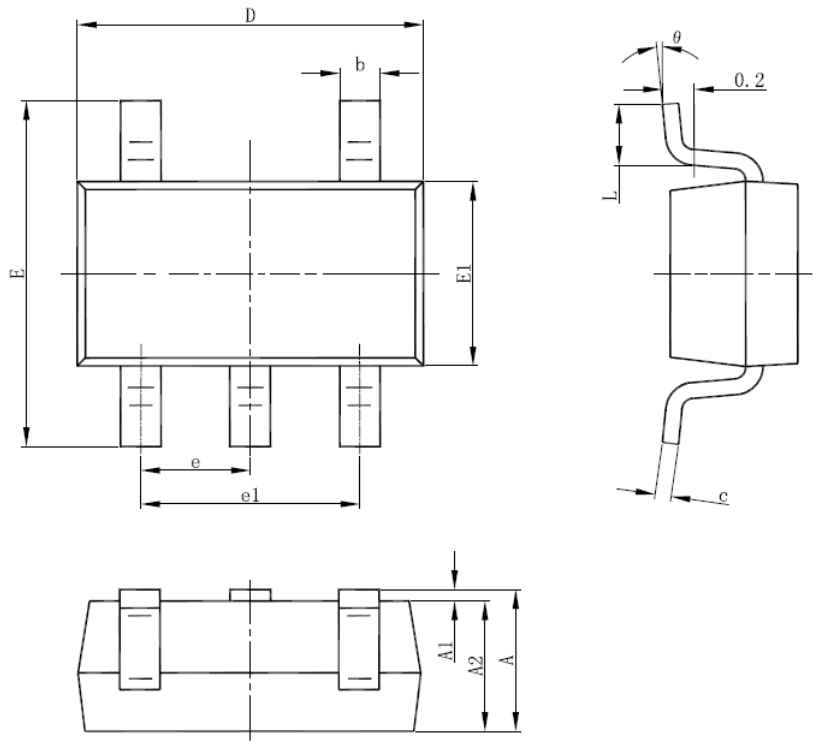
1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.



The Layout of Guard Ring

Package Outline Dimensions

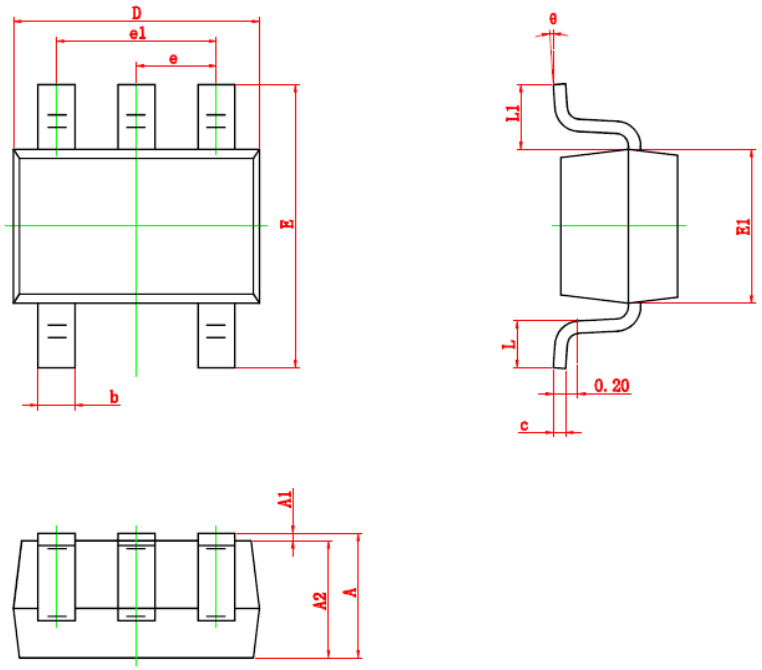
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

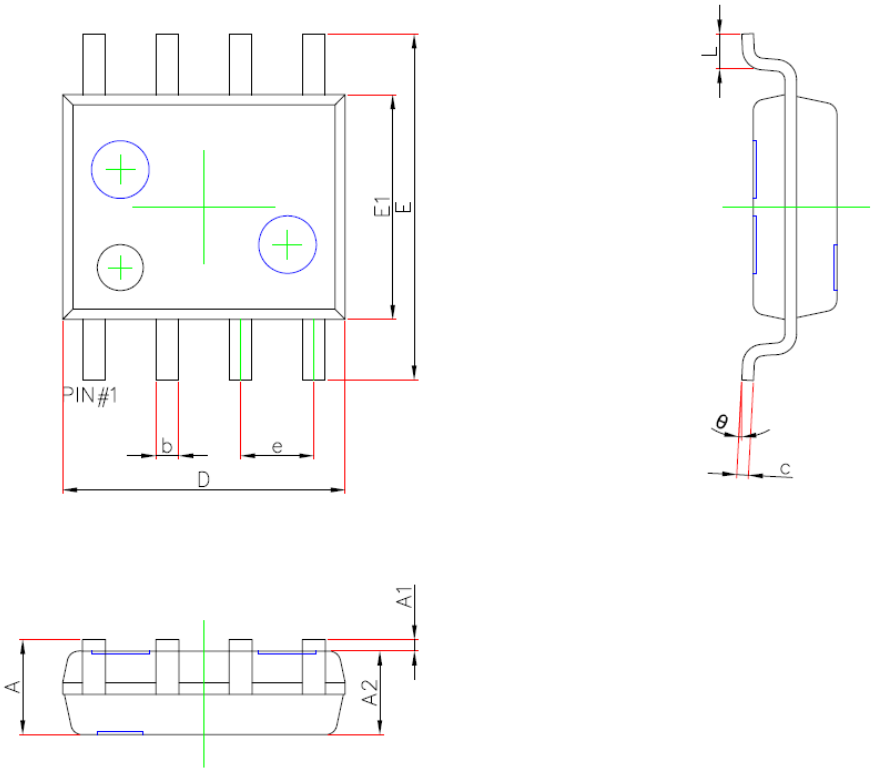
SC-70-5 (SOT353)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525 REF.		0.021 REF.	
θ	0°	8°	0°	8°

Package Outline Dimensions

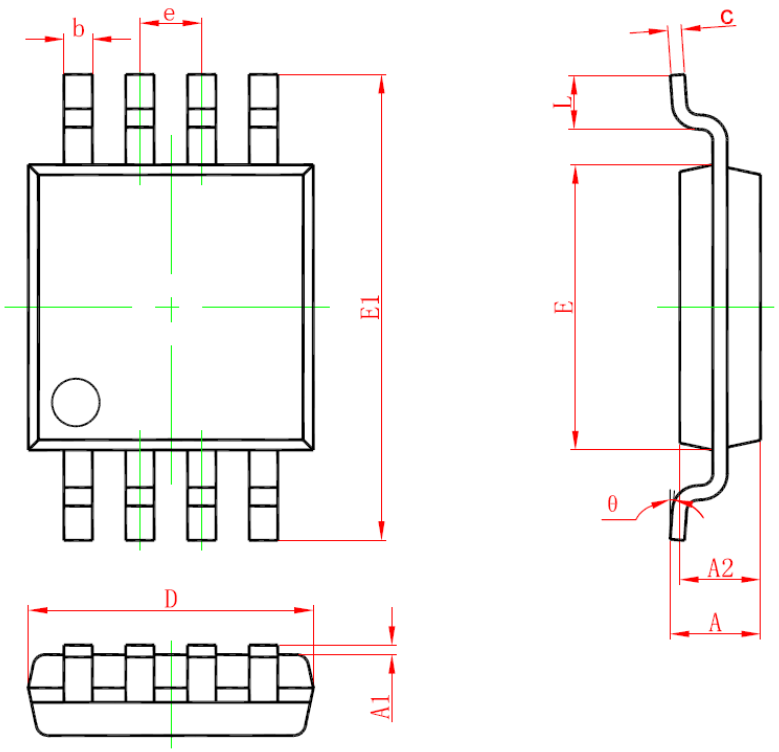
SOP-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Package Outline Dimensions

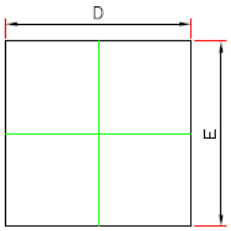
MSOP-8



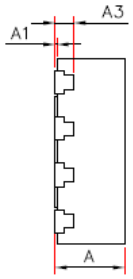
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Package Outline Dimensions

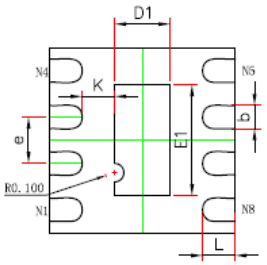
DFN-8 2*2



TOP VIEW



SIDE VIEW

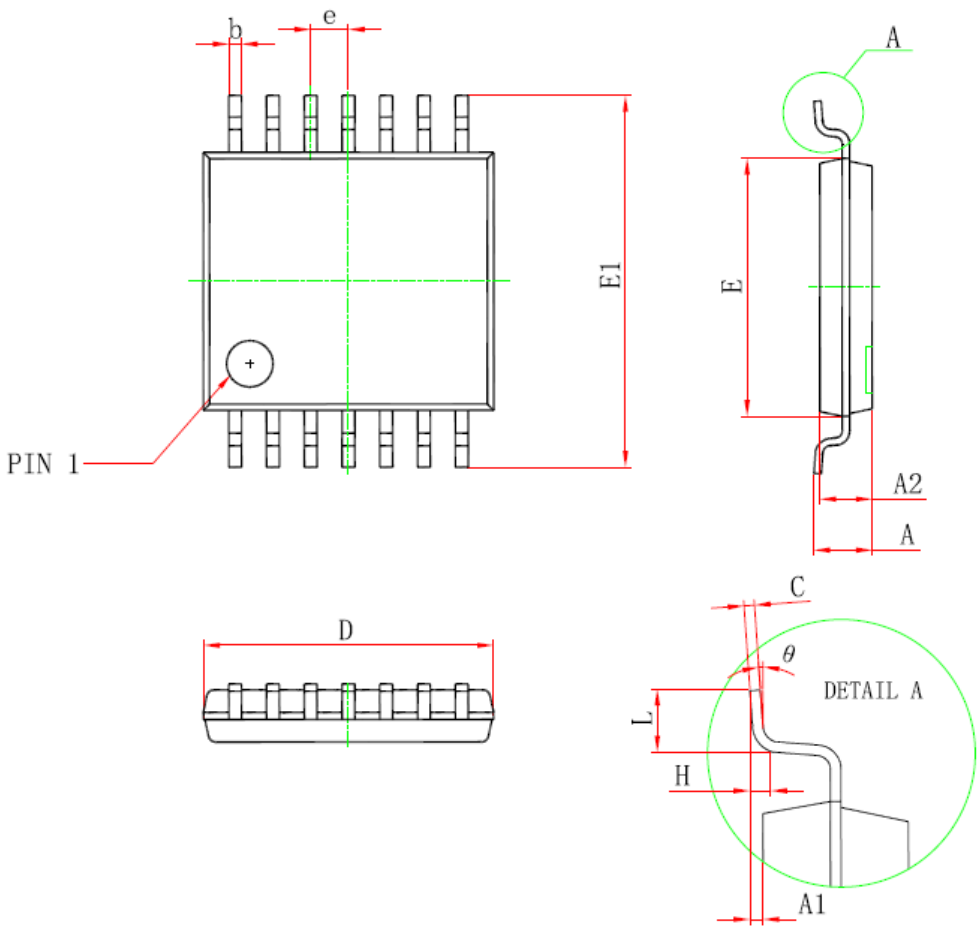


BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.500	0.700	0.020	0.028
E1	1.100	1.300	0.043	0.051
k	0.350REF.		0.014REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.274	0.426	0.011	0.017

Package Outline Dimensions

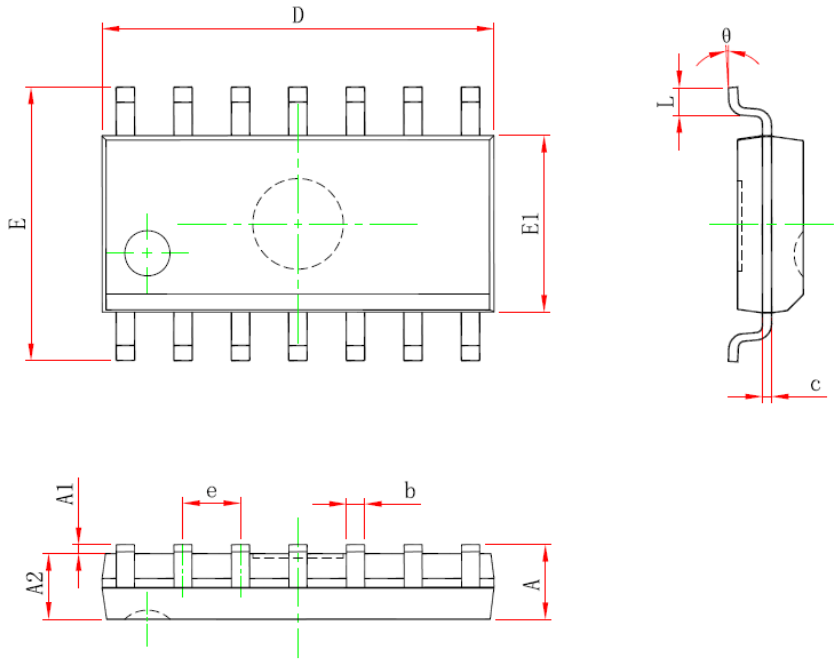
TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Package Outline Dimensions

SOP-14 (SOIC-14)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°