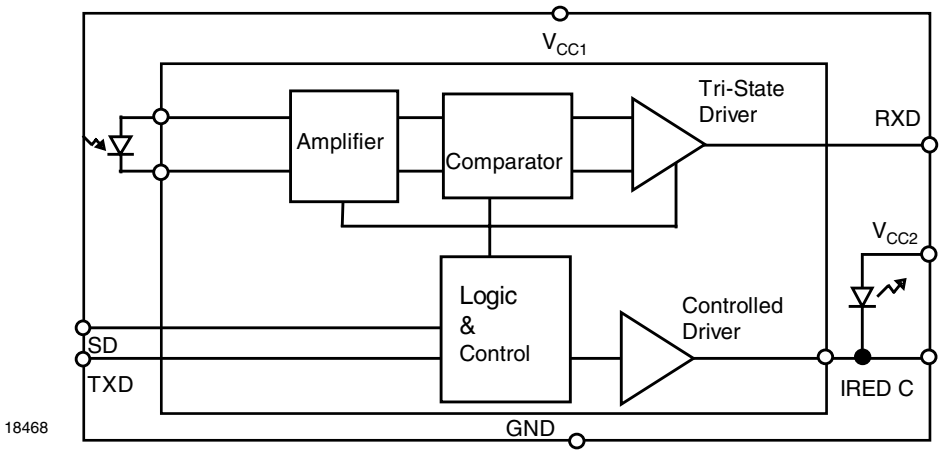
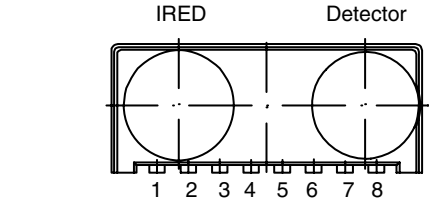
Functional Block Diagram



Pinout

TFDU6102
weight 200 mg

"U" Option BabyFace (Universal)



Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s
FIR: 4 Mbit/s
VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4.A new version of the standard in any case obsoletes the former version.

Note: We apologize to use sometimes in our documentation the abbreviation LED and the word Light Emitting Diode instead of Infrared Emitting Diode (IRED) for IR-emitters. That is by definition wrong; we are here following just a bad trend.

Typical values are for design aid only, not guaranteed nor subject to production testing and may vary with time.

Pin Description

Pin Number	Function	Description	I/O	Active
1	V_{CC2} IRED Anode	Connect IRED anode directly to V_{CC2}. For voltages higher than 3.6 V an external resistor might be necessary for reducing the internal power dissipation. An unregulated separate power supply can be used at this pin.		
2	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	TXD	This input is used to transmit serial data when SD is low. An on-chip protection circuit disables the LED driver if the TXD pin is asserted for longer than 80 µs. When used in conjunction with the SD pin, this pin is also used to receiver speed mode.	I	HIGH
4	RXD	Received Data Output, push-pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. **Floating with a weak pull-up of 500 kΩ (typ.) in shutdown mode.**	O	LOW
5	SD	Shutdown, also used for dynamic mode switching. Setting this pin active places the module into shutdown mode. On the falling edge of this signal, the state of the TXD pin is sampled and used to set receiver low bandwidth (TXD = Low, SIR) or high bandwidth (TXD = High, MIR and FIR) mode. Will be overwritten by the mode pin input, which must float, when dynamic programming is used.	I	HIGH
6	V_{CC1}	Supply Voltage		
7	Mode	HIGH: High speed mode, MIR and FIR; LOW: Low speed mode, SIR only (see chapter "Mode Switching"). Must float, when dynamic programming is used.	I	
	Mode	The mode pin can also be used to indicate the dynamically programmed mode. The maximum load is limited to 50 pF. High indicates FIR/MIR-, low indicates SIR-mode	O	
8	GND	Ground		

Absolute Maximum Ratings

Reference point Ground Pin 8, unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range, transceiver	0 V < V_{CC2} < 6 V	V_{CC1}	- 0.5		+ 6	V
Supply voltage range, transmitter	0 V < V_{CC1} < 6 V	V_{CC2}	- 0.5		+ 6.5	V
Input currents	For all pins, except IRED anode pin				10	mA
Output sinking current					25	mA
Power dissipation	See derating curve, figure 5	P_D			500	mW
Junction temperature		T_J			125	°C
Ambient temperature range (operating)		T_{amb}	- 25		+ 85	°C
Storage temperature range		T_{stg}	- 25		+ 85	°C
Soldering temperature	See recommended solder profile (see figure 4)				260	°C
Average output current		I_{IRED} (DC)			125	mA
Repetitive pulse output current	< 90 µs, t_{on} < 20 %	I_{IRED} (RP)			600	mA
IRED anode voltage		V_{IREDA}	- 0.5		+ 6.5	V
Voltage at all inputs and outputs	V_{in} > V_{CC1} is allowed	V_{IN}			5.5	V
Load at mode pin when used as mode indicator					50	pF

Eye safety information

Reference point Pin: GND unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Virtual source size	Method: (1 - 1/e) encircled energy	d	2.5	2.8		mm
Maximum Intensity for Class 1	IEC60825-1 or EN60825-1, edition Jan. 2001	I_e			*) (500)**)	mW/sr

*) Due to the internal limitation measures the device is a "class1" device

**) IrDA specifies the max. intensity with 500 mW/sr

Electrical Characteristics

Transceiver

T_{amb} = 25 °C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage		V_{CC}	2.7		5.5	V
Supply current (Idle)*)	SD = Low, E_e = 0 klx	I_{CC}		2	3	mA
Supply current (Idle)*)	SD = Low, E_e = 1 klx **)	I_{CC}		2	3	mA
Shutdown supply current	SD = High, Mode = Floating E_e = 0 klx	I_{SD}			2.0	µA
	SD = High, Mode = Floating E_e = 1 klx **)	I_{SD}			2.5	µA
	SD = High, T = 85 °C, Mode = Floating, not ambient light sensitive	I_{SD}			5	µA
Operating temperature range		T_A	- 25		+ 85	°C
Output voltage low	I_{OL} = 1 mA, C_{load} = 15 pF	V_{OL}			0.4	V
Output voltage high	I_{OH} = 500 µA, C_{load} = 15 pF	V_{OH}	0.8 x V_{CC}			V
	I_{OH} = 250 µA, C_{load} = 15 pF	V_{OH}	0.9 x V_{CC}			V
Output RXD current limitation high state	Short to Ground				20	mA
Output RXD current limitation low state	Short to V_{CC1}				20	mA
RXD to V_{CC1} impedance	SD = High	R_{RXD}	400	500	600	kΩ
Input voltage low (TXD, SD, Mode)		V_{IL}	- 0.5		0.5	V
Input voltage high (TXD, SD, Mode)	CMOS level ***)	V_{IH}	V_{CC} - 0.5		V_{CC} + 0.5	V
Input leakage current (TXD, SD)		I_L	- 10		+ 10	µA
Input leakage current Mode		I_{ICH}	- 2		+ 2	µA
Input capacitance (TXD, SD, Mode)		C_{IN}			5	pF

*) Receive mode only.
In transmit mode, add additional 85 mA (typ) for IRED current. Add RXD output current depending on RXD load.

**) Standard Illuminant A.

***) The typical threshold level is 0.5 x V_{CC2}. It is recommended to use the specified min/max values to avoid increased operating current.

Optoelectronic Characteristics

Receiver

T_{amb} = 25 °C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum irradiance *Ee* in angular range **) SIR mode	9.6 kbit/s to 115.2 kbit/s λ = 850 nm to 900 nm	E_e		25 (2.5)	35 (3.5)	mW/m² (µW/cm²)
Minimum irradiance *Ee* in angular range, MIR mode	1.152 Mbit/s λ = 850 nm to 900 nm	E_e		65 (6.5)		mW/m² (µW/cm²)
Minimum irradiance *Ee* inangular range, FIR mode	4.0 Mbit/s λ = 850 nm to 900 nm	E_e		80 (8.0)	90 (9.0)	mW/m² (µW/cm²)
Maximum irradiance Ee in angular range ***)	λ = 850 nm to 900 nm	E_e		5 (500)		kW/m² (mW/cm²)
Maximum no detection irradiance	*)	E_e	4 (0.4)			mW/m² (µW/cm²)
Rise time of output signal	10 % to 90 %, 15 pF	$t_{r\ (RXD)}$	10		40	ns
Fall time of output signal	90 % to 10 %, 15 pF	$t_{f\ (RXD)}$	10		40	ns
RXD pulse width of output signal, 50 %, SIR mode	Input pulse length 1.4 µs < P_{Wopt} < 25 µs	t_{PW}		2.1		µs
	Input pulse length 1.4 µs < P_{Wopt} < 25 µs, - 25 °C < T < 85 °C ****)	t_{PW}	1.5	1.8	2.6	µs
RXD pulse width of output signal, 50 %, MIR mode	Input pulse length P_{Wopt} = 217 ns, 1.152 Mbit/s	t_{PW}	110	250	270	ns
RXD pulse width of output signal, 50 %, FIR mode	Input pulse length P_{Wopt} = 125 ns, 4.0 Mbit/s	t_{PW}	100		140	ns
	Input pulse length P_{Wopt} = 250 ns, 4.0 Mbit/s	t_{PW}	225		275	ns
Stochastic jitter, leading edge	Input irradiance = 100 mW/m², 4.0 Mbit/s				20	ns
	Input irradiance = 100 mW/m², 1.152 Mbit/s				40	ns
	Input irradiance = 100 mW/m², 576 kbit/s				80	ns
	Input irradiance = 100 mW/m², ≤ 115.2 kbit/s				350	ns
Receiver start up time	After completion of shutdown programming sequence Power on delay				500	µs
Latency		t_L		170	300	µs

Note: All timing data measured with 4 Mbit/s are measured using the IrDA® FIR transmission header.
The data given here are valid 5 µs after starting the preamble.

*) This parameter reflects the backlight test of the IrDA physical layer specification to guarantee immunity against light from fluorescent lamps

) IrDA sensitivity definition: **Minimum Irradiance E_e In Angular Range, power per unit area. The receiver must meet the BER specification while the source is operating at the minimum intensity in angular range into the minimum half-angle range at the maximum Link Length

***) Maximum Irradiance Ee In Angular Range, power per unit area. The optical delivered to the detector by a source operating at the maximum intensity in angular range at Minimum Link Length must not cause receiver overdrive distortion and possible related link errors. If placed at the Active Output Interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER). For more definitions see the document “Symbols and Terminology” on the Vishay Website (http://www.vishay.com/docs/82512/82512.pdf).

****) Retriggering once during applied optical pulse may occur.

Transmitter

T_{amb} = 25 °C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
IRED operating current, switched current limiter	See derating curve (fig. 5). For 3.3 V operations no external resistor needed. For 5 V application that might be necessary depending on operating temperature range.	I_D	500	550	600	mA
Output leakage IRED current		I_{IRED}	- 1		1	µA
Output radiant intensity recommended application circuit	α = 0°, 15° TXD = High, SD = Low, $V_{CC1} = V_{CC2}$ = 3.3 V Internally current-controlled, no external resistor	I_e	120	170	350	mW/sr
Output radiant intensity	V_{CC1} = 5.0 V, α = 0°, 15° TXD = Low or SD = High, (Receiver is inactive as long as SD = High)	I_e			0.04	mW/sr
Output radiant intensity, angle of half intensity		α		± 24		°
Peak - emission wavelength		λ_p	880		900	nm
Spectral bandwidth		$\Delta\lambda$		40		nm
Optical rise time, fall time		t_{ropt}, t_{fopt}	10		40	ns
Optical output pulse duration	Input pulse width 217 ns, 1.152 Mbit/s	t_{opt}	207	217	227	ns
	Input pulse width 125 ns, 4.0 Mbit/s	t_{opt}	117	125	133	ns
	Input pulse width 250 ns, 4.0 Mbit/s	t_{opt}	242	250	258	ns
	Input pulse width 0.1 µs < t_{TXD} < 100 µs *)	t_{opt}		t_{TXD}		µs
	Input pulse width $t_{TXD} \geq$ 100 µs *)	t_{opt}	23		100	µs
Optical overshoot					25	%

*) Typically the output pulse duration will follow the input pulse duration t and will be identical in length t.
However, at pulse duration larger than 100 µs the optical output pulse duration is limited to 100 µs. This pulse duration limitation can already start at 23 µs.

Recommended Circuit Diagram

Vishay Semiconductors transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (TXD, SD, Mode) and the output RXD should be directly (DC) coupled to the I/O circuit.

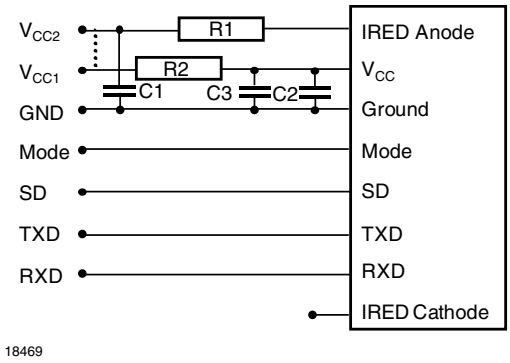


Figure 1. Recommended Application Circuit

The capacitor C1 is buffering the supply voltage and reduces the influence of the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is only necessary for higher operating voltages and elevated temperatures, see derating curve in figure 5, to avoid too high internal power dissipation.

The capacitors C2 and C3 combined with the resistor R2 (as the low pass filter) is smoothing the supply voltage V_{CC1}. R2, C1, C2, and C3 are optional and dependent on the quality of the supply voltages V_{CC1} and V_{CC2} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver. The placement of these parts is critical. It is strongly recommended to position C2 and C3 as close as possible to the transceiver power supply pins. A Tantalum capacitor should be used for C1 and C3 while a ceramic capacitor is used for C2.

In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at V_{CC2}. Often some power supplies are not apply to follow the fast current is rise time. In that case another 4.7 µF (type, see table under C1) at V_{CC2} will be helpful.

Keep in mind that basic RF-design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Wienfield Hill, 1989, Cambridge University Press, ISBN: 0 521 37095 7.

Table 1.
Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1, C3	4.7 µF, 16 V	293D 475X9 016B
C2	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	**5 V supply voltage:** 2 Ω , 0.25 W (recommended using two 1 Ω, 0.125 W resistor in series) **3.3 V supply voltage:** no resistors necessary, the internal controller is able to control the current	e.g. 2 x CRCW-1206-1R0-F-RT1
R2	10 Ω, 0.125 W	CRCW-1206-10R0-F-RT1

I/O and Software

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

Mode Switching

The TFDU6102 is in the SIR mode after power on as a default mode, therefore the FIR data transfer rate has to be set by a programming sequence using the TXD and SD inputs as described below or selected by setting the Mode Pin. The Mode Pin can be used to statically set the mode (Mode Pin: LOW: SIR, HIGH: 0.576 Mbit/s to 4.0 Mbit/s). If not used or in standby mode, the mode input should float or should not be loaded with more than 50 pF. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity.
To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

Setting to the High Bandwidth Mode (0.576 Mbit/s to 4.0 Mbit/s)

1. Set SD input to logic "HIGH".
2. Set TXD input to logic "HIGH". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of TXD, which determines speed setting).
4. After waiting $t_h \geq 200$ ns TXD can be set to logic "LOW". The hold time of TXD is limited by the maximum allowed pulse length.

After that TXD is enabled as normal TXD input and the transceiver is set for the high bandwidth (576 kbit/s to 4 Mbit/s) mode.

Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)

1. Set SD input to logic "HIGH".
2. Set TXD input to logic "LOW". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of TXD, which determines speed setting).
4. TXD must be held for $t_h \geq 200$ ns.

After that TXD is enabled as normal TXD input and the transceiver is set for the lower bandwidth (9.6 kbit/s to 115.2 kbit/s) mode.

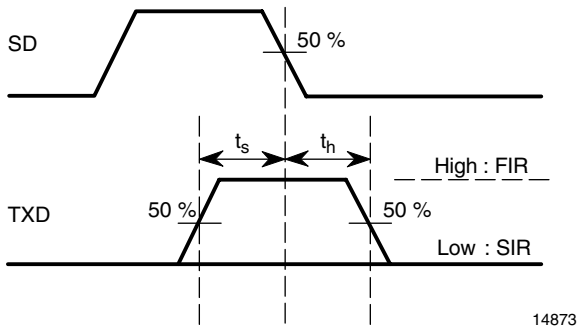


Figure 2. Mode Switching Timing Diagram

Table 2.
Truth table

Inputs			Outputs	
SD	TXD	Optical input Irradiance mW/m^2	RXD	Transmitter
high	x	x	weakly pulled (500 kΩ) to V_{CC1}	0
low	high	x	low (active)	I_e
	high > 80 µs	x	high	0
	low	< 4	high	0
	low	> Min. irradiance*Ee* < Max. irradiance *Ee*	low (active)	0
	low	> Max. irradiance *Ee*	x	0

Recommended Solder Profiles for TFDU6102

Solder Profile for Sn/Pb Soldering

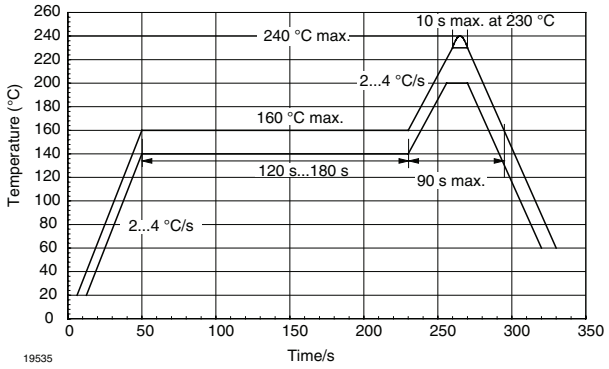


Figure 3. Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-Free, Recommended Solder Profile

The TFDU6102 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn (3.0 - 4.0) Ag (0.5 - 0.9) Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 4 and 5 are VISHAY's recommended profiles for use with the TFDU6102 transceivers. For more details please refer to the application note
“SMD Assembly Instructions”
(http://www.vishay.com/docs/82602/82602.pdf).

A ramp-up rate less than 0.9 °C/s is not recommended. Ramp-up rates faster than 1.3 °C/s could damage an optical part because the thermal conductivity is less than compared to a standard IC.

Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all VISHAY transceivers (TFDUxxxx and TFBSxxx) are equivalent to MSL4.
The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing"
(http://www.vishay.com/docs/82601/82601.pdf).

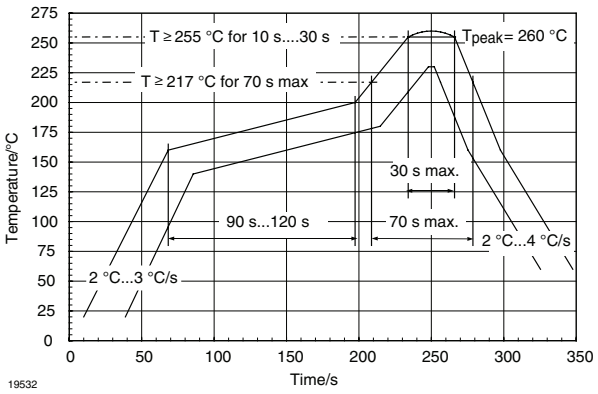


Figure 4. Solder Profile, RSS Recommendation

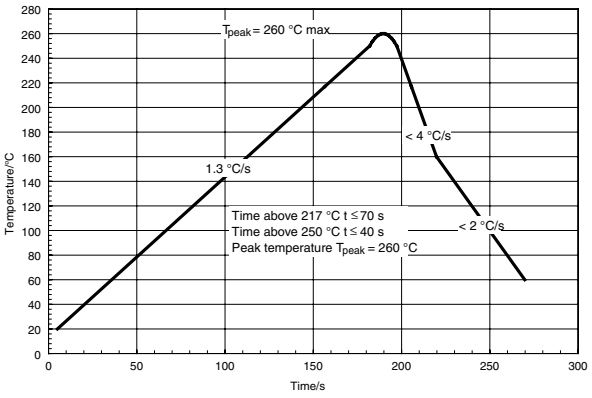


Figure 5. RTS Recommendation

Current Derating Diagram

Figure 5 shows the maximum operating temperature when the device is operated without external current limiting resistor. A power dissipating resistor of 2 Ω is recommended from the cathode of the IRED to Ground for supply voltages above 4 V. In that case the device can be operated up to 85 °C, too.

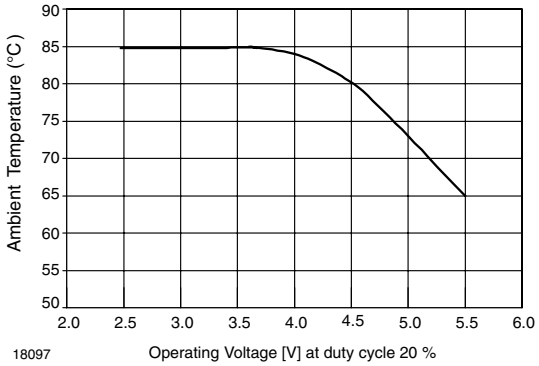


Figure 6. Temperature Derating Diagram

Package Dimensions

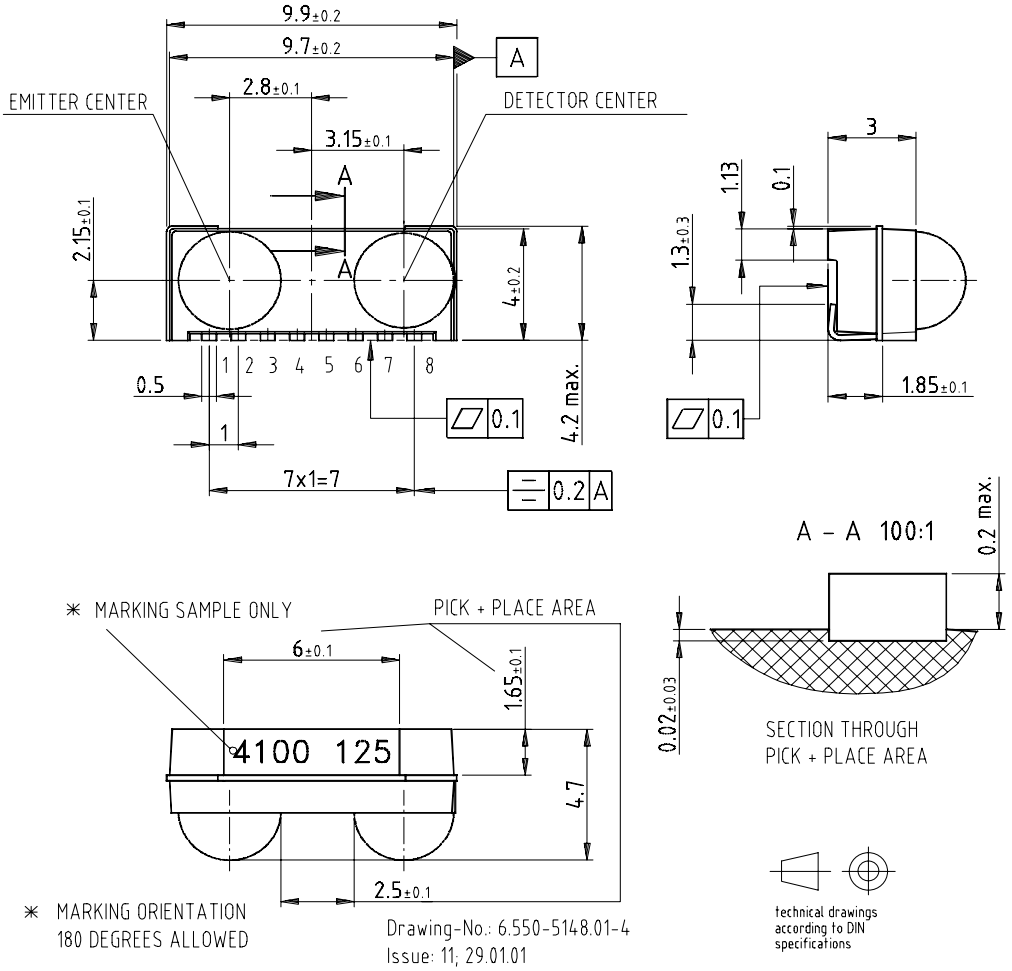


Figure 7. Package drawing TFDU6102, dimensions in mm, tolerance ± 0.2 mm if not otherwise mentioned

Solder Footprint

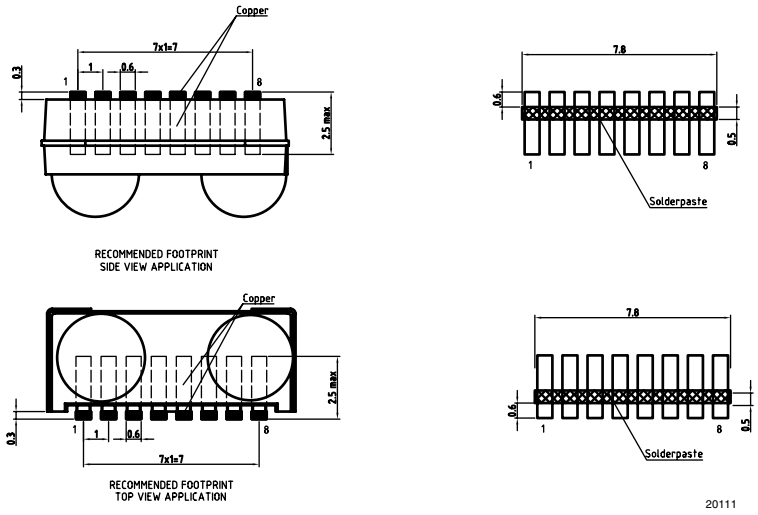
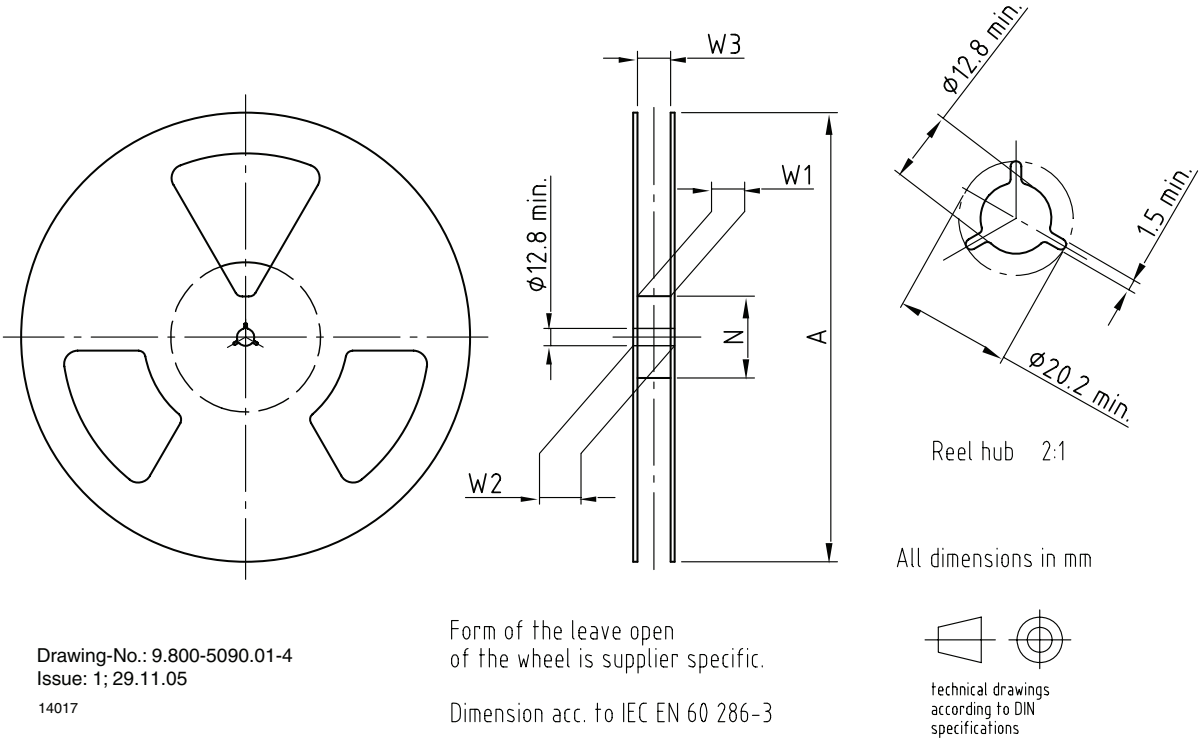


Figure 8. Solder footprint for top and side view mounting TFDU6102, dimensions in mm, tolerance ± 0.2 mm if not otherwise mentioned

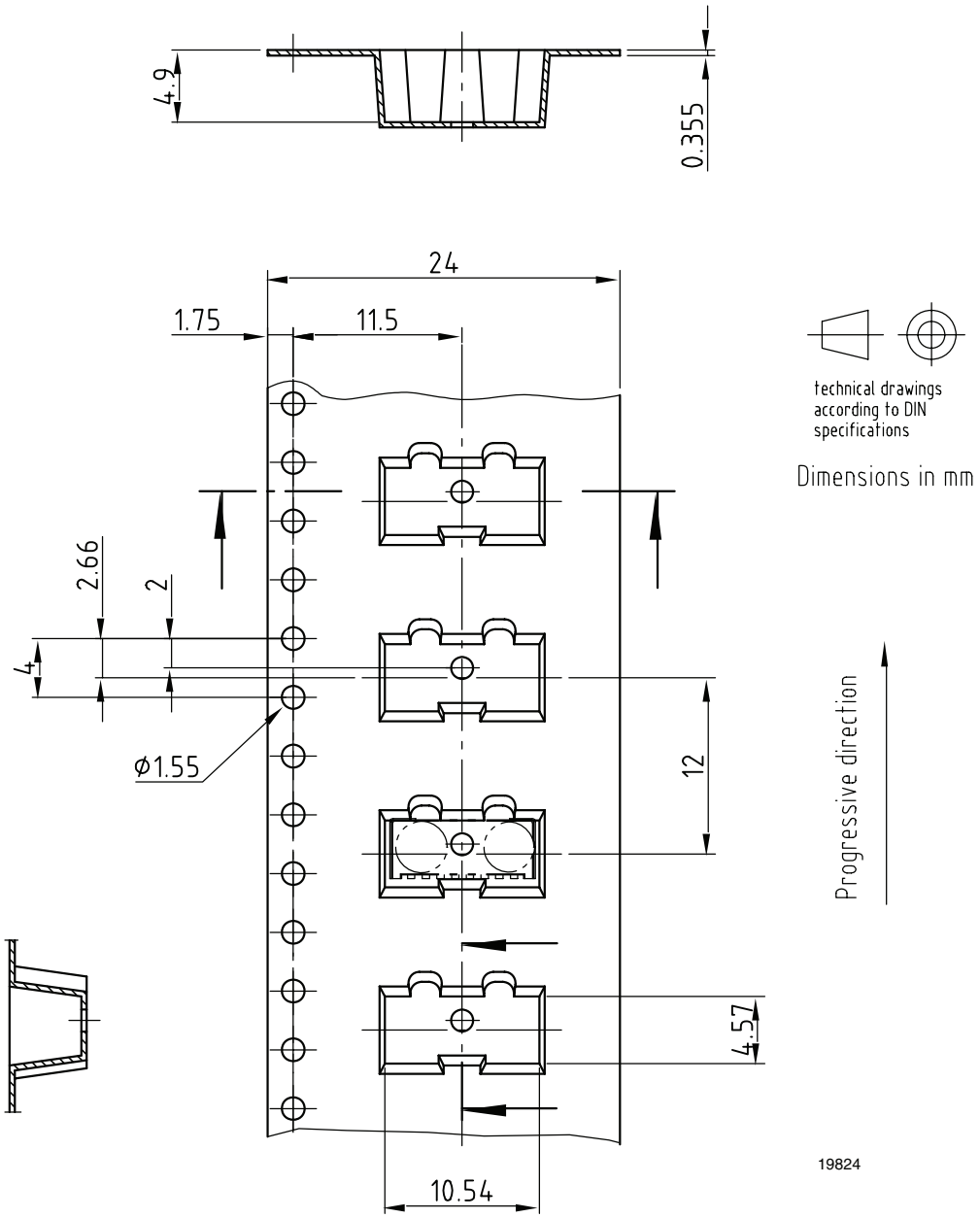
Reel Dimensions



Tape Width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
24	330	60	24.4	30.4	23.9	27.4

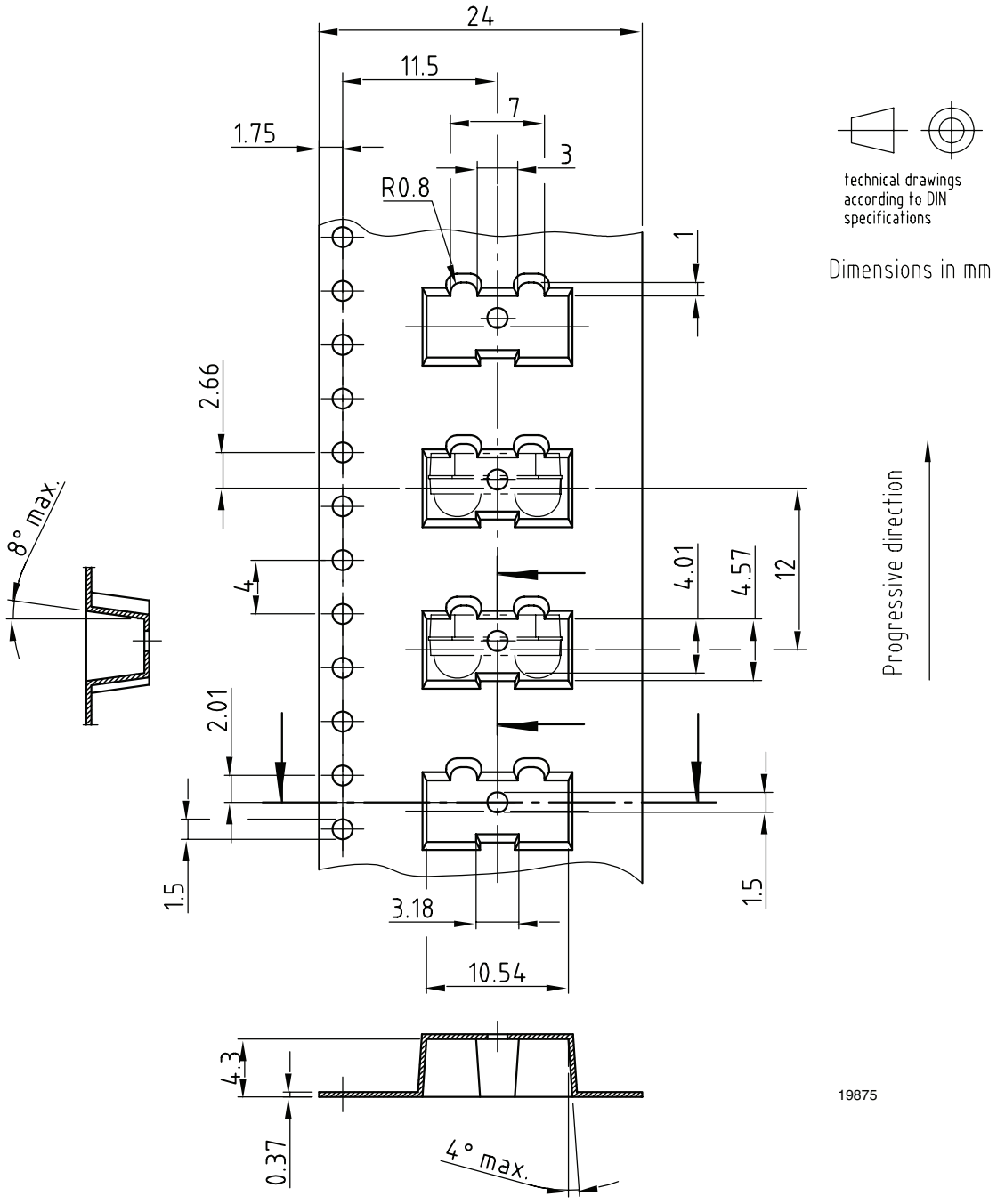
Figure 9. Reel dimensions [mm]

Tape Dimensions



Drawing-No.: 9.700-5251.01-4
Issue: 3; 02.09.05

Figure 10. Tape drawing, TFDU6102 for top view mounting, tolerance ± 0.1 mm



Drawing-No.: 9.700-5297.01-4
Issue: 1; 04.08.05

Figure 11. Tape drawing, TFDU6102 for side view mounting, tolerance ± 0.1 mm

Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany

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All product specifications and data are subject to change without notice.

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