

Product Brief

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Features

CSI-2 TX/RX Interface

- MIPI CSI-2 compliant (Version 1.01 Revision 0.04 — 2 April 2009)
- Configurable to TX or RX controller
- Supports up to 1 Gbps per data lane
- Supports up to 4 data lanes
- Supports the following video data formats
 - For CSI RX configuration: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and user-defined 8-bit
 - For CSI TX configuration: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14

Parallel Port Interface

- Supports the following video data formats
 - 24-bit bus — un-packed format (Both input and output mode)
 - RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.
 - YUV444 (for parallel input mode only)
 - YUV422 8-bit — ITU BT.656 and ITU BT.601 (for parallel input mode only)
- Up to 100 MHz PCLK frequency for output mode, and 154 MHz for input mode

I²C Slave Interface

- Support for normal (100KHz), fast mode (400 KHz) and special mode (1 MHz)
- Can be used to configure all TC358746 internal registers

GPIO signals

- 3 GPIO signals can be configured as control signals

System

- Clock and power management support to achieve low-power states.
- Chip Select (CS) input signal to allow multiple TC358746 chips on the same system

Power supply inputs

- Core and MIPI D-PHY: 1.2V
- I/O: 1.8V – 3.3V

Package

- TC358746XBG:
72-pin, 4.5 mm x 4.5 mm, 0.40 mm ball pitch, 1.0 mm height

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