# Contents

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 60 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25°C | 4 | A |
| $I_D$ | Drain current (continuous) at $T_C$=100°C | 2.9 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 16 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25°C | 3.3 | W |
| | Derating factor | 0.026 | W/°C |
| dv/dt (2) | Peak diode recovery voltage slope | 10 | V/ns |
| $E_{AS}$ (3) | Single pulse avalanche energy | 200 | mJ |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -55 to 150 | °C |

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 4$ A, di/dt ≤150A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
3. Starting $T_j$ = 25 °C, $I_D$ = 4A, $V_{DD}$ = 30V

**Table 2. Thermal data**

| | | | |
|---|---|---|---|
| Rthj-pcb | Thermal resistance junction-PCB(1) max | 38 | °C/W |
| Rthj-pcb | Thermal resistance junction-PCB(2) max | 100 | °C/W |
| $T_l$ (3) | Maximum lead temperature for soldering purpose typ | 260 | °C |

1. When Mounted on FR-4 board with 1 inch$^2$ pad, 2 oz. of Cu. and t < 10 sec.
2. When Mounted on minimum recommended footprint
3. for 10 sec. 1.6 mm from case

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 3. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 µA, $V_{GS}$= 0 | 60 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating,<br>$V_{DS}$ = Max rating @125°C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±20V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10V, $I_D$= 1.5A | | 0.07 | 0.10 | Ω |

**Table 4. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$= 15V, $I_D$=1.5A | | 3 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ =25V, f=1 MHz, $V_{GS}$=0 | | 315<br>70<br>30 | | pF<br>pF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$=48V, $I_D$ = 3A<br>$V_{GS}$ =10V<br>(see Figure 14) | | 10<br>3.5<br>3.5 | 13 | nC<br>nC<br>nC |

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

**Table 5. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on delay time<br>rise time | $V_{DD}$=30 V, $I_D$=1.5A,<br>$R_G$=4.7Ω, $V_{GS}$=10V<br>(see Figure 13) | | 7<br>18 | | ns<br>ns |
| $t_{d(off)}$<br>$t_f$ | Turn-off delay time<br>fall time | $V_{DD}$=30 V, $I_D$=1.5A,<br>$R_G$=4.7Ω, $V_{GS}$=10V<br>(see Figure 13) | | 17<br>6 | | ns<br>ns |

**Table 6. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 4 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | | | 16 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$=4A, $V_{GS}$=0 | | | 1.3 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$=4 A,<br>di/dt = 100A/µs,<br>$V_{DD}$=25 V, Tj=150°C<br>(see Figure 15) | | 50<br>88<br>3.5 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

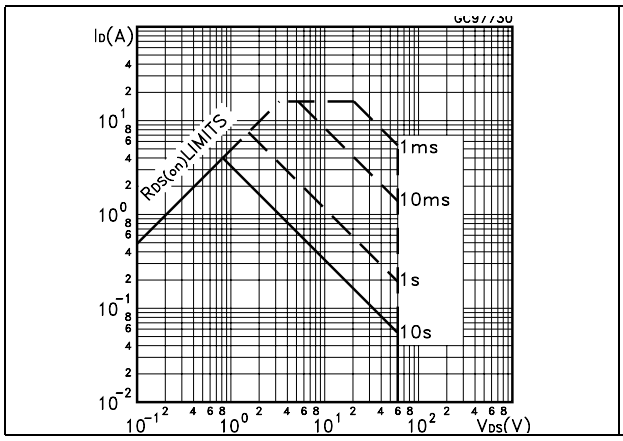



**Figure 2. Thermal impedance**

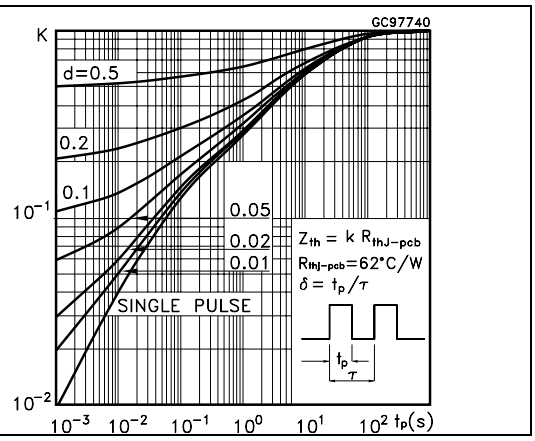



**Figure 3. Output characteristics**

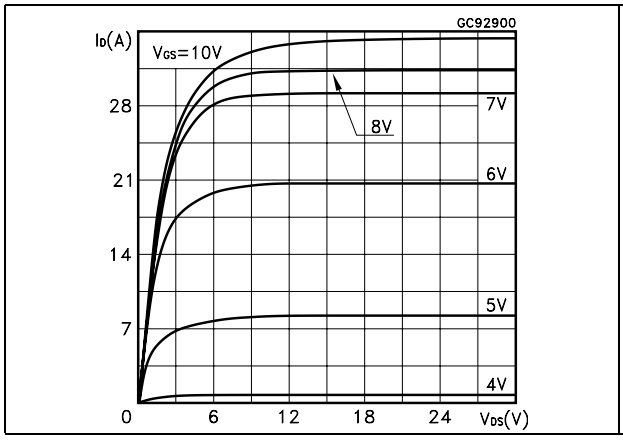



**Figure 4. Transfer characteristics**

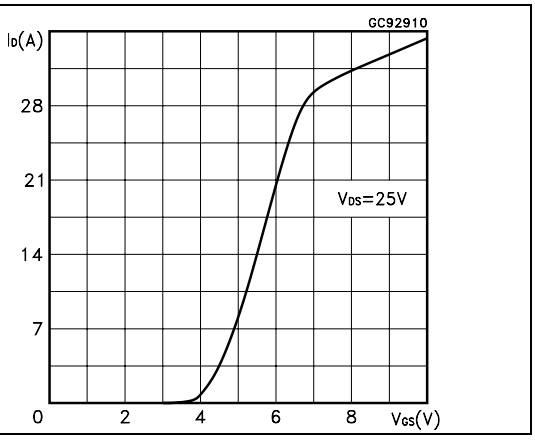



**Figure 5. Transconductance**

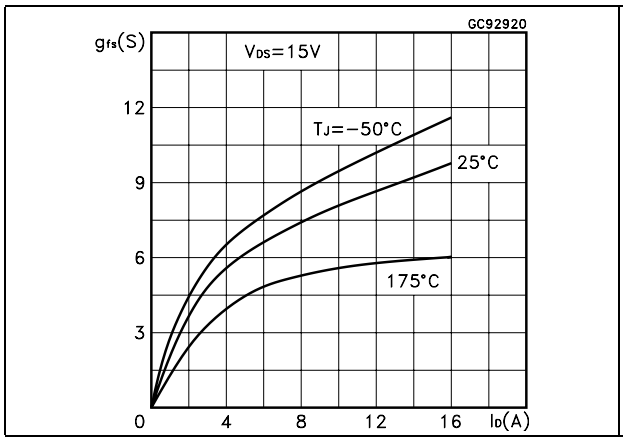



**Figure 6. Static drain-source on resistance**

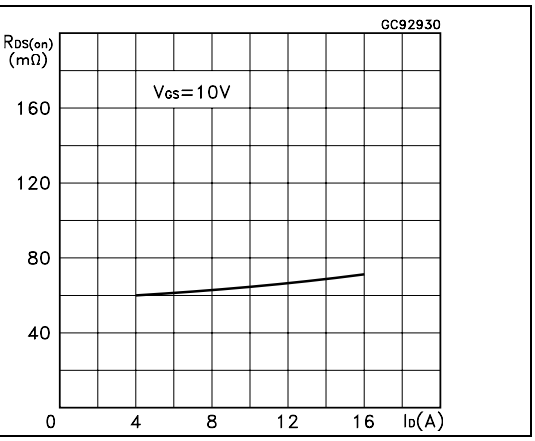


**Figure 7. Gate charge vs. gate-source voltage**

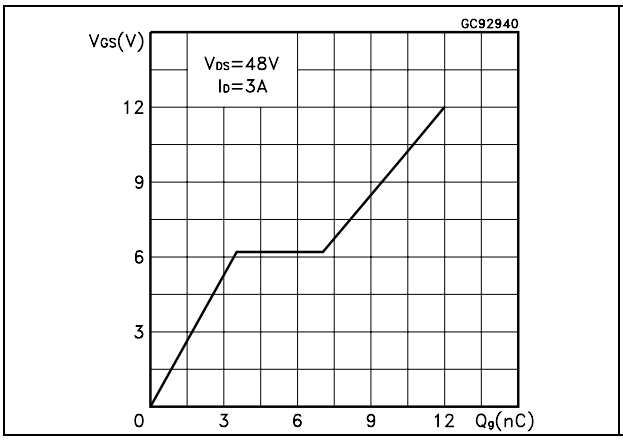



**Figure 8. Capacitance variations**

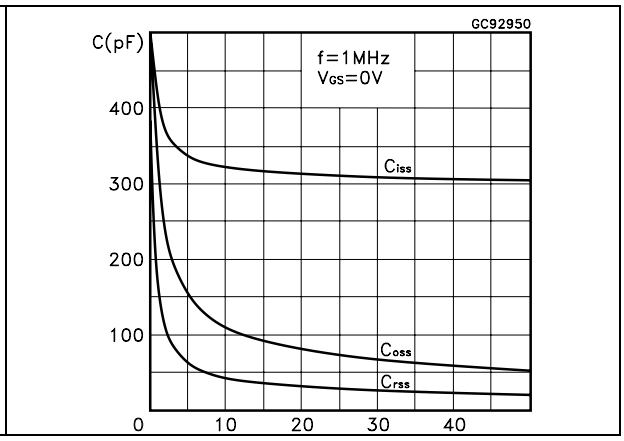



**Figure 9. Normalized gate threshold voltage vs. temperature**

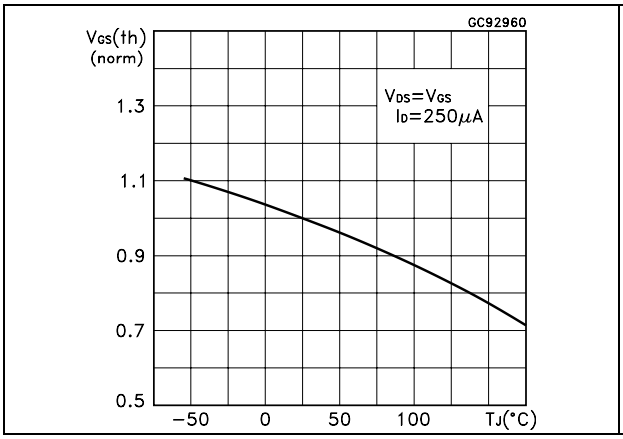



**Figure 10. Normalized on resistance vs. temperature**

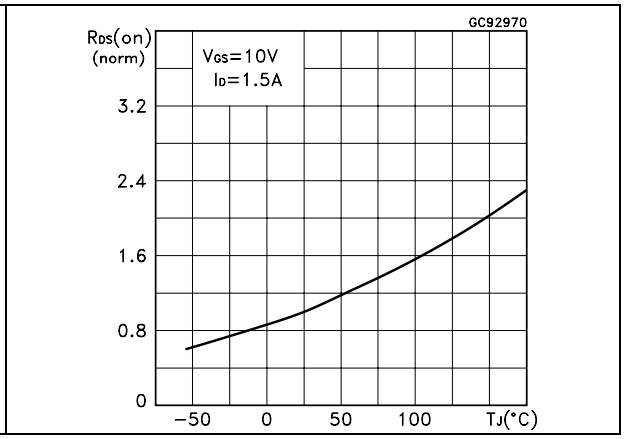



**Figure 11. Source-drain diode forward characteristics**

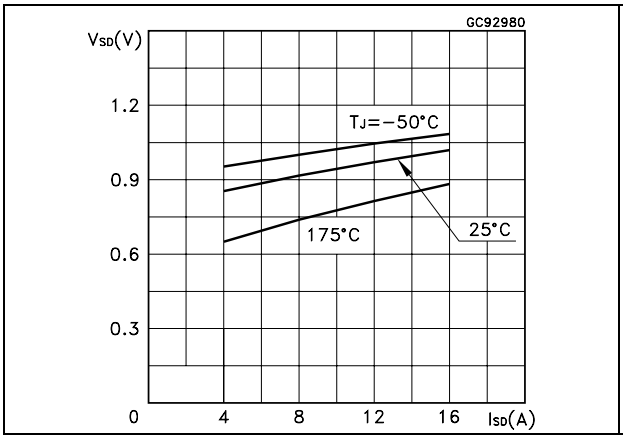
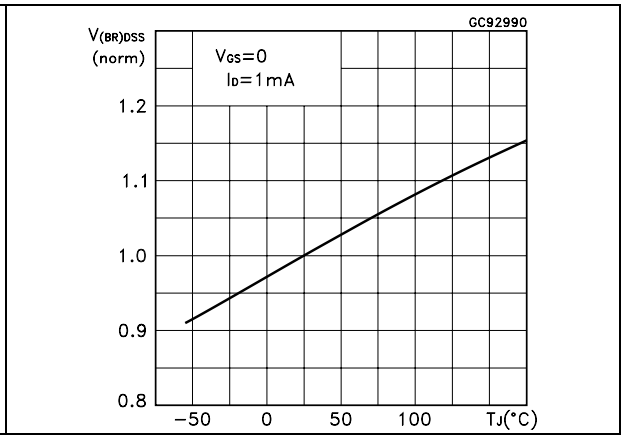



**Figure 12. Normalized breakdown voltage vs. temperature**



# 3 Test circuit

**Figure 13. Switching times test circuit for resistive load**

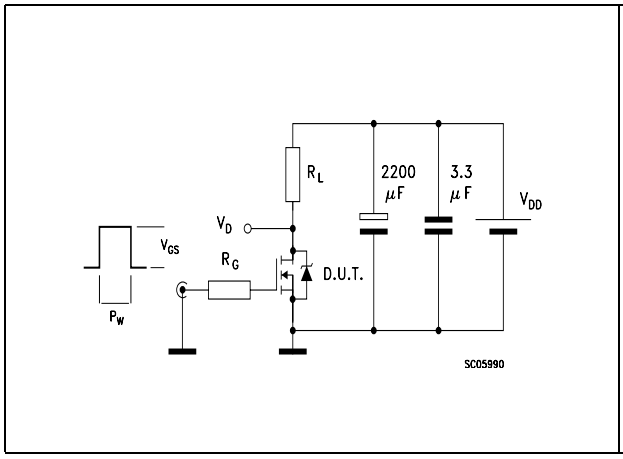



**Figure 14. Gate charge test circuit**

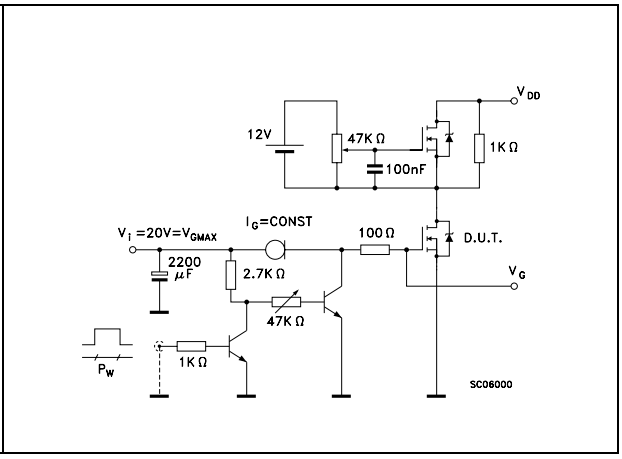



**Figure 15. Test circuit for inductive load switching and diode recovery times**

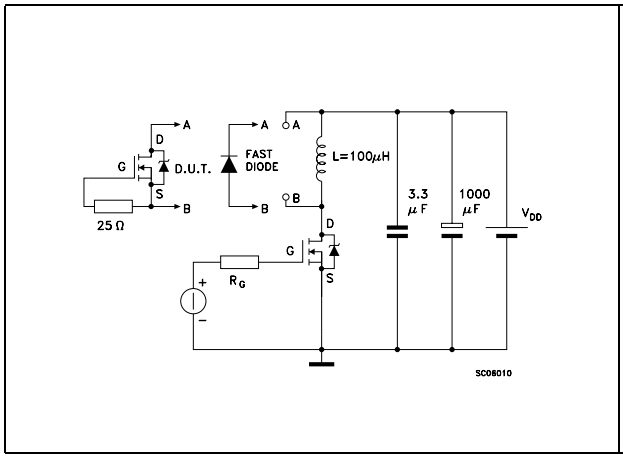



**Figure 16. Unclamped Inductive load test circuit**

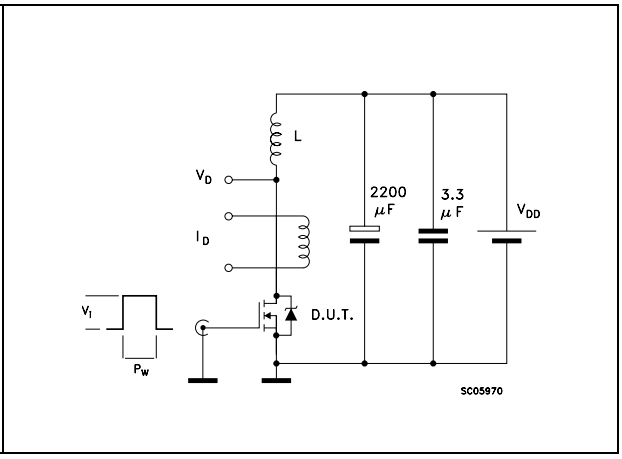



**Figure 17. Unclamped inductive waveform**

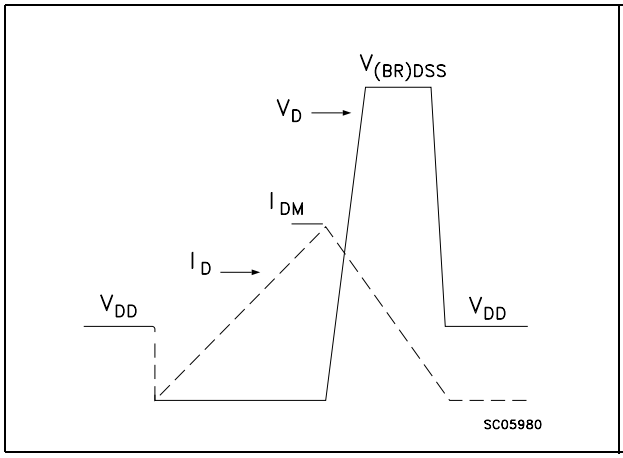
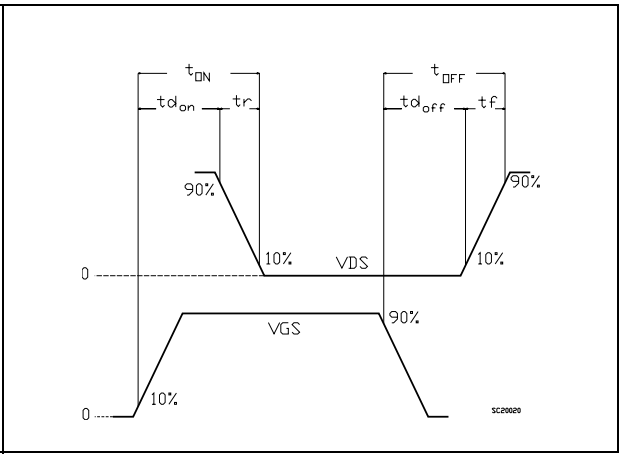



**Figure 18. Switching time waveform**

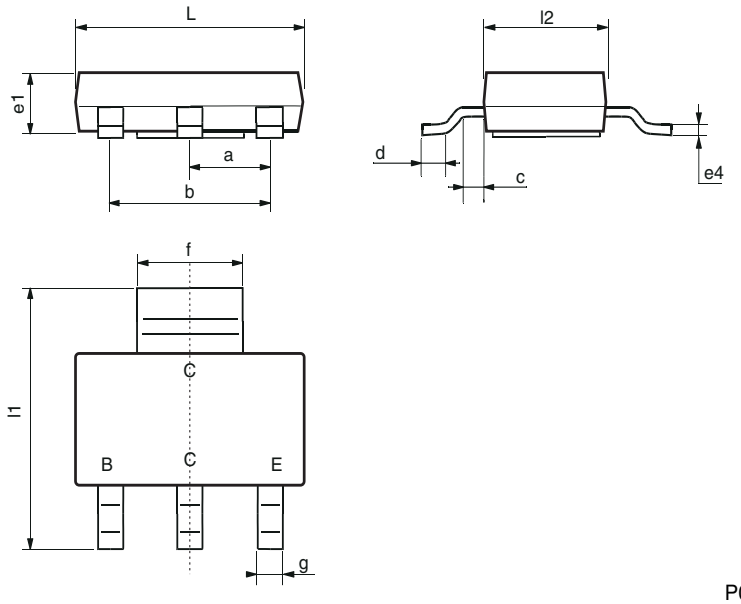


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

## SOT-223 MECHANICAL DATA

| DIM. | mm | | | mils | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a | 2.27 | 2.3 | 2.33 | 89.4 | 90.6 | 91.7 |
| b | 4.57 | 4.6 | 4.63 | 179.9 | 181.1 | 182.3 |
| c | 0.2 | 0.4 | 0.6 | 7.9 | 15.7 | 23.6 |
| d | 0.63 | 0.65 | 0.67 | 24.8 | 25.6 | 26.4 |
| e1 | 1.5 | 1.6 | 1.7 | 59.1 | 63 | 66.9 |
| e4 | | | 0.32 | | | 12.6 |
| f | 2.9 | 3 | 3.1 | 114.2 | 118.1 | 122.1 |
| g | 0.67 | 0.7 | 0.73 | 26.4 | 27.6 | 28.7 |
| l1 | 6.7 | 7 | 7.3 | 263.8 | 275.6 | 287.4 |
| l2 | 3.5 | 3.5 | 3.7 | 137.8 | 137.8 | 145.7 |
| L | 6.3 | 6.5 | 6.7 | 248 | 255.9 | 263.8 |




P008B

# 5 Revision history

**Table 7. Revision history**

| Date | Revision | Changes |
|---|---|---|
| 21-Jun-2004 | 4 | Complete datasheet |
| 04-Oct-2006 | 5 | The document has been reformatted |
| 01-Feb-2007 | 6 | Typo mistake on *Table 1*. |

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