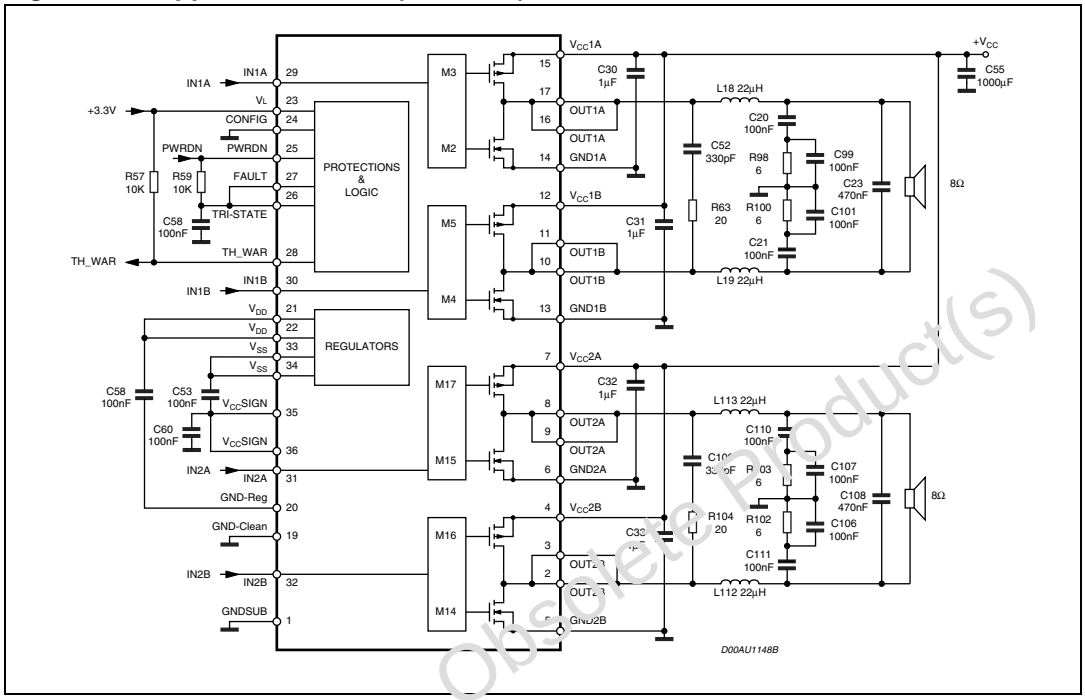
1 Introduction

Figure 1. Application circuit (dual BTL)



2 Pin description

Figure 2. Pin out

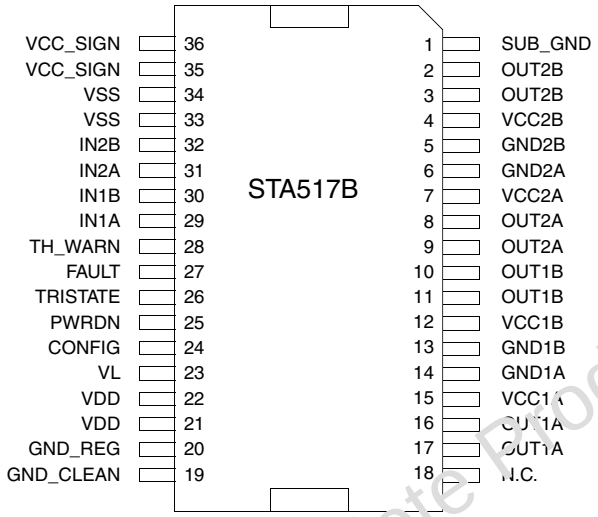


Table 2. Pin function

Pin	Name	Type	Description
1	GND_SUB	PWR	Substrate ground
2, 3	OUT2B	O	Output half bridge 2B
4	VCC2B	PWR	Positive supply
5	GND2B	PWR	Negative supply
6	GND2A	PWR	Negative supply
7	VCC2A	PWR	Positive supply
8, 9	OUT2A	O	Output half bridge 2A
10, 11	OUT1B	O	Output half bridge 1B
12	VCC1B	PWR	Positive supply
13	GND1B	PWR	Negative supply
14	GND1A	PWR	Negative supply
15	VCC1A	PWR	Positive supply
16, 17	OUT1A	O	Output half bridge 1A
18	N.C.	-	No internal connection
19	GND_CLEAN	PWR	Logical ground
20	GND_REG	PWR	Ground for regulator V_{DD}
21, 22	VDD	PWR	5-V regulator referred to ground
23	VL	PWR	High logical state setting voltage, V_L

Table 2. Pin function (continued)

Pin	Name	Type	Description
24	CONFIG	I	Configuration pin: 0: normal operation 1: bridges in parallel (OUT1A = OUT1B, OUT2A = OUT2B (If IN1A = IN1B, IN2A = IN2B))
25	PWRDN	I	Standby pin: 0: low-power mode 1: normal operation
26	TRISTATE	I	Hi-Z pin: 0: all power amplifier outputs in high impedance state 1: normal operation
27	FAULT	O	Fault pin advisor (open-drain device, needs pull-up resistor): 0: fault detected (short circuit or thermal, for example) 1: normal operation
28	TH_WARN	O	Thermal warning advisor (open-drain device, needs pull-up resistor): 0: temperature of the IC >120 °C 1: normal operation
29	IN1A	I	Input of half bridge 1A
30	IN1B	I	Input of half bridge 1B
31	IN2A	I	Input of half bridge 2A
32	IN2B	I	Input of half bridge 2B
33, 34	VSS	PWR	5-V regulator referred to $+V_{CC}$
35, 36	VCC_SIGN	PWR	Signal positive supply

3 Electrical characteristics

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC_MAX}	DC supply voltage (pins 4, 7, 12, 15)	60	V
V_{max}	Maximum voltage on pins 23 to 32	5.5	V
T_{j_MAX}	Operating junction temperature	0 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

Warning: **Stresses beyond those listed under "Absolute maximum ratings" make cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating condition" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supply with nominal value rated inside recommended operating conditions, may experience some rising beyond the maximum operating condition for short time when no or very low current is sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum rating is not exceeded.**

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)	-	1	2.5	°C/W
T_{jSD}	Thermal shut-down junction temperature	-	150	-	°C
T_{warn}	Thermal warning temperature	-	130	-	°C
t_{hSD}	Thermal shut-down hysteresis	-	25	-	°C

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage for pins PVCCA, PVCCB	10	-	56	V
T_{amb}	Ambient operating temperature	0	-	70	°C

Unless otherwise stated, the test conditions for *Table 6* below are V_L = 3.3 V, V_{CC} = 50 V and T_{amb} = 25 °C

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{dsON}	Power P-channel/N-channel MOSFET R_{dsON}	I_{dd} = 1 A	-	200	240	mΩ
I_{dss}	Power P-channel/N-channel leakage Idss	-	-	-	100	µA
g_N	Power P-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
g_P	Power N-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
Dt_s	Low current dead time (static)	see *Figure 3*	-	10	20	ns
Dt_d	High current dead time (dynamic)	L = 22 µH, C = 470 nF R_L = 8 Ω, I_{dd} = 4.5 A see *Figure 4*	-		50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load	-	-	100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load	-	-	100	ns
t_r	Rise time	Resistive load see *Figure 3*	-	-	25	ns
t_f	Fall time	Resistive load see *Figure 3*	-	-	25	ns
$V_{IN-High}$	High level input voltage	-	-	-	V_L / 2 + 300 mV	V
V_{IN-Low}	Low level input voltage	-	V_L / 2 - 300 mV	-	-	V
I_{IN-H}	High level input current	V_{IN} = V_L	-	1	-	µA
I_{IN-L}	Low level input current	V_{IN} = 0.3 V	-	1	-	µA
$I_{PWRDN-H}$	High level PWRDN pin input current	V_L = 3.3 V	-	35	-	µA
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3 V	0.8	-		V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3 V		-	1.7	V
$I_{VCC-PWRDN}$	Supply current from V_{CC} in power down	V_{PWRDN} = 0 V	-	-	3	mA
I_{FAULT}	Output current on pins FAULT, TH_WARN with fault condition	V_{pin} = 3.3 V	-	1	-	mA
$I_{VCC-HiZ}$	Supply current from V_{CC} in tristate	$V_{TRISTATE}$ = 0 V	-	22	-	mA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{VCC}	Supply current from V_{CC} in operation, both channels switching)	Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters	-	70	-	mA
I_{OCP}	Overcurrent protection threshold Isc (short-circuit current limit) (1)	-	6.5	8	10	A
V_{UVP}	Undervoltage protection threshold	-	-	7	-	V
V_{OVP}	Overvoltage protection threshold	-	60	-	70	V
t_{pw_min}	Output minimum pulse width	No load	25	-	40	ns

1. See specific application note number: AN1994

Table 7. Threshold switching voltage variation with voltage on pin VL

Voltage on pin VL, V_L	V_{LOW} max	V_{HIGH} min	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5.0	0.85	1.85	V

Table 8. Logic truth table

Pin TRISTATE	Inputs as per *Figure 4*		Transistors as per *Figure 4*				Output mode
	INxA	INxB	Q1	Q2	Q3	Q4	
0	x	x	Off	Off	Off	Off	Hi Z
1	0	0	Off	Off	On	On	Dump
1	0	1	Off	On	On	Off	Negative
1	1	0	On	Off	Off	On	Positive
1	1	1	On	On	Off	Off	Not used

3.1 Test circuits

Figure 3. Test circuit

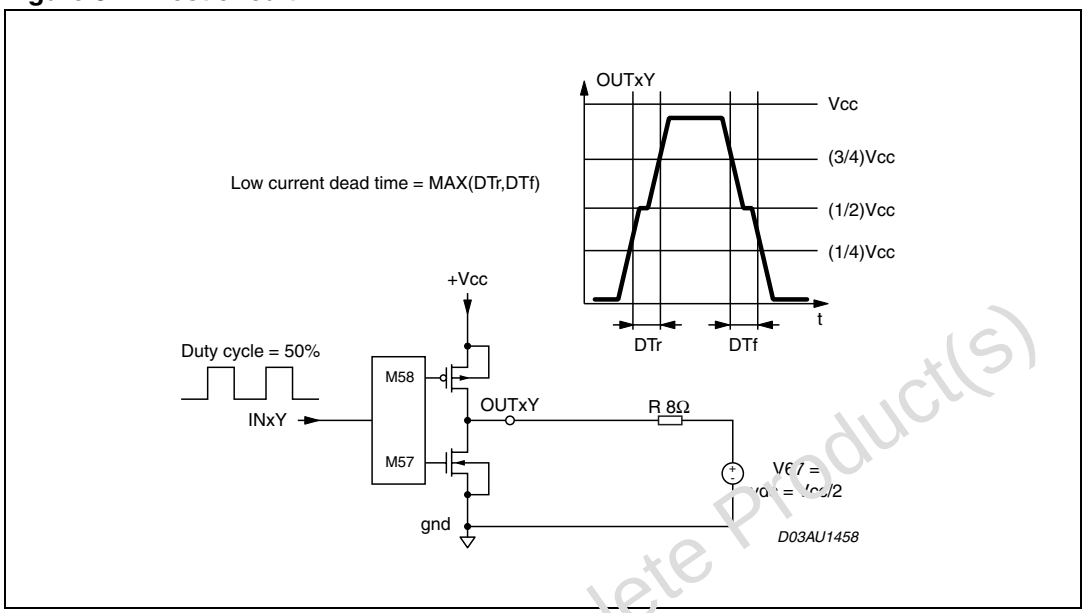
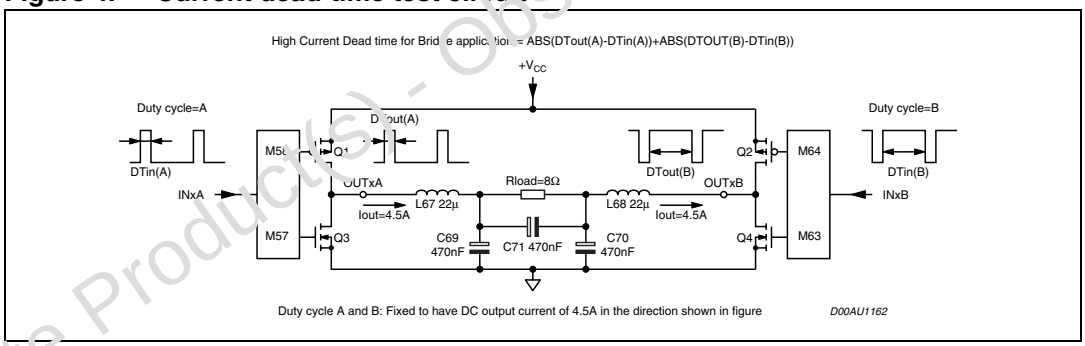


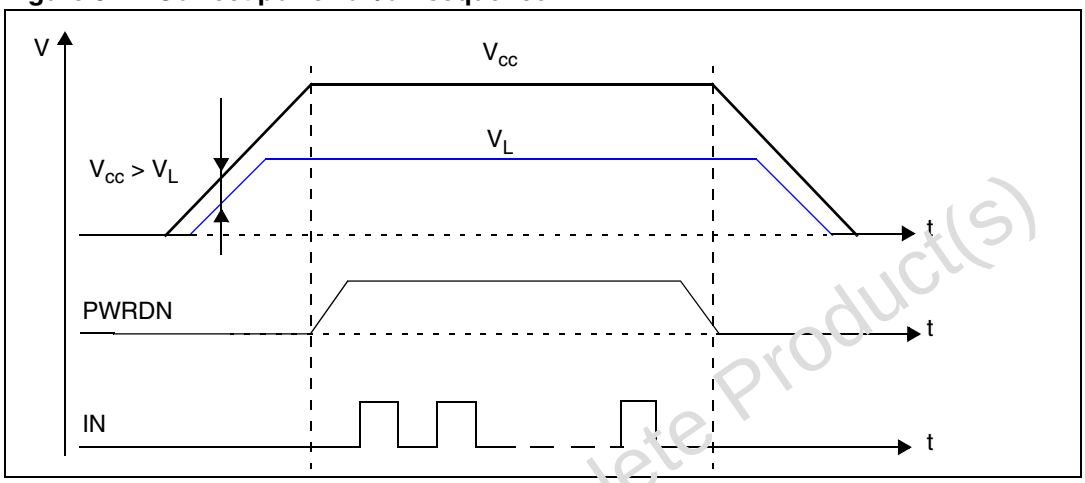
Figure 4. Current dead-time test circuit



4 Power supply and control sequencing

To guarantee correct operation and reliability, the recommended power-on/off sequence as shown in *Figure 5* must be followed

Figure 5. Correct power-on/off sequence



V_{CC} must turn on before V_L. This prevents uncontrolled current flowing through the internal protection diode connected between V_I (logic supply) and V_{CC} (high power supply). which could result in damage to the device.

PWRDN must be released after V_L is switched on. An input signal can then be sent to the power stage.

5 Applications

Figure 6 below shows a single-BLT configuration capable of giving 360 W into a 4-Ω load at 10% THD with V_{CC} = 55 V. This result was obtained using the STA30X+STA50X demo board. Note that a PWM modulator as driver is required.

Figure 6. Typical single-BTL configuration for 360 W

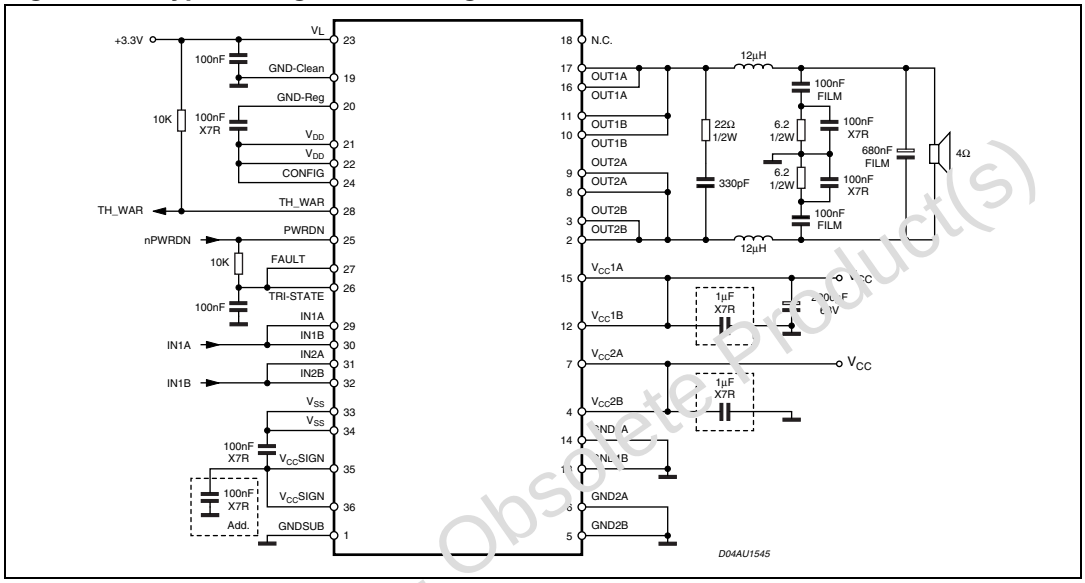
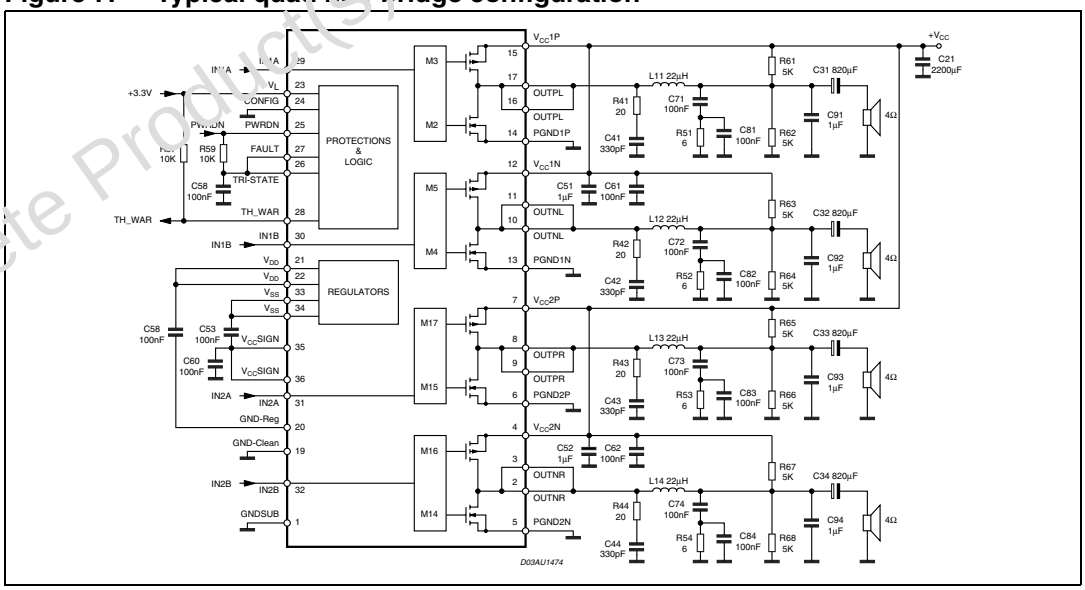


Figure 7. Typical quad half-bridge configuration



For more information, refer to the application note AN1994.

6 Package mechanical data

Figure 8. PowerSO36 exposed pad up outline drawing

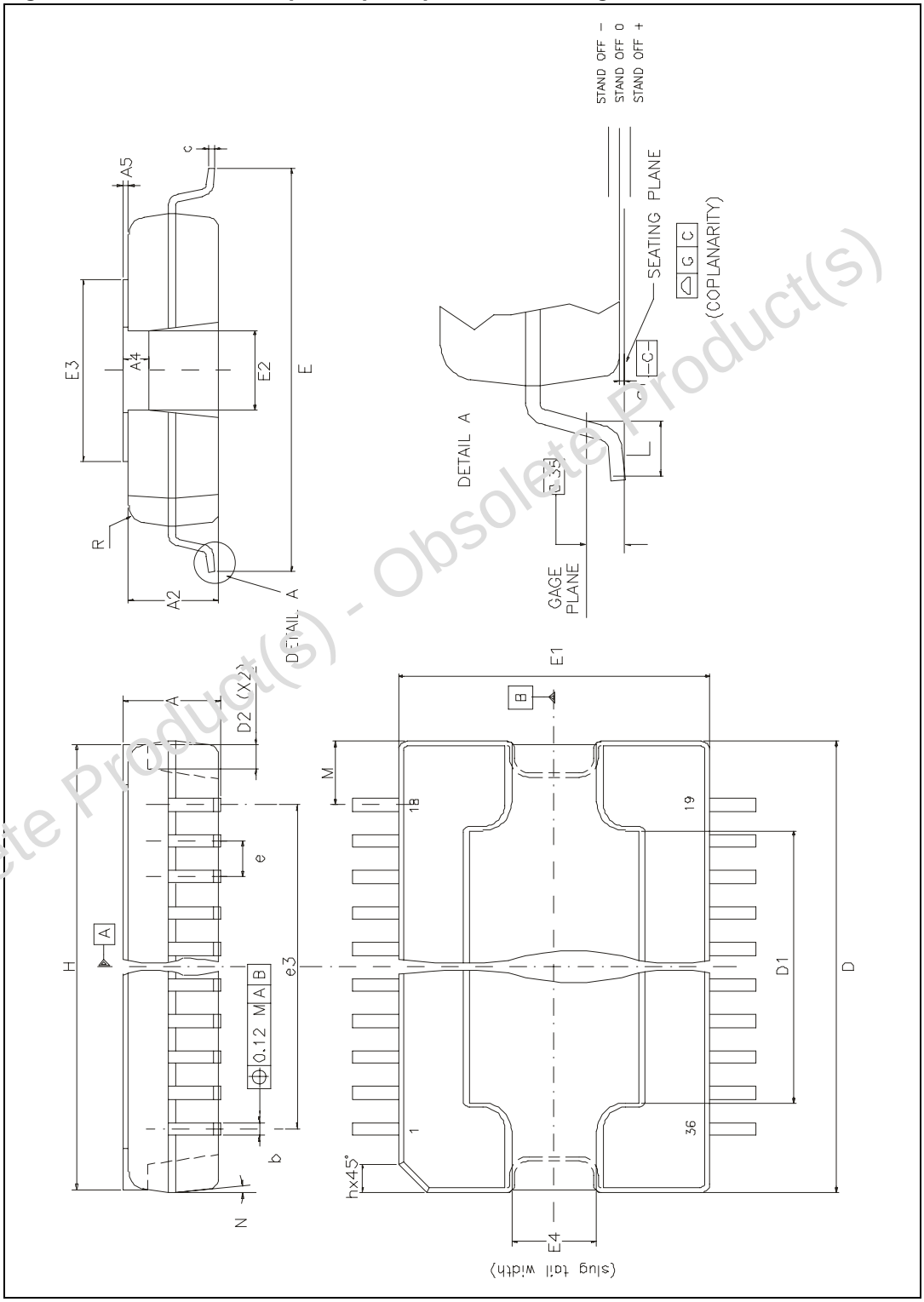


Table 9. PowerSO36 exposed pad up dimensions

Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	3.25	-	3.43	0.128	-	0.135
A2	3.10	-	3.20	0.122	-	0.126
A4	0.80	-	1.00	0.031	-	0.039
A5	-	0.20	-	-	0.008	-
a1	0.03	-	-0.04	0.001	-	-0.002
b	0.22	-	0.38	0.009	-	0.015
c	0.23	-	0.32	0.009	-	0.013
D	15.80	-	16.00	0.622	-	0.630
D1	9.40	-	9.80	0.370	-	0.386
D2	-	1.00	-	-	0.039	-
E	13.90	-	14.50	0.547	-	0.571
E1	10.90	-	11.10	0.429	-	0.437
E2	-	-	2.90	-	-	0.114
E3	5.80	-	6.20	0.228	-	0.244
E4	2.90	-	3.20	0.114	-	0.126
e	-	0.65	-	-	0.026	-
e3	-	11.05	-	-	0.435	-
G	0	-	0.08	0	-	0.003
H	15.50	-	15.90	0.610	-	0.626
h	-	-	1.10	-	-	0.043
L	0.80	-	1.10	0.031	-	0.043
M	2.25	-	2.60	0.089	-	0.102
N	-	-	10 degrees	-	-	10 degrees
R	-	0.6	-	-	0.024	-
s	-	-	8 degrees	-	-	8 degrees

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7 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Feb-2007	1	Initial release.
19-Mar-2007	2	Update to reflect product maturity.
11-Aug-2009	3	Updated section Description on cover page.
21-Jan-2010	4	Updated title to 6.5 A on cover page Updated text and figure caption in *Chapter 5: Applications on page 10*.

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