ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 40V
Logic Inputs ..... -0.3V to 5.5V
Analog Inputs ..... -0.3V to V_{IN}
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Operating Junction Temperature
  Hermetic (J, L Packages) ..... 150°C
  Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C
RoHS Peak Package Solder Reflow Temp. (40 sec. max. exp.)..... 260°C (+0, -5)

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DATA

J Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 25°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 70°C/W
N Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 30°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 60°C/W
DW Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 90°C/W
L Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 120°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ..... 8V to 35V
Collector Supply Voltage ..... 4.5V to 35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 350KHz
Oscillator Timing Resistor ..... 2KΩ to 150KΩ
Oscillator Timing Capacitor ..... 1nF to 20µF
Available Deadtime Range at 40KHz ..... 3% to 50%
Operating Ambient Temperature Range:
  SG1526 ..... -55°C to 125°C
  SG2526 ..... -25°C to 85°C
  SG3526 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1526 with -55°C ≤ T_A ≤ 125°C, SG2526 with -25°C ≤ T_A ≤ 85°C, SG3526 with 0°C ≤ T_A ≤ 70°C, and V_{IN} = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1526/2526			SG3526			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	V_{IN} = 8 to 35V		10	30		10	30	mV
Load Regulation	I_L = 0 to 20mA		10	30		10	50	mV
Temperature Stability (Note 9)	Over Operating T_J		15	50		15	50	mV
Total Output Voltage Range (Note 9)	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V		50	125		50	125	mA
Undervoltage Lockout Section								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		V

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	SG1526/2526			SG3526			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C		±3	±8		±3	±8	%
Voltage Stability	V_{IN} = 8 to 35V		0.5	1.0		0.5	1.0	%
Temperature Stability (Note 9)	Over Operating T_J		7	10		5	10	%
Minimum Frequency (Note 9)	R_T = 150KΩ, C_T = 20µF			1.0			1.0	Hz
Maximum Frequency	R_T = 2KΩ, C_T = 1.0nF	350			350			KHz
Sawtooth Peak Voltage	V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 5)								
Input Offset Voltage	R_S ≤ 2KΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ, T_J = 25°C	64	72		60	72		dB
High Output Voltage	V_{PIN1} - V_{PIN2} ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
Low Output Voltage	V_{PIN2} - V_{PIN1} ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2KΩ	70	94		70	94		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	66	80		66	80		dB
PWM Comparator Section (Note 4)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = 0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = 3.6V	45	49		45	49		%
Digital Ports ($\overline{SYNC}$, $\overline{SHUTDOWN}$, and $\overline{RESET}$)								
HIGH Output Voltage	I_{SOURCE} = 40µA	2.4	4		2.4	4		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = 2.4V		-125	-300		-125	-300	µA
LOW Input Current	V_{IL} = 0.4V		-225	-500		-225	-500	µA
Current Limit Comparator Section (Note 6)								
Sense Voltage	R_S ≤ 50Ω, T_J = 25°C	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = 0.4V		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET}$ = 2.4V	50	100	200	50	100	200	µA
Output Drivers (each output) (Note 7)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2		1.2	2	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	µs
Power Consumption Section (Note 8)								
Standby Current	$\overline{SHUTDOWN}$ = 0.4V		18	30		18	30	mA

Note 3. I_L = 0mA
Note 4. F_{OSC} = 40KHz (R_T = 4.12KΩ ±1%, C_T = .01µF ±1%, R_D = 0Ω)
Note 5. V_{CM} = 0 to 5.2V
Note 6. V_{CM} = 0 to 12V
Note 7. V_C = 15V
Note 8. V_{IN} = 35V
Note 9. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

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CHARACTERISTIC CURVES

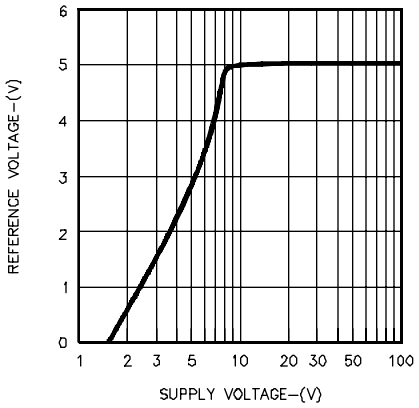

FIGURE 1.
REFERENCE VOLTAGE VS. SUPPLY VOLTAGE

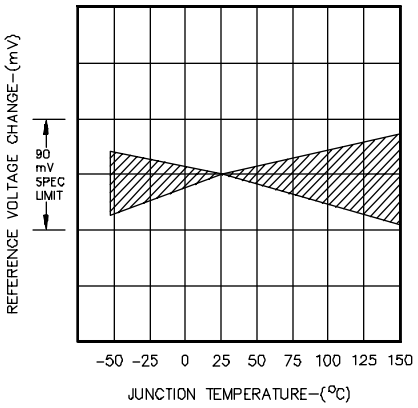

FIGURE 2.
REFERENCE TEMPERATURE STABILITY

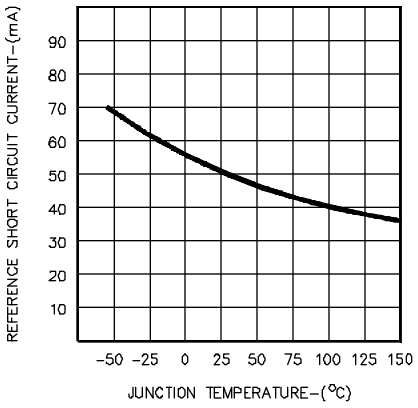

FIGURE 3.
REFERENCE SHORT CIRCUIT CURRENT

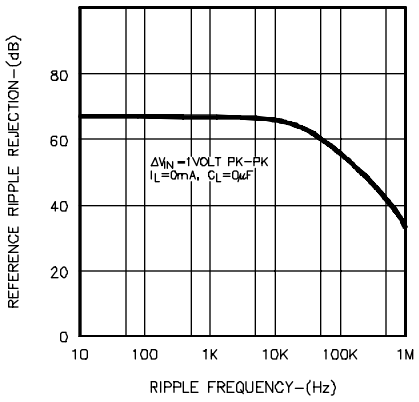

FIGURE 4.
REFERENCE RIPPLE REJECTION

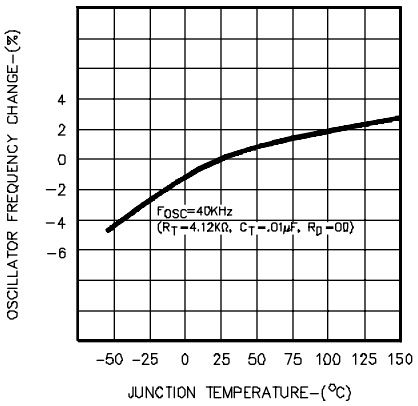

FIGURE 5.
OSCILLATOR FREQUENCY TEMPERATURE STABILITY

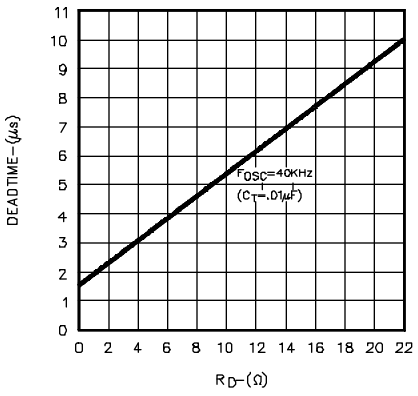

FIGURE 6.
OUTPUT DRIVER DEADTIME VS. R_D VALUE

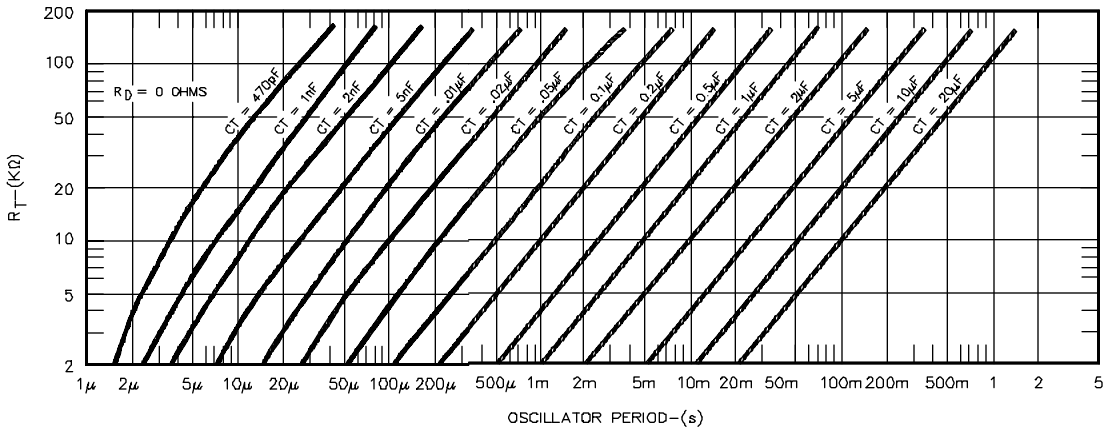

FIGURE 7.
OSCILLATOR PERIOD VS. R_T AND C_T

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CHARACTERISTIC CURVES (continued)

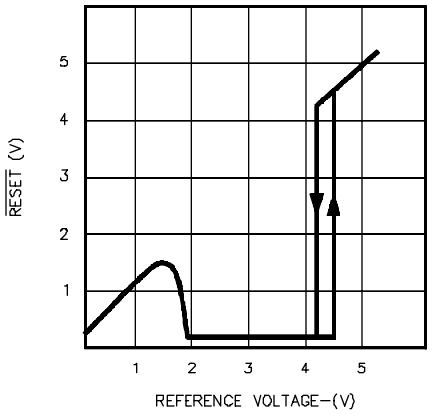

FIGURE 8.
UNDERVOLTAGE LOCKOUT CHARACTERISTIC

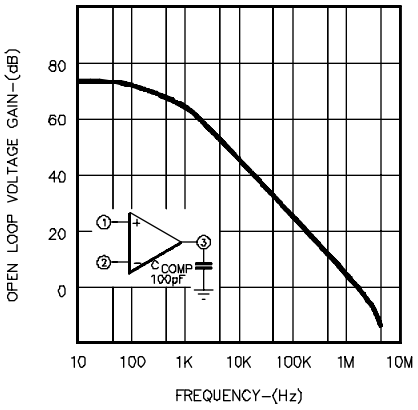

FIGURE 9.
ERROR AMPLIFIER OPEN LOOP GAIN
VS. FREQUENCY

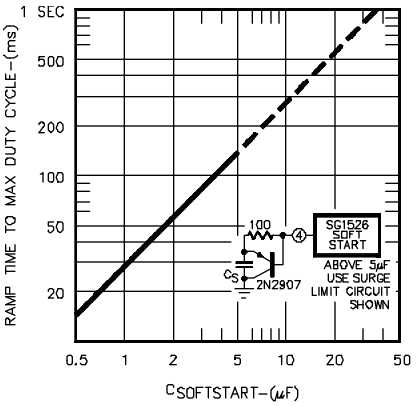

FIGURE 10.
SOFTSTART TIME CONSTANT VS. C_S

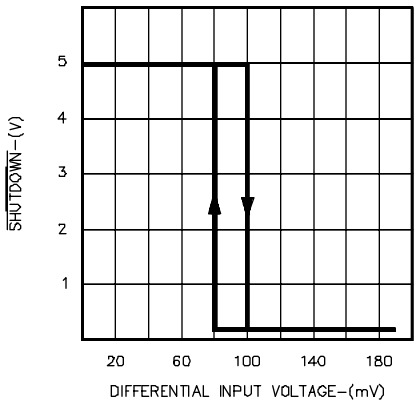

FIGURE 11.
CURRENT LIMIT TRANSFER FUNCTION

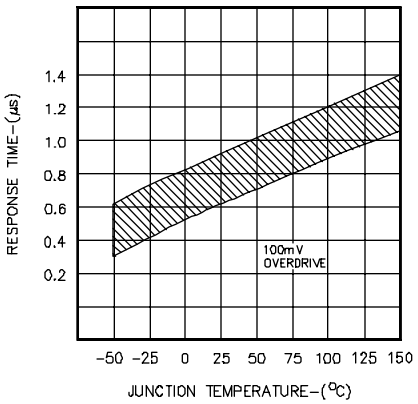

FIGURE 12.
COMPARATOR INPUT TO DRIVER OUTPUT DELAY

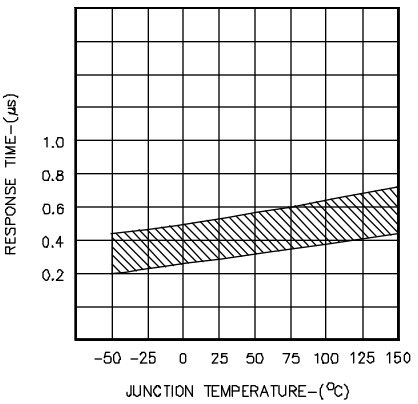

FIGURE 13.
SHUTDOWN INPUT TO DRIVER OUTPUT DELAY

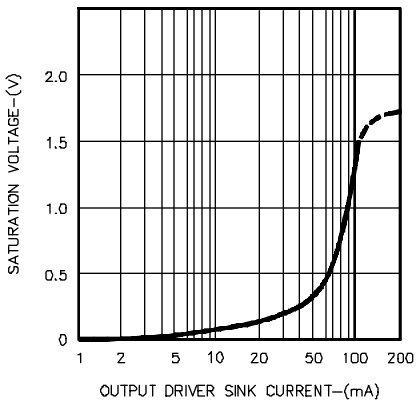

FIGURE 14.
OUTPUT DRIVER SATURATION VOLTAGE VS. I_{SINK}

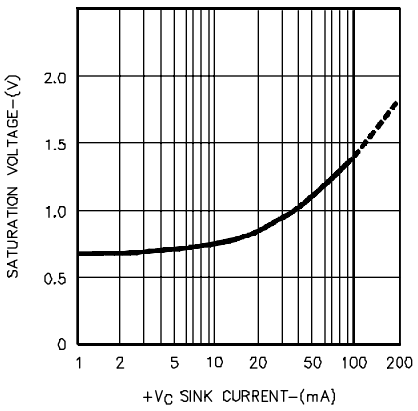

FIGURE 15.
OUTPUT SUPPLY SATURATION VOLTAGE VS. I_{SINK}

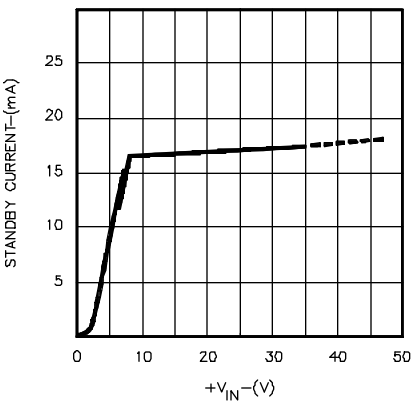

FIGURE 16.
STANDBY CURRENT VS. SUPPLY VOLTAGE

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APPLICATION INFORMATION

VOLTAGE REFERENCE

The reference regulator of the SG1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8 volts., and provides up to 20mA of load current to external circuitry at +5.0 volts. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

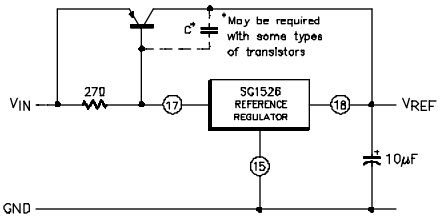

FIGURE 17.
EXTENDING REFERENCE OUTPUT CURRENT

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit protects the SG1526 and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2 volt bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$, or 1.8 volts at 25°C. When the reference voltage rises to approximately +4.4 volts, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2 volts, the undervoltage circuit pulls RESET $\overline{\text{LOW}}$ again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The SG1526 can operate from a +5 volt supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2 volts.

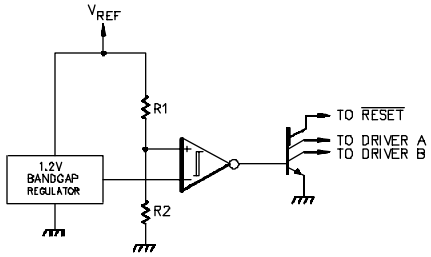

FIGURE 18.
SIMPLIFIED UNDERVOLTAGE LOCKOUT

SOFT-START CIRCUIT

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the SG1526, the undervoltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100µA current source to charge C_S. Q2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_S. As the soft-start voltage ramps up to +5 volts, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null. Figure 10 gives the timing relationship between C_S and ramp time to 100% duty cycle.

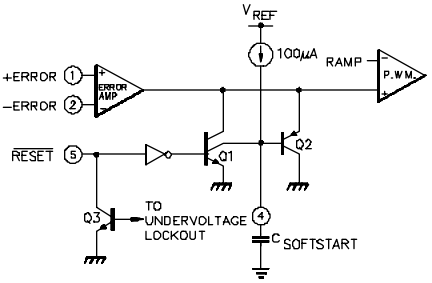

FIGURE 19.
SOFT-START CIRCUIT SCHEMATIC

DIGITAL CONTROL PORTS

The three digital control ports of the SG1526 are bi-directional. Each pin can drive TTL and 5 volt CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving SYNC LOW initiates a discharge cycle in the oscillator. Pulling SHUTDOWN LOW immediately inhibits all PWM output pulses. Holding RESET LOW discharges the soft-start capacitor. The logic threshold is +1.1 volts at 25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pullup resistor to +5 volts.

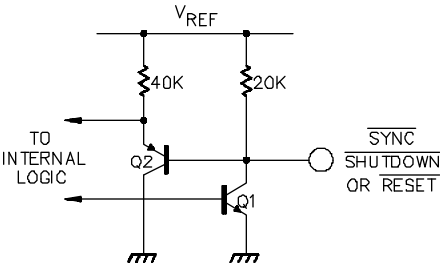

FIGURE 20.
DIGITAL CONTROL PORT SCHEMATIC

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APPLICATION INFORMATION (continued)

OSCILLATOR

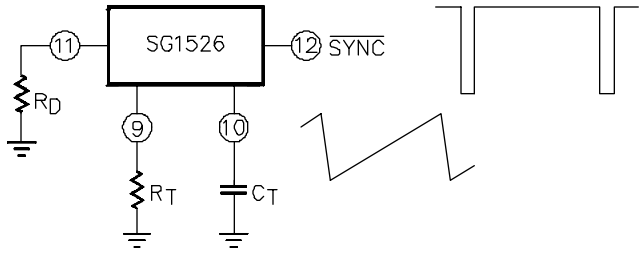

FIGURE 21 - OSCILLATOR CONNECTIONS AND WAVEFORMS

The oscillator is programmed for frequency and deadtime with three components: R_T, C_T, and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D using Figure 6 as a guide. At 40kHz dead time increases by 400nSec/ohm.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The SG1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5µSec wide at the SYNC pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all SYNC terminals are likewise connected to the $\overline{SYNC}$ pin of the master. Slave R_T terminals should not be left open nor should they be tied to the +5V reference; at least 50K should be connected to each pin. Slave R_D terminals may be either left open or grounded.

ERROR AMPLIFIER

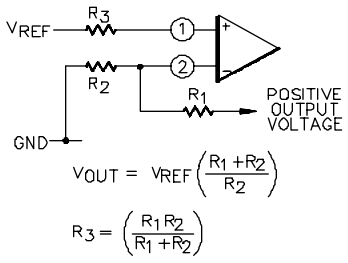

FIGURE 22A

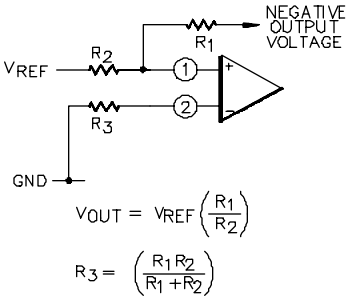

FIGURE 22B

ERROR AMPLIFIER CONNECTIONS

The error amplifier is a transconductance design, with an output impedance of 2 megohms and an effective output capacitance of 100 pF. Since all voltage gain takes place at the output pin, the open-loop gain can be shaped with shunt reactance to ground. For unity gain stability the amplifier requires an additional external 100 pF to ground, resulting in an open-loop pole at 400 Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0 volts and the feedback connections in Figure 22A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0 volt reference voltage, as shown in Figure 22B.

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APPLICATION INFORMATION (continued)

OUTPUT DRIVERS

The totem-pole output drivers of the SG1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$ pin, as required. Curves for the saturation voltage at these outputs as a function of load current are found in Figures 14 and 15.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents, as shown in Figure 25.

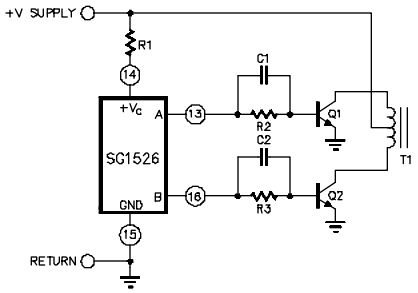


FIGURE 23.
PUSH-PULL CONFIGURATION

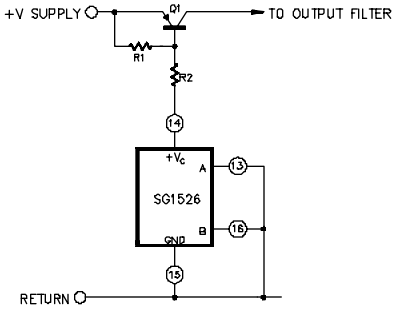


FIGURE 24.
SINGLE-ENDED CONFIGURATION

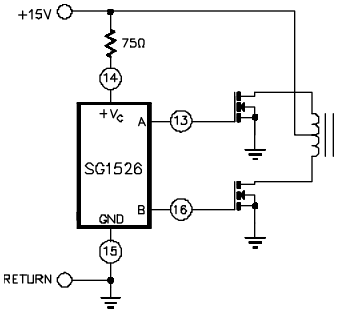
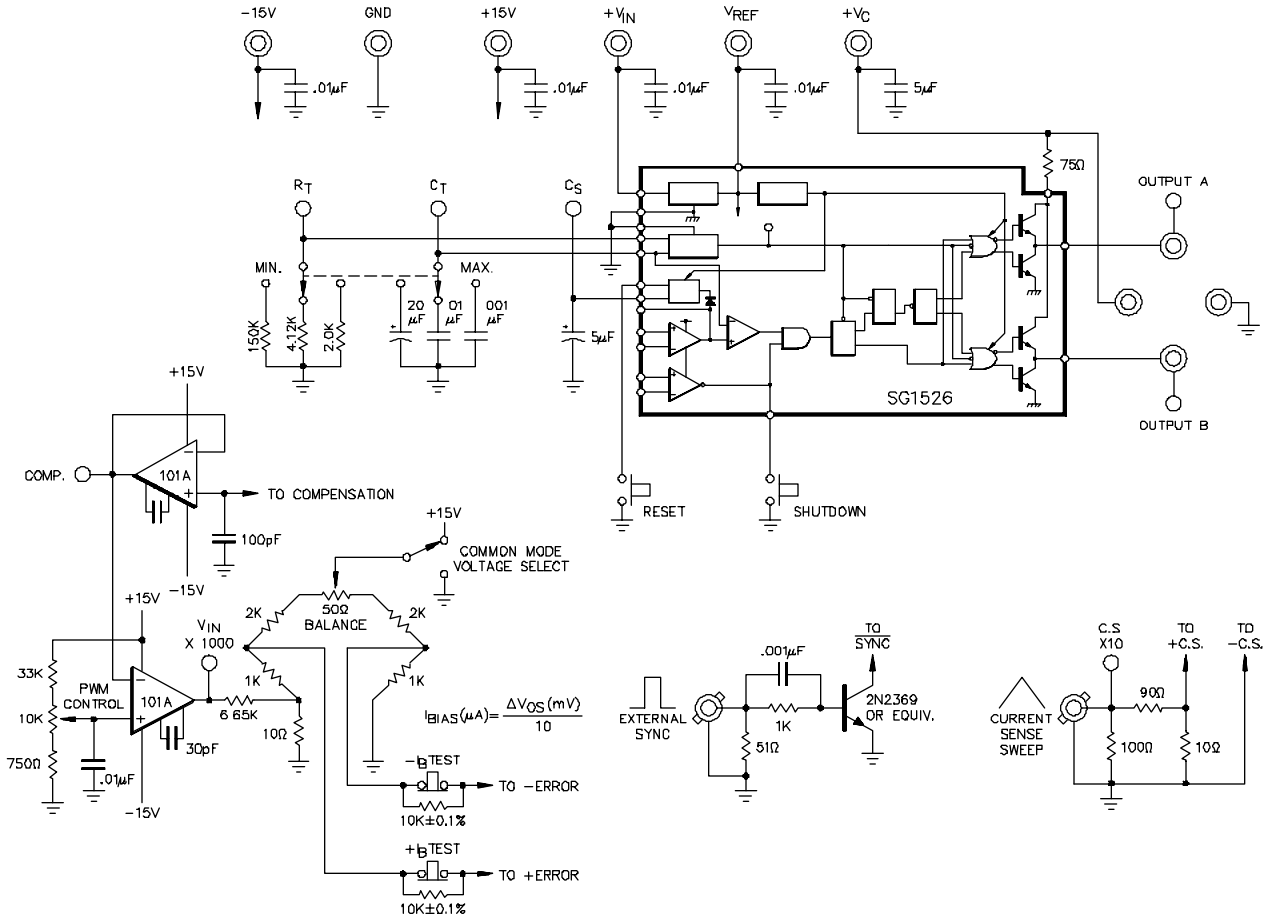


FIGURE 25.
DRIVING N-CHANNEL POWER MOSFETS

SG1526 LAB TEST FIXTURE



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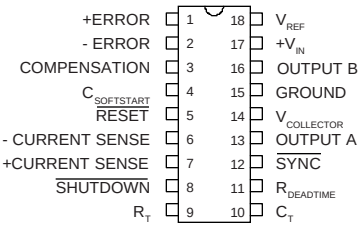
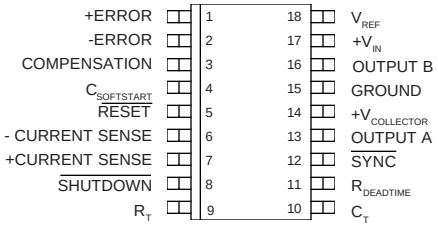
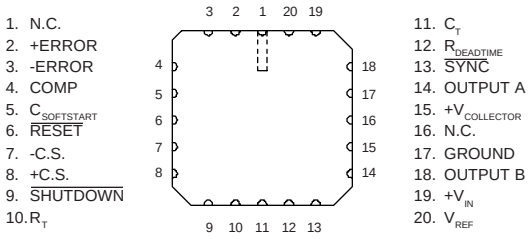
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1526J/883B SG1526J SG2526J SG3526J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
18-PIN PLASTIC DIP N - PACKAGE	SG2526N SG3526N	-25°C to 85°C 0°C to 70°C	
	N Package: RoHS Compliant / Pb-free Transition DC: 0503		N Package: RoHS / Pb-free 100% Matte Tin Lead Finish
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2526DW SG3526DW	-25°C to 85°C 0°C to 70°C	
	DW Package: RoHS Compliant / Pb-free Transition DC: 0516		DW Package: RoHS / Pb-free 100% Matte Tin Lead Finish
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1526L/883B SG1526L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

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