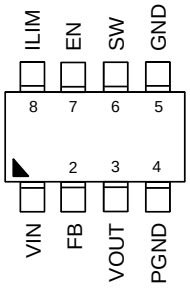
Pin Configuration

(TOP VIEW)

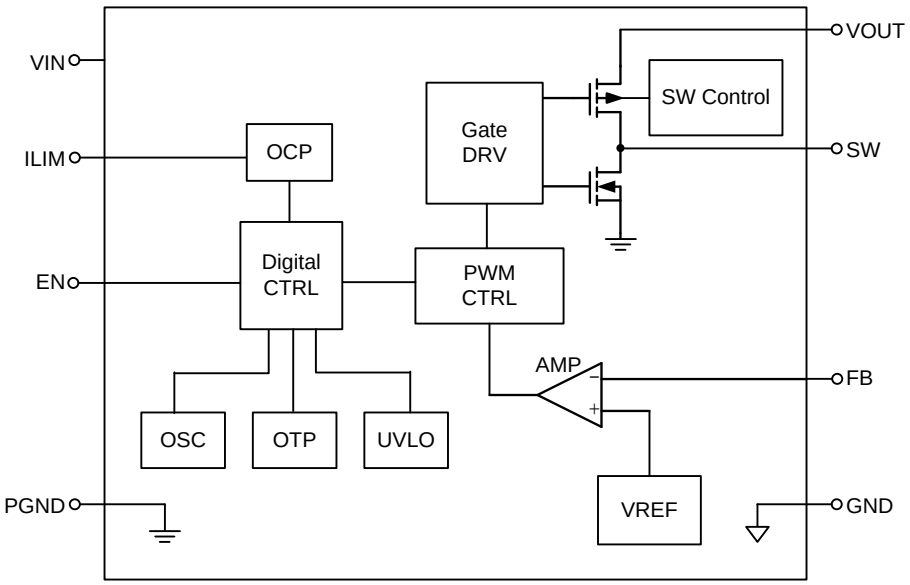


TSOT-23-8 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Power input. Input capacitor C_{IN} must be placed as close to IC as possible.
2	FB	Voltage feedback.
3	VOUT	Boost converter output.
4	PGND	Power ground.
5	GND	Analog ground.
6	SW	Switching node.
7	EN	Enable input (1 enabled, 0 disabled), must not be floating.
8	ILIM	Average output current limit control pin. (H/L)

Functional Block Diagram



Operation

The RT4812 combined built-in power transistors, synchronous rectification, and low supply current, it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to a maximum load current of 2.1A. Quiescent current in Shutdown mode is less than 1μA, which maximizes battery life.

Mode		Depiction	Condition
LIN	LIN 1	Linear startup 1	$V_{IN} > V_{OUT}$
	LIN 2	Linear startup 2	$V_{IN} > V_{OUT}$
Soft-Start		Boost soft-start	$V_{OUT} < V_{OUT(MIN)}$
Boost		Boost mode	$V_{OUT} = V_{OUT(MIN)}$

LIN State

When V_{IN} is rising, it enters the LIN State. There are two parts for the LIN state. It provides maximum current for 1A to charge the C_{OUT} in LIN1, and the other one is for 3A in LIN2. By the way, the EN is pulled high and V_{IN} > UVLO.

As the figure shown, if the timeout is over the specification, it will enter the Fault mode.

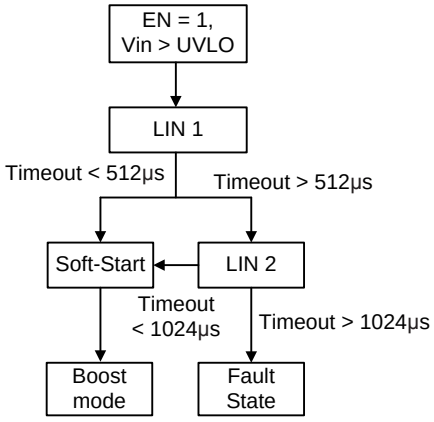


Figure 1. RT4812 State Chart

Startup and Shutdown State

When V_{IN} is rising and through the LIN state, it will enter the Startup state. If EN is pulled low, any function is turned-off in shutdown mode.

Soft-Start State

It starts to switch in Soft-start state. After the LIN state, output voltage is rising with the internal reference voltage.

Fault State

As the Figure 1 shown, it will enter to the Fault state as below,

- The timeout of LIN2 is over the 1024μs.

It will be the high impedance between the input and output when the fault is triggered. A restart will be start after 20ms.

OCP

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, the OCP is cycle by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

OTP

The converter has an over-temperature protection. When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

Absolute Maximum Ratings (Note 1)

- VIN, FB, ILIM, EN, SW to GND ---------- –0.2V to 6V
- VOUT to GND ---------- 6.2V
- Power Dissipation, PD @ TA = 25°C
- TSOT-23-8 (FC) ---------- 1.78W
- Package Thermal Resistance (Note 2)

  TSOT-23-8 (FC), θ_{JA} ---------- 56°C/W

  TSOT-23-8 (FC), θ_{JC} ---------- 28°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- –65°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range ---------- 1.8V to 5.5V
- Output Voltage Range ---------- 1.8V to 5.5V
- Junction Temperature (T_J) Range ---------- –40°C to 125°C
- Ambient Temperature (T_A) Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{IN}	$V_{IN} < V_{OUT} - 0.2V$	1.8	--	5.5	V
Output Voltage	V_{OUT}	$V_{IN} < V_{OUT} - 0.2V$	1.8	--	5.5	V
Under Voltage Lockout Rising Threshold	$UVLO_{\_RISE}$		1.5	1.65	1.8	V
Under Voltage Lockout Falling Threshold	$UVLO_{\_Falling}$		1.3	1.55	1.7	V
FB Voltage	V_{FB}	Force PWM	0.495	0.5	0.505	V
Regulated DC V_{OUT} Voltage	V_{OUT}	$1.8 \le V_{IN} \le V_{OUT} - 0.2V$ I_{OUT} = 0mA (PSM)	–2	--	4	%
Shutdown Current	I_{SHDN}	EN = 0V	--	0.1	1	μA
Quiescent Current		Close loop, no load FB = 3V, non-switching current	--	90	--	μA
Pre-charge Current	Ipre		--	1	--	A
Switching Frequency	f_{SW}	$V_{OUT} - V_{IN} > 1V$	--	0.5	--	MHz
Average Output Current Limit	I_{LIM}	I_{LIM} = L	1	--	--	A
		I_{LIM} = H	2.1	--	--	
High Side Switch Ron		V_{IN} = 5V	--	45	--	mΩ
Low Side Switch Ron		V_{IN} = 5V	--	30	--	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB Pin Input Leakage	I_{FB}		–1	--	1	μA
Leakage of SW	I_{SW}	All switch off	--	--	5	μA
Line Regulation	$\Delta V_{OUT, LINE}$	V_{IN} = 2.7V to 4.5V, V_{OUT} = 5V, I_{OUT} = 1500mA	–2	--	2	%
Load Regulation	$\Delta V_{OUT, LOAD}$	CCM, I_{OUT} < 2A, V_{IN} = 3.6V, V_{OUT} = 5V	–1.5	--	1.5	%
Output Over Voltage Protection	V_{OVP}		5.8	6	6.2	V
EN Input Low Voltage	V_{IL}		--	--	0.4	V
EN Input High Voltage	V_{IH}		1.2	--	--	V
EN Sink Current			--	0.1	1	μA
Thermal Shutdown	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	30	--	°C

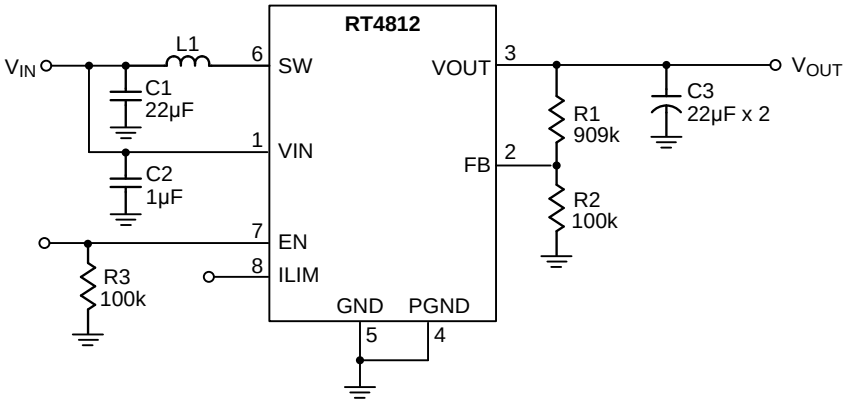
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a two-layer Richtek Evaluation Board.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

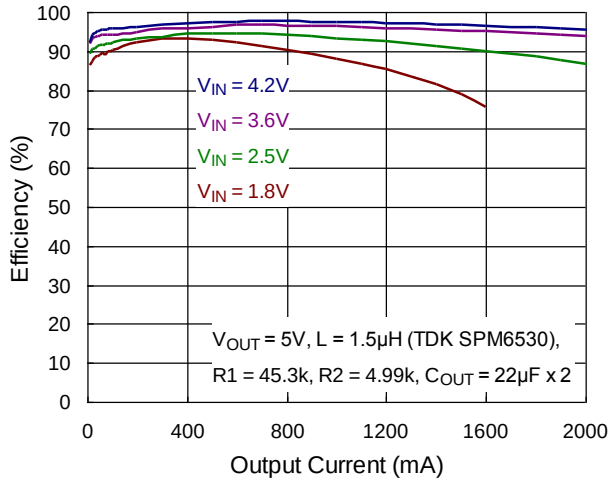
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

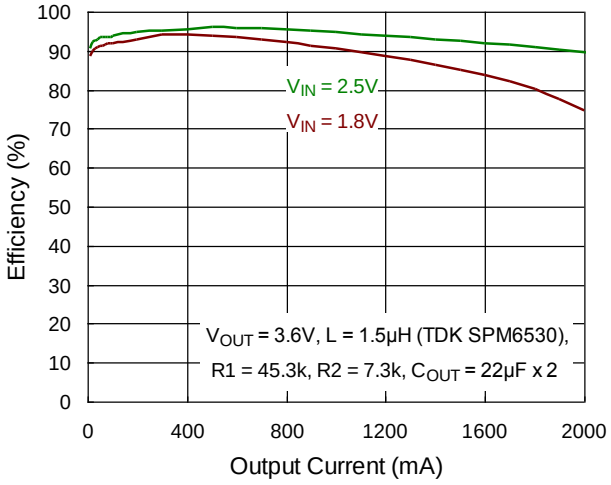


Typical Operating Characteristics

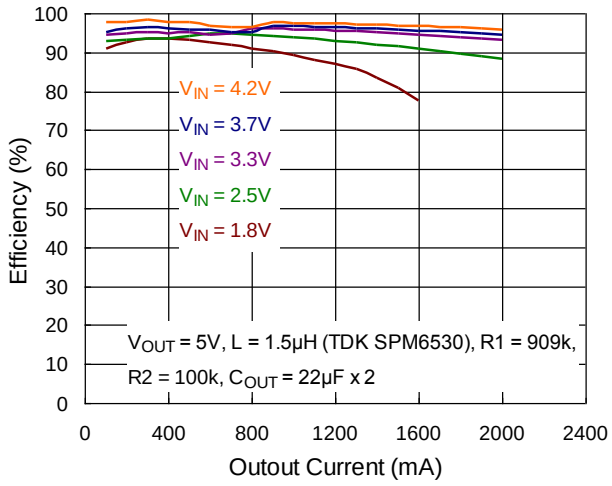
Efficiency vs. Output Current



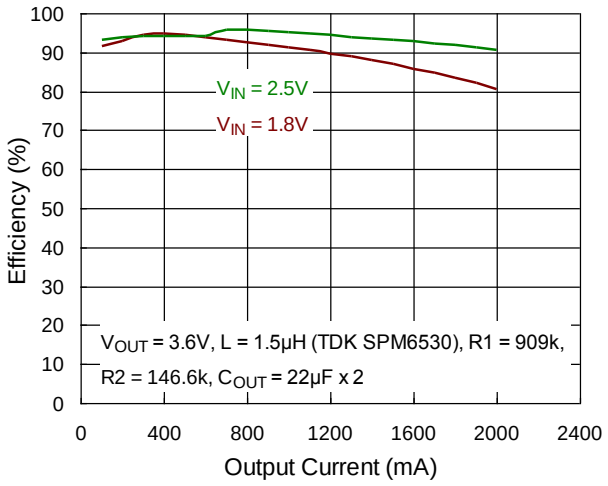
Efficiency vs. Output Current



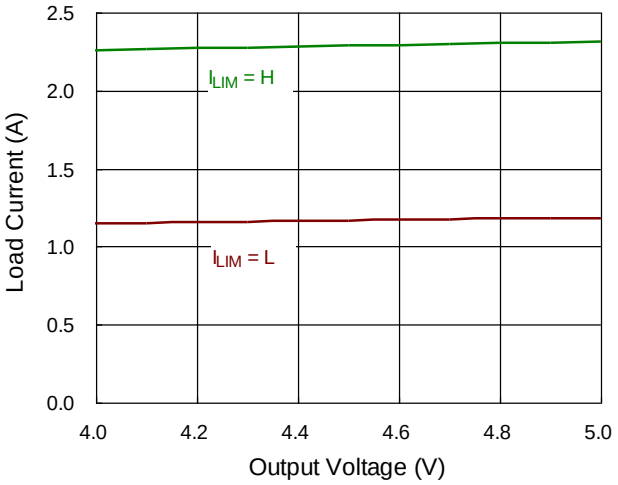
Efficiency vs. Outout Current



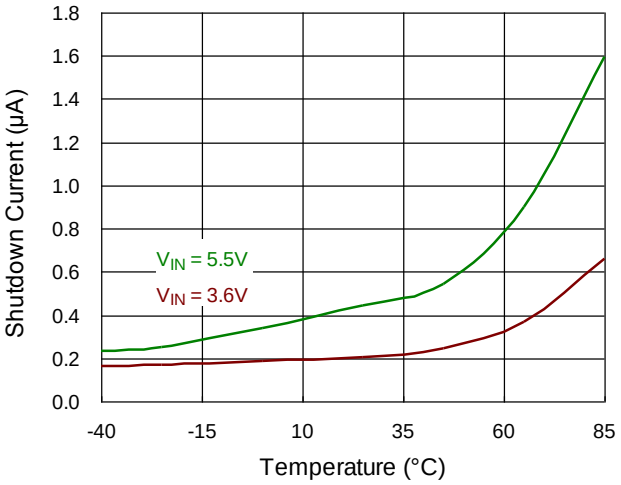
Efficiency vs. Output Current



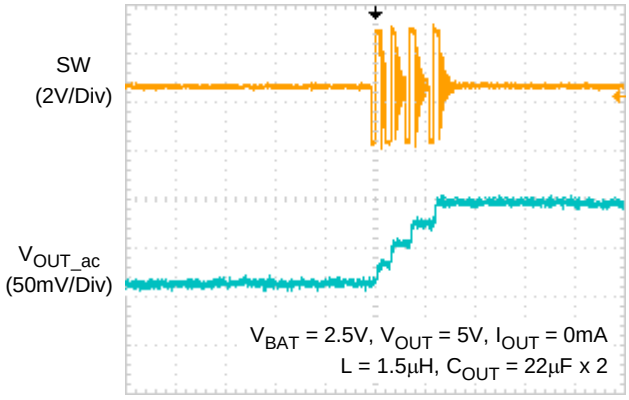
Load Current vs. Output Voltage



Shutdown Current vs. Temperature

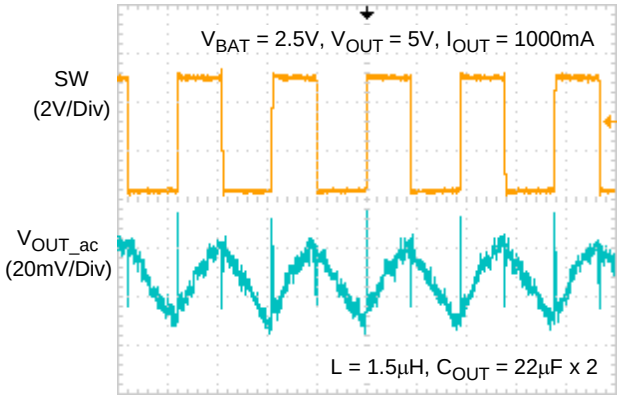


Output Voltage Ripple



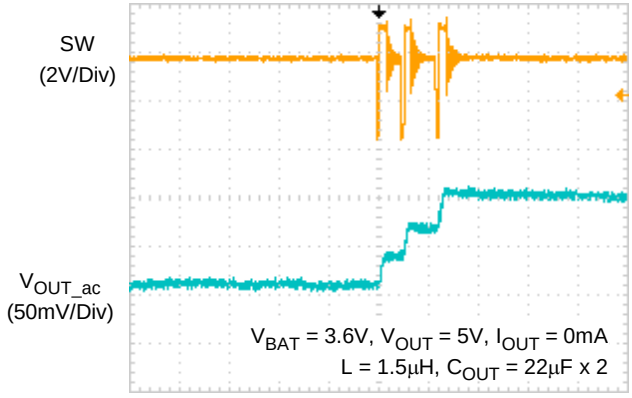
Time (10µs/Div)

Output Voltage Ripple



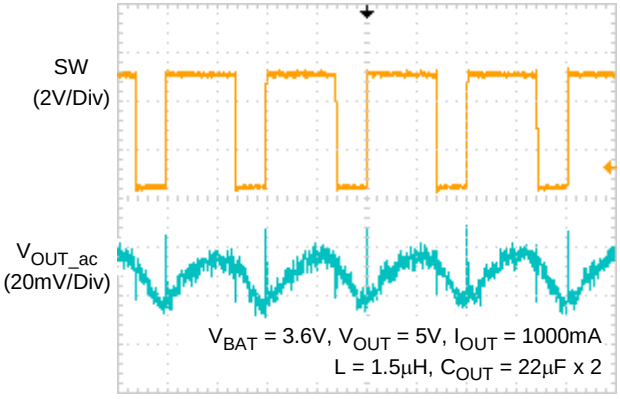
Time (1µs/Div)

Output Voltage Ripple



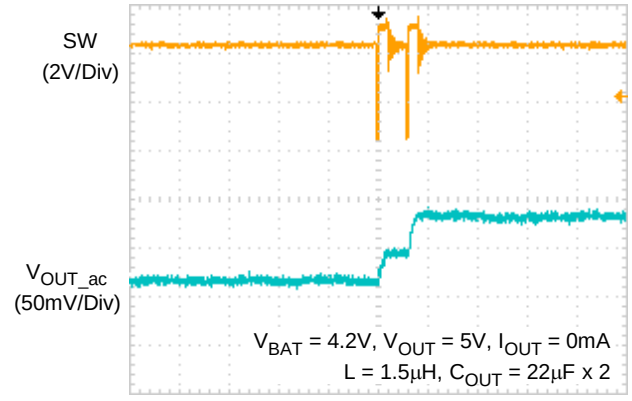
Time (10µs/Div)

Output Voltage Ripple



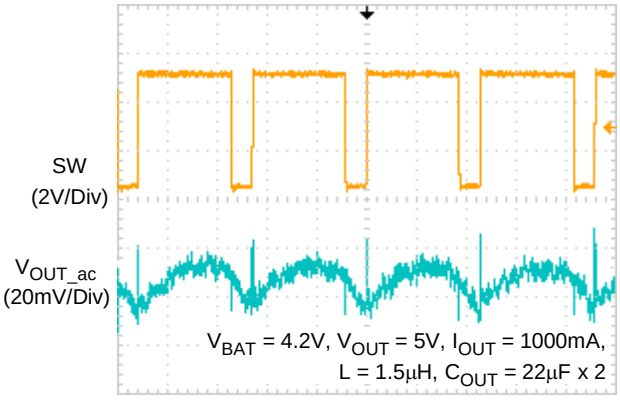
Time (1µs/Div)

Output Voltage Ripple



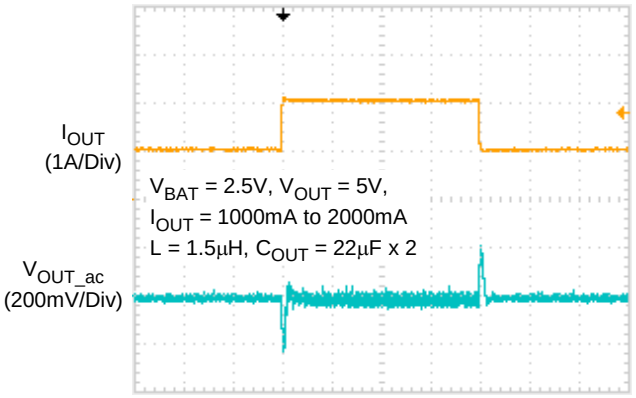
Time (10µs/Div)

Output Voltage Ripple



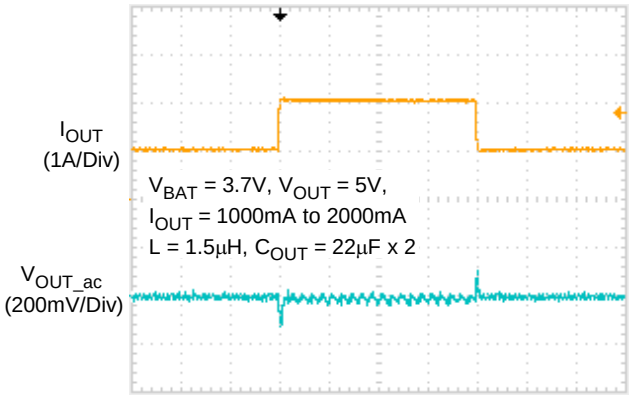
Time (1µs/Div)

Load Transient Response



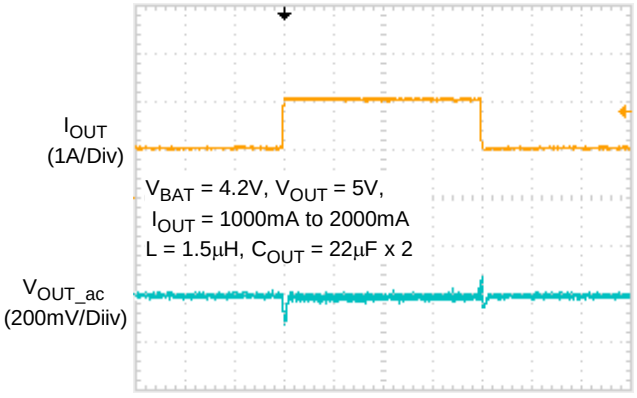
Time (500µs/Div)

Load Transient Response



Time (500µs/Div)

Load Transient Response



Time (500µs/Div)

Application Information

Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

Soft-Start State

After the successful completion of the LIN state (V_{OUT} ≥ V_{IN} = 300mV), the regulator begins switching with boost valley-current limited value 3500mA.

During Soft-Start state, V_{OUT} is ramped up by Boost internal loop. If V_{OUT} fails to reach target value during the Soft-Start period for more than 2ms, a fault condition is declared.

Output Voltage Setting

The output voltage is adjustable by an external resistive divider. The resistive divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. Output voltage can be calculated by equation as below :

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

Power Save Mode

PSM is the way to improve efficiency at light load.

When the output voltage is lower than a set threshold voltage, the converter will operate in PSM.

It raises the output voltage with several pulses until the loop exits PSM.

Under-Voltage Lockout

The under-voltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions and prevents the battery from deep discharge. VIN voltage must be greater than 1.65V to enable the converter. During operation, if VIN voltage drops below 1.55V, the converter is disabled and waiting internal IC default parameter value ready until the supply exceeds the UVLO rising threshold. The RT4812 automatically restarts if the input voltage recovers to the input voltage UVLO high level.

Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over temperature threshold.

Inductor Selection

The recommended nominal inductance value is 1.5μH

It is recommended to use inductor with dc saturation current ≥ 5000mA

Table 1. List of Inductors

Manufacturer	Series	Dimensions (in mm)	Saturation Current (mA)
TDK	SPM6530T	7.1 x 6.5 x 3.0	11500
Taiyo Yuden	NRS5040T	5.15 x 5.15 x 4.2	6400

Input Capacitor Selection

At least a 22μF and the rate voltage is 16V for DC bias input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for SW. And at least a 1μF ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor Selection

At least 22μF x 2 capacitors is recommended to improve V_{OUT} ripple.

Output voltage ripple is inversely proportional to C_{OUT}.

Output capacitor is selected according to output ripple which is calculated as :

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore :

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

The maximum V_{RIPPLE} occurs at minimum input voltage and maximum output load.

Output Discharge Function

With the EN pin set to low, the VOUT pin is internally connected to GND for 10ms by an internal discharge N-MOSFET switch. After the 10ms, IC will be true-shut down.

This feature prevents residual charge voltages on capacitor connected to VOUT pins, which may impact proper power up of the system.

Valley Current Limit

The RT4812 employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V_{OUT} – V_{IN}) / V_{OUT} ratio. The output voltage decreases when further loading current increase. The current limit function is implemented by the scheme, refer to Figure 2.

Average Output Current Limit

The RT4812 features the average output current limit to protect the output terminal. When the load current is over the limit, output current will be clamped.

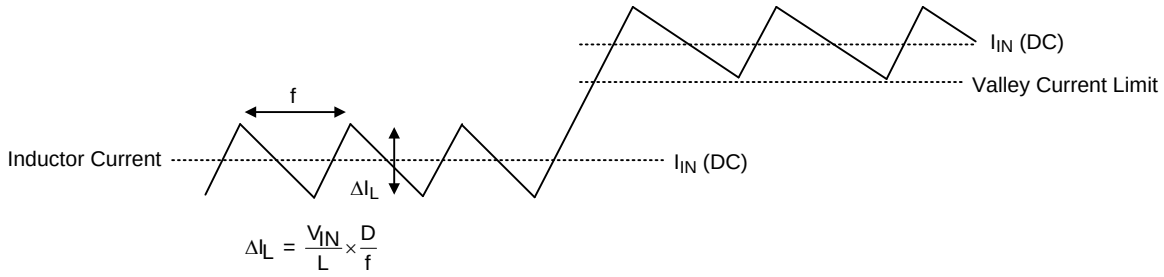


Figure 2. Inductor Currents In Current Limit Operation

Table 2. List of Capacitor

Reference	Qty.	Part Number	Description	Package	Manufacturer
CIN	1	GRM21BR61C226ME44	22μF / 16V / X5R	0805	MuRata
COUT	2	GRM21BR61C226ME44	22μF / 16V / X5R	0805	MuRata

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSOT-23-8 (FC) package, the thermal resistance, θ_{JA}, is 56°C/W on a standard two-layer EVB test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (56°C/W) = 1.78W for TSOT-23-8 (FC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

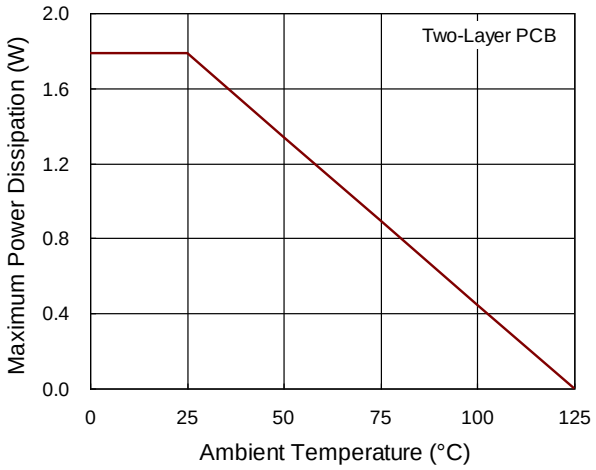


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Consideration

The PCB layout is an important step to maintain the high performance of the RT4812.

Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT4812 through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4812, the following PCB layout guidelines must be strictly followed.

- Input/Output capacitors must be placed as close as possible to the Input/Output pins.
- SW should be connected to Inductor by wide and short trace, keep sensitive components away from this trace.
- The feedback divider should be placed as close as possible to the FB pin.

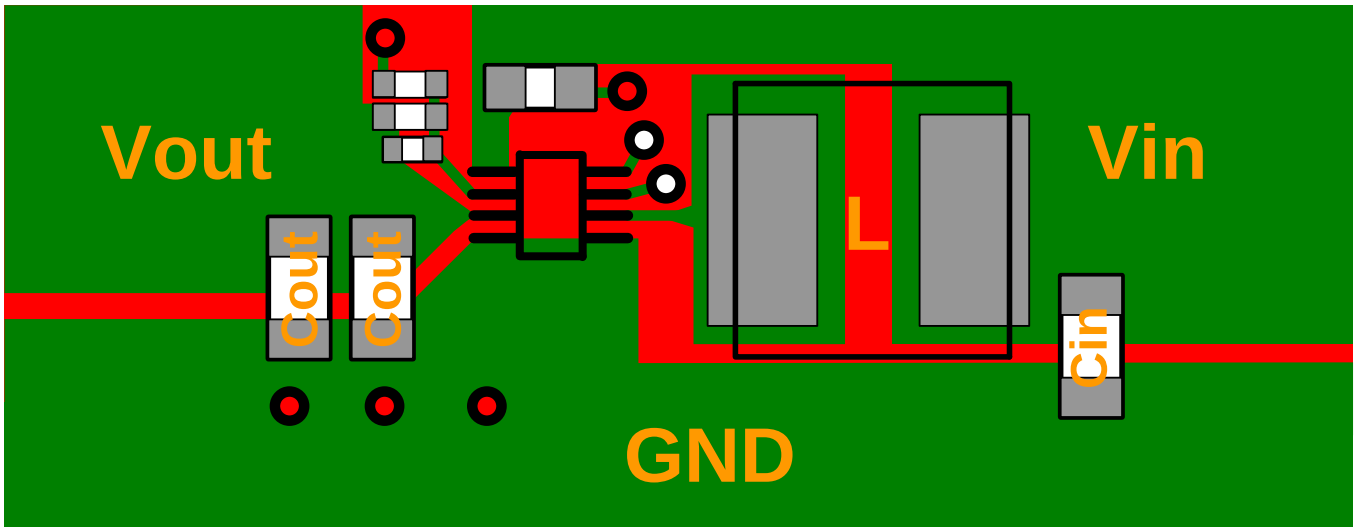
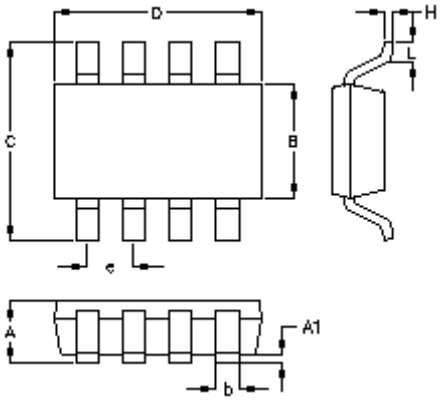


Figure 4. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 (FC) Surface Mount Package

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