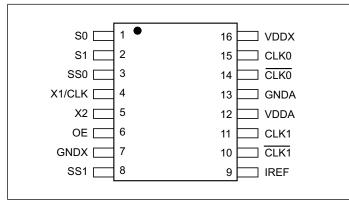




# **Pin Configuration**



# **Pin Description**

Pin #	Pin Name	I/О Туре	Description
1	SO	Input	Select pin 0 (Internal pull-up resistor). See Table 1.
2	S1	Input	Select pin 1 (Internal pull-up resistor). See Table 1.
3	SS0	Input	Spread Select pin 0 (Internal pull-up resistor). See Table 2.
4	X1/CLK	Input	Crystal or clock input. Connect to a 25MHz crystal or single ended clock.
5	X2	Output	Crystal connection. Leave unconnected for clock input.
6	OE	Input	Output enable. Internal pull-up resistor.
7	GNDX	Power	Crystal ground pin.
8	SS1	Input	Spread Select pin 1 (Internal pull-up resistor). See Table 2.
9	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
10	CLK1	Output	HCSL compliment clock output
11	CLK1	Output	HCSL clock output
12	VDDA	Power	Connect to a +3.3V source.
13	GNDA	Power	Output and analog circuit ground.
14	CLK0	Output	HCSL compliment clock output
15	CLK0	Output	HCSL clock output
16	VDDX	Power	Connect to a +3.3V source.

### Table 1: Output Select Table

<u>S1</u>	<b>S0</b>	CLK(MHz)
0	0	25
0	1	100
1	0	125
1	1	200

## Table 2: Spread Selection Table

SS1	SS0	Spread	
0	0 Center ±0.		
0	1 Down -0.5		
1	0 Down -0.7		
1	1	No Spread	





# Application Information

## **Decoupling Capacitors**

Decoupling capacitors of 0.01µF should be connected between each V<sub>DD</sub> pin and the ground plane and placed as close to the V<sub>DD</sub> pin as possible.

## Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

# **Crystal Capacitors**

 $C_L$  = Crystals's load capacitance in pF

Crystal Capacitors (pF) = (CI - 8) \*2

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. (16-8)\*2=16.

## Current Source (Iref) Reference Resistor - R<sub>R</sub>

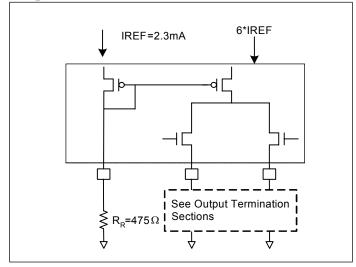
If board target trace impedance is  $50\Omega$ , then  $R_R = 475\Omega$  providing an IREF of 2.32 mA. The output current (I<sub>OH</sub>) is 6\*IREF.

## **Output** Termination

The PCI Express differential clock outputs of the PI6C557-03 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The PI6C557-03 can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

## **Output Structures**



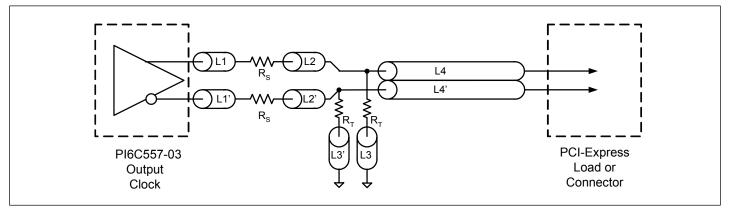




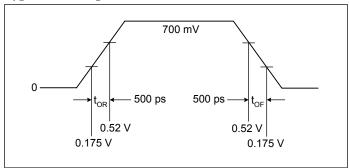
# **PCI Express Layout Guidelines**

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled $50\Omega$ trace.	0.5 max	inch
L2 length, route as non-coupled $50\Omega$ trace.	0.2 max	inch
L3 length, route as non-coupled $50\Omega$ trace.	0.2 max	inch
R <sub>S</sub>	33	Ω
R <sub>T</sub>	49.9	Ω
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip $100\Omega$ differential trace.	2 min to 16 max	inch
L4 length, route as coupled stripline $100\Omega$ differential trace.	1.8 min to 14.4 max	inch
Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip $100\Omega$ differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled stripline $100\Omega$ differential trace.	0.225 min to 12.6 max	inch

## **PCI Express Device Routing**



# Typical PCI Express (HCSL) Waveform



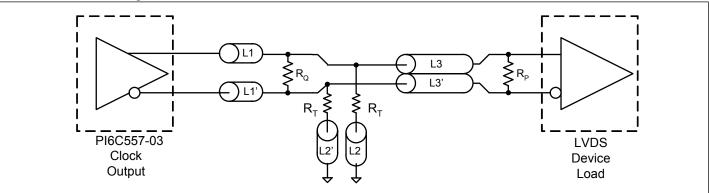




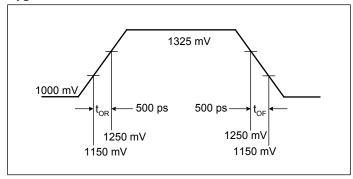
# **Application Information**

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled $50\Omega$ trace.	0.5 max	inch
L2 length, route as non-coupled $50\Omega$ trace.	0.2 max	inch
R <sub>p</sub>	100	Ω
R <sub>Q</sub>	100	Ω
R <sub>T</sub>	150	Ω
L3 length, route as $100\Omega$ differential trace.		
L3 length, route as $100\Omega$ differential trace.		

# LVDS Device Routing



# **Typical LVDS Waveform**







# **Electrical Specifications**

## **Maximum Ratings**

Supply Voltage to Ground Potential5.5V	7
All Inputs and Outputs0.5V to $\mathrm{V_{DD}}\text{+}0.5\mathrm{V}$	7
Ambient Operating Temperature40 to +85°C	2
Storage Temperature65 to +150°C	2
Junction Temperature	2
Soldering Temperature	2

### Note:

Stresses greater than those listed under MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **Recommended Operation Conditions**

Parameter	Min.	Тур.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)			+3.6	V

### DC Characteristics ( $V_{DD}$ = 3.3V ±10%, $T_A$ = -40°C to +85°C)

Symbol	Parameter	Conditions		Min.	Тур.	Max.	Unit
V <sub>DD</sub>	Supply Voltage			3.0	3.3	3.60	V
V <sub>IH</sub>	Input High Voltage <sup>(1)</sup>	S0, S1, OE, CLK,	SS0, SS1	2.0		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage <sup>(1)</sup>	S0, S1, OE, CLK,	SS0, SS1	GND -0.3		0.8	V
I <sub>IL</sub>	Input Leakage Current	0 < Vin < VDD	With input pull-up and pull-downs	-20		20	
			Without input pull-up and pull-downs	-5		5	μΑ
I <sub>DD</sub>	Operating Supply	$R_L = 50\Omega, C_L = 2$	pF			95	mA
I <sub>DDOE</sub>	Current	OE = LOW				50	mA
C <sub>IN</sub>	Input Capacitance	Input pin capacitance				7	pF
C <sub>OUT</sub>	Output Capacitance	put Capacitance Output pin capacitance				6	pF
L <sub>PIN</sub>	Pin Inductance					5	nH
R <sub>OUT</sub>	Output Resistance	CLK Outputs		3.0			kΩ

### Notes:

1. Single edge is monotonic when transitioning through region.





Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
F <sub>IN</sub>	Input Frequency			25		MHz
V <sub>OUT</sub>	Output Frequency		25		200	MHz
V <sub>OH</sub>	Output High Voltage <sup>(1,2)</sup>	$@V_{DD} = 3.3V$	660	700	850	mV
V <sub>OL</sub>	Output Low Voltage <sup>(1,2)</sup>		-150	0		mV
V <sub>CPA</sub>	Crossing Point Voltage <sup>(1,2)</sup>	Absolute	250	350	550	mV
V <sub>CN</sub>	Crossing Point Voltage <sup>(1,2,4)</sup>	Variation over all edges			140	mV
J <sub>CC</sub>	Jitter, Cycle-to-Cycle <sup>(1,3)</sup>			60	100	ps
MF	Modulation Frequency	Spread Spectrum	30	31.5	33	kHz
t <sub>OR</sub>	Rise Time <sup>(1,2)</sup>	From 0.175V to 0.525V	175	332	700	ps
t <sub>OF</sub>	Fall Time <sup>(1,2)</sup>	From 0.525V to 0.175V	175	344	700	ps
$\Delta T_R / \Delta T$	Rise/Fall Time Variation <sup>(1,2)</sup>				125	ps
T <sub>SKEW</sub>	Skew between outputs	V <sub>DD</sub> /2			50	ps
T <sub>DUTY-</sub> cycle	Duty Cycle <sup>(1,3)</sup>		45		55	%
T <sub>OE</sub>	Output Enable Time <sup>(5)</sup>	All outputs		0.1		μs
T <sub>OT</sub>	Output Disable Time <sup>(5)</sup>	All outputs		0.1		μs
t <sub>STABLE</sub>	From power-up to VDD=3.3V		1.6	3.0		ms
t <sub>SPREAD</sub>	Setting period after spread change			3.0		ms
F <sub>error</sub>	Synthesizer Error	PLL locked, xtal load is matched and SSC off		0		ppm

# AC Characteristics ( $V_{DD} = 3.3V \pm 10\%$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ )

Notes:

1. RL =  $50\Omega$  with CL = 2 pF and RR =  $475\Omega$ 

2. Single-ended waveform

3. Differential waveform

4. Measured at the crossing point

5. CLK pins are tri-stated when OE is LOW

### **Thermal Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
$\theta_{JA}$	Thermal Resistance Junction to Ambient	Still air			90	°C/W
$\theta_{JC}$	Thermal Resistance Junction to Case				24	°C/W

### **Recomended Crystal Specification**

Diodes recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm http://www.pericom.com/pdf/datasheets/se/GC\_GF.pdf b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm http://www.pericom.com/pdf/datasheets/se/FY\_F9.pdf c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm http://www.pericom.com/pdf/datasheets/se/FL.pdf

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# **Part Marking**

L Package Cu



X: Die Rev W: Year & Workweek 1st X: Assembly Code 2nd X: Fab Code

L Package Au

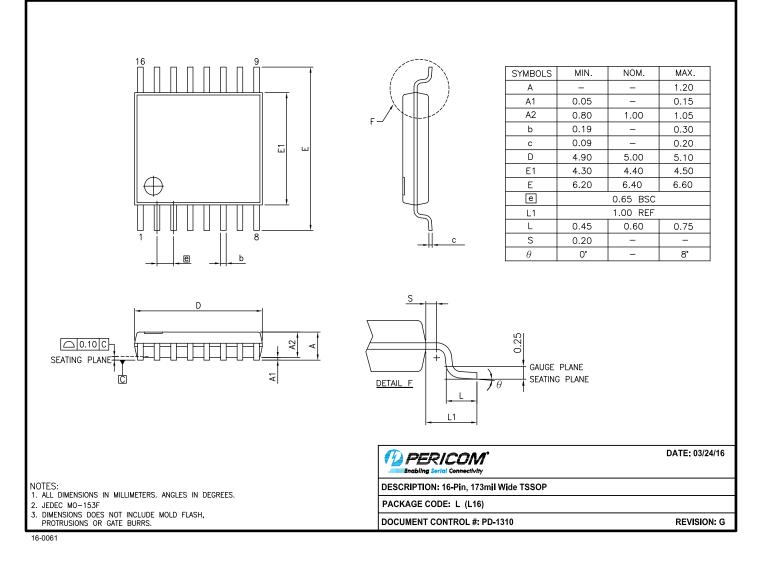


X: Die Rev YW: Year & Workweek 1st X: Assembly Code 2nd X: Fab Code





# Packaging Mechanical: 16-TSSOP (L)



### For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

# **Ordering Information**

Ordering Code	Package Code	Package Description
PI6C557-03LEX	L	16-Pin, 173mil Wide (TSSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. E = Pb-free and Green

5. X suffix = Tape/Reel

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