Typical Performance Data @ 25°C, V_{DD} = 3.0V unless otherwise noted

Figure 3. Insertion Loss

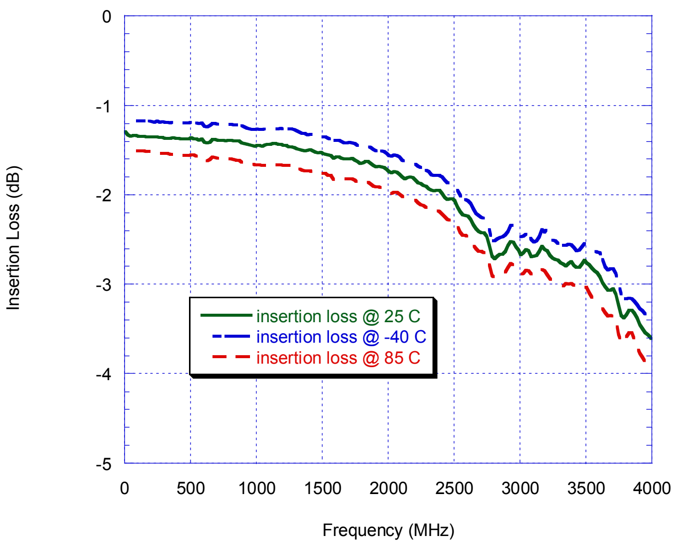


Figure 4. Attenuation at Major steps

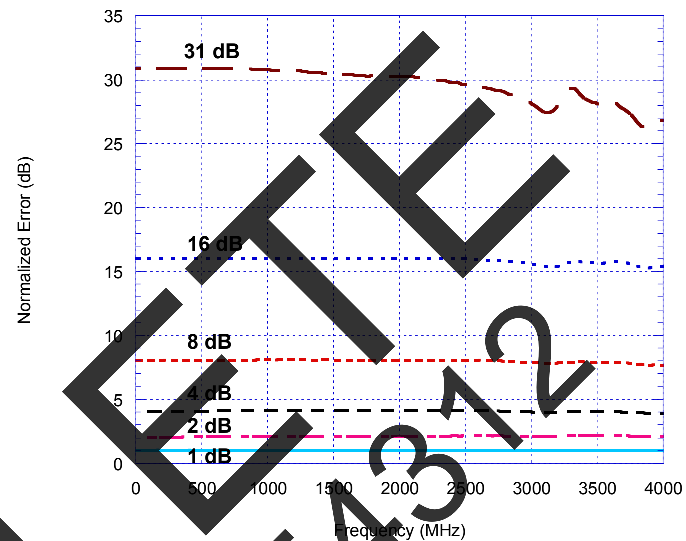


Figure 5. Input Return Loss at Major Attenuation Steps

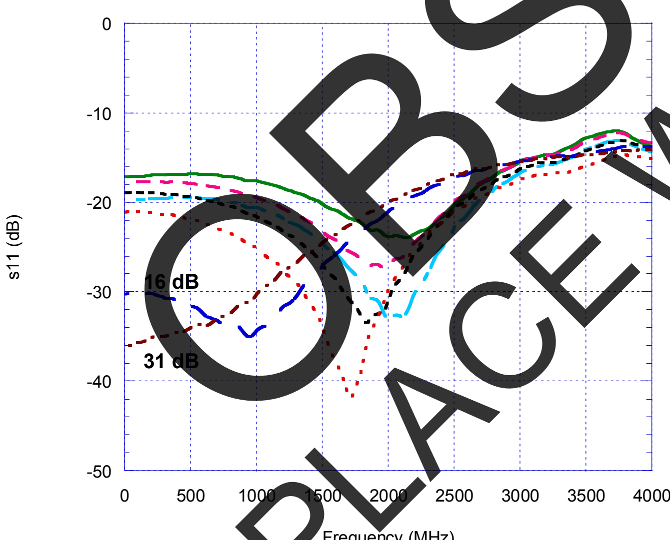
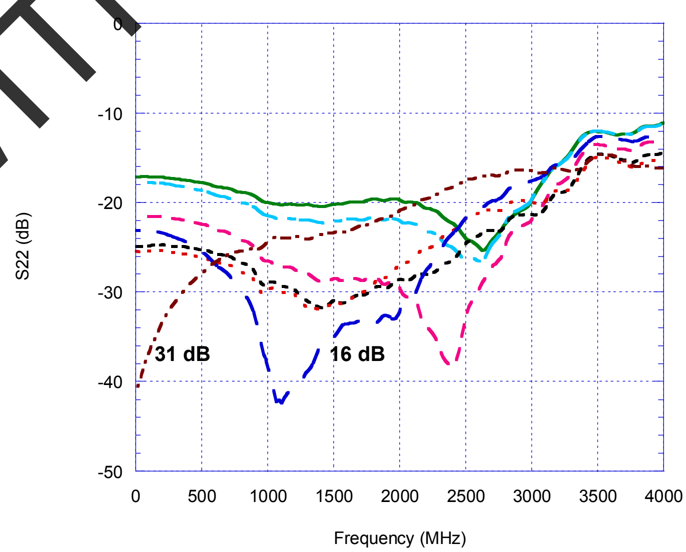


Figure 6. Output Return Loss at Major Attenuation Steps



Typical Performance Data @ 25°C, V_{DD} = 3.0V unless otherwise noted

Figure 7. Attenuation Error vs. Frequency

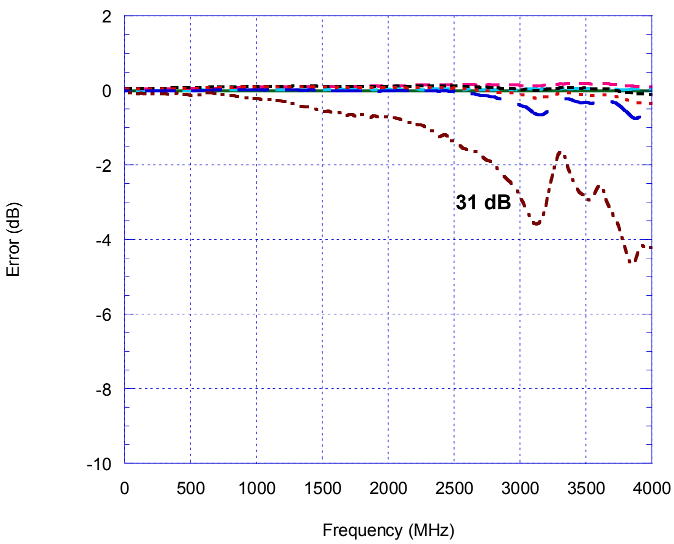


Figure 8. Attenuation Error vs. Attenuation Setting at 10 MHz and 510 MHz

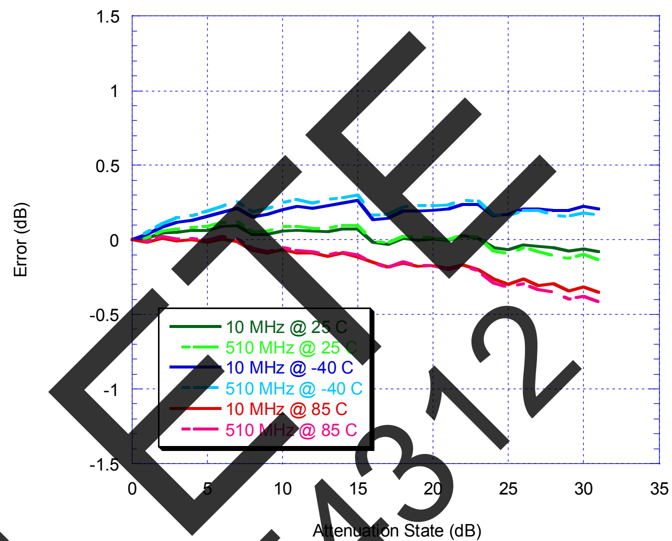


Figure 9. Attenuation Error vs. Attenuation Setting 1010 MHz and 1210 MHz

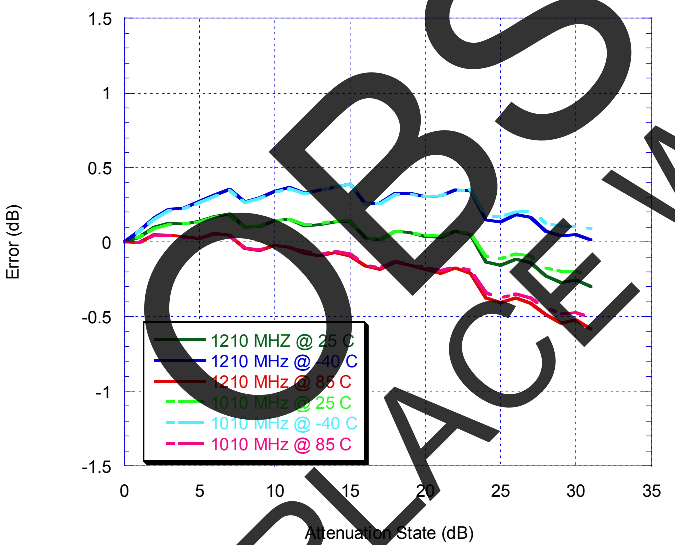
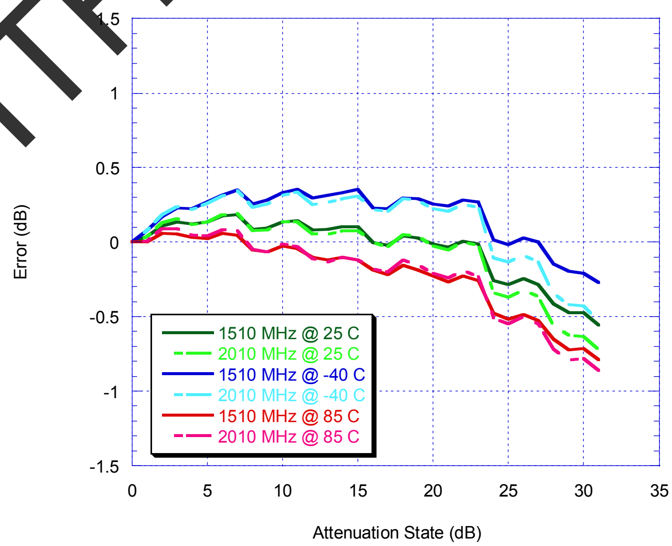


Figure 10. Attenuation Error vs. Attenuation Setting at 1510 MHz and 2010 MHz



Note: Positive attenuation error indicates higher attenuation than target value

Typical Performance Data @ 25°C, V_{DD} = 3.0V unless otherwise noted

Figure 11. Attenuation Error vs. Attenuation Setting at 2010 MHz and 2510 MHz

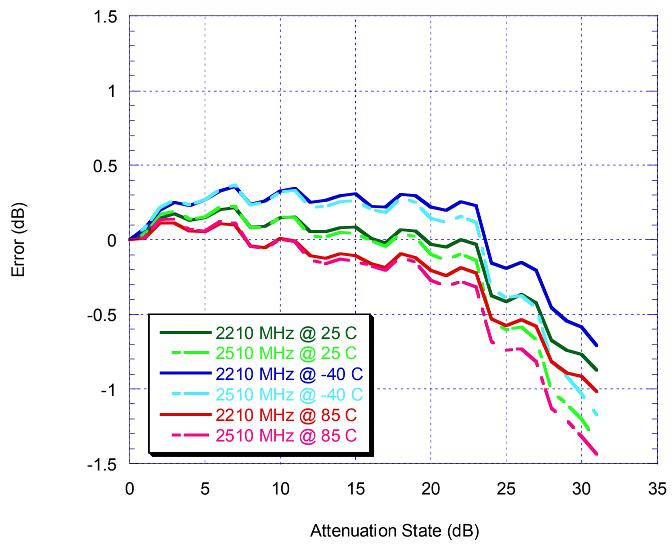


Figure 12. 1 dB Compression vs. Frequency

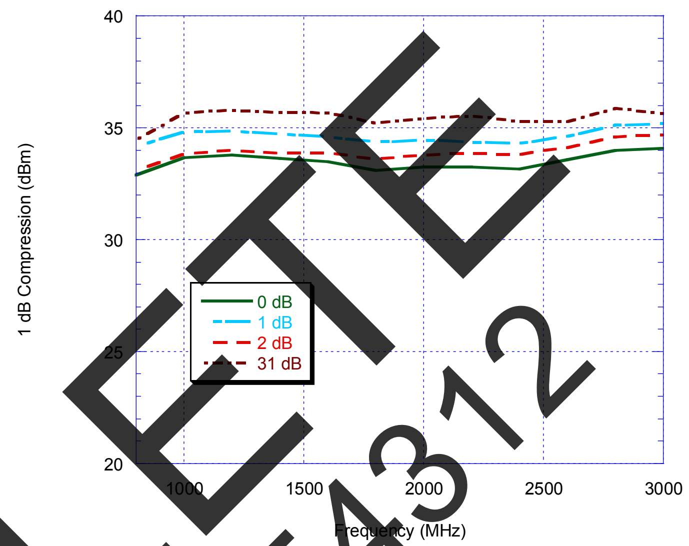
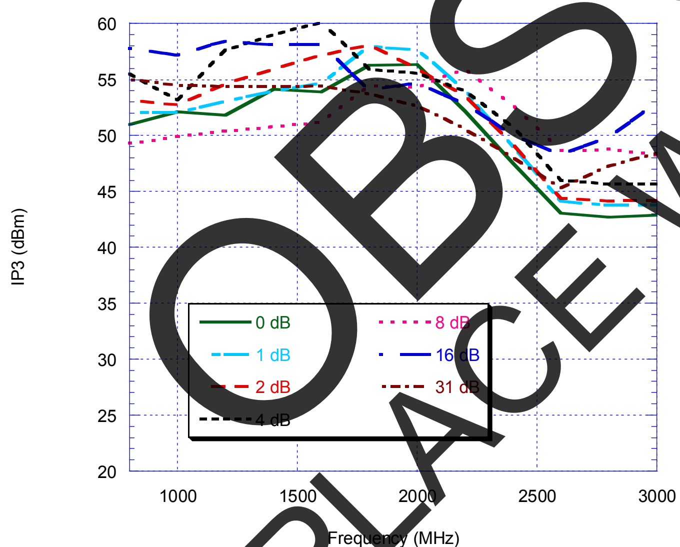


Figure 13. Input IP3 vs. Frequency



Note: Positive attenuation error indicates higher attenuation than target value

Figure 14. Pin Configuration (Top View)

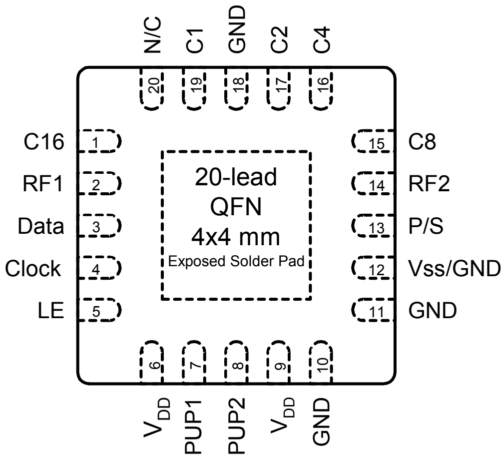


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	C16	Attenuation control bit, 16 dB (Note 4)
2	RF1	RF port (Note 1)
3	Data	Serial interface data input (Note 4)
4	Clock	Serial interface clock input
5	LE	Latch Enable input (Note 2)
6	V_{DD}	Power supply pin
7	PUP1	Power-up selection bit
8	PUP2	Power-up selection bit
9	V_{DD}	Power supply pin
10	GND	Ground connection
11	GND	Ground connection
12	V_{ss}/GND	Negative supply voltage or GND connection (Note 3)
13	P/S	Parallel/Serial mode select
14	RF2	RF port (Note 1)
15	C8	Attenuation control bit, 8 dB
16	C4	Attenuation control bit, 4 dB
17	C2	Attenuation control bit, 2 dB
18	GND	Ground connection
19	C1	Attenuation control bit, 1 dB
20	N/C	No connect. Can be connected to any bias
Paddle	GND	Ground for proper operation

Notes: 1. Both RF ports must be held at 0 V_{DC} or DC blocked with an external series capacitor
2. Latch Enable (LE) has an internal 100 kΩ resistor to V_{DD}
3. Connect pin 12 to GND to enable internal negative voltage generator. Connect pin 12 to V_{SS} ($-V_{DD}$) to bypass and disable internal negative voltage generator
4. Place a 10 kΩ resistor in series, as close to pin as possible to avoid frequency resonance. See "Resistor on Pin 1 & 3" paragraph

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the 5x5 mm QFN package is MSL1.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50Ω)		+30	dBm
V_{ESD}	ESD voltage (Human Body Model)		500	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current			100	µA
Digital Input High	0.7xV_{DD}			V
Digital Input Low			0.3xV_{DD}	V
Digital Input Leakage			1	µA
Input Power			+24	dBm
Temperature range	-40		85	°C

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified in *Table 3*.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE4306 has a maximum 25 kHz switching rate.

Resistor on Pin 1 & 3

A 10 kΩ resistor on the inputs to Pin 1 & 3 (see *Figure 16*) will eliminate package resonance between the RF input pin and the two digital inputs. Specified attenuation error versus frequency performance is dependent upon this condition.

Programming Options

Parallel/Serial Selection
Either a parallel or serial interface can be used to control the PE4306. The P/S bit provides this selection, with P/S = LOW selecting the parallel interface and P/S = HIGH selecting the serial interface.

Parallel / Direct Mode Interface
The parallel interface consists of five CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 5*.

The parallel interface timing requirements are defined by *Figure 18* (Parallel Interface Timing Diagram), *Table 9* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Figure 18*) to latch new attenuation state into device.

For direct programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Table 5. Truth Table

P/S	C16	C8	C4	C2	C1	Attenuation State
0	0	0	0	0	0	Reference Loss
0	0	0	0	0	1	1 dB
0	0	0	0	1	0	2 dB
0	0	0	1	0	0	4 dB
0	0	1	0	0	0	8 dB
0	1	0	0	0	0	16 dB
0	1	1	1	1	1	31 dB

Note: Not all 32 possible combinations of C1-C16 are shown

Serial Interface
The PE4306's serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. The latch is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The stop bit (B0) of the data should always be low to prevent an unknown state in the device. The timing for this operation is defined by *Figure 17* (Serial Interface Timing Diagram) and *Table 8* (Serial Interface AC Characteristics).

Power-up Control Settings
The PE4306 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S = 1), the five control bits and a stop bit are set to whatever data is present on the five parallel data inputs (C1 to C16). This allows any one of the 32 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in *Table 6* (Power-Up Truth Table, Parallel Mode).

Table 6. Power-Up Truth Table, Parallel Interface Mode

P/S	LE	PUP2	PUP1	Attenuation State
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31 dB
0	1	X	X	Defined by **C1-C16**

Note: Power up with LE = 1 provides normal parallel operation with C1-C16, and PUP1 and PUP2 are not active.

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE4306 DSA.

J9 is used in conjunction with the supplied DC cable to supply V_{DD}, GND, and $-V_{DD}$. If use of the internal negative voltage generator is desired, then connect $-V_{DD}$ (black banana plug) to ground. If an external $-V_{DD}$ is desired, then apply -3V.

J1 should be connected to the LPT1 port of a PC with the supplied control cable. The evaluation software is written to operate the DSA in serial mode, so switch 7 (P/S) on the DIP switch SW1 should be ON with all other switches off. Using the software, enable or disable each attenuation setting to the desired combined attenuation. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

To evaluate the power up options, first disconnect the control cable from the evaluation board. The control cable must be removed to prevent the PC port from biasing the control pins.

During power up with P/S = 1 high and LE = 0 or P/S = 0 low and LE = 1, the default power-up signal attenuation is set to the value present on the five control bits on the five parallel data inputs (C1 to C16). This allows any one of the 32 attenuation settings to be specified as the power-up state.

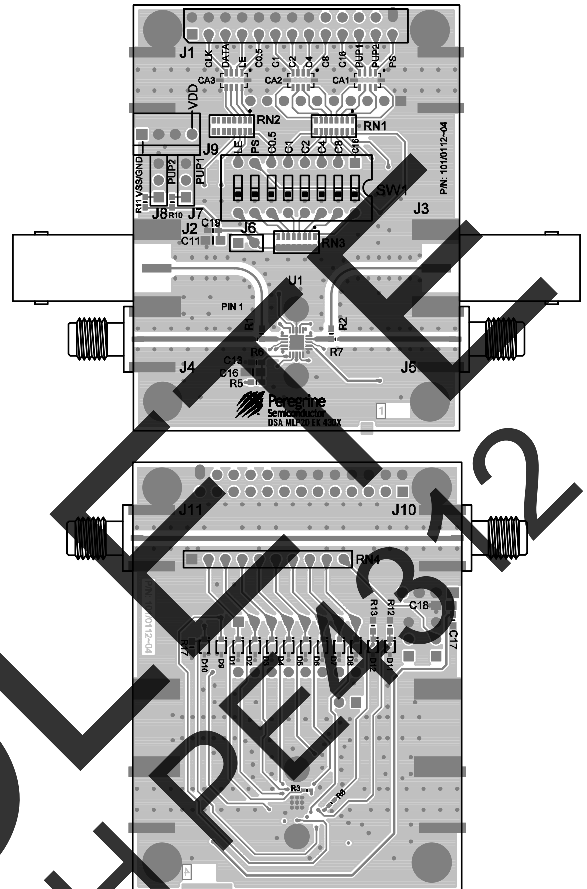
During power up with P/S = 0 high and LE = 0, the control bits are automatically set to one of four possible values presented through the PUP interface. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in the *Table 6*.

Pin 20 is open and can be connected to any bias.

Resistor on Pin 1 & 3

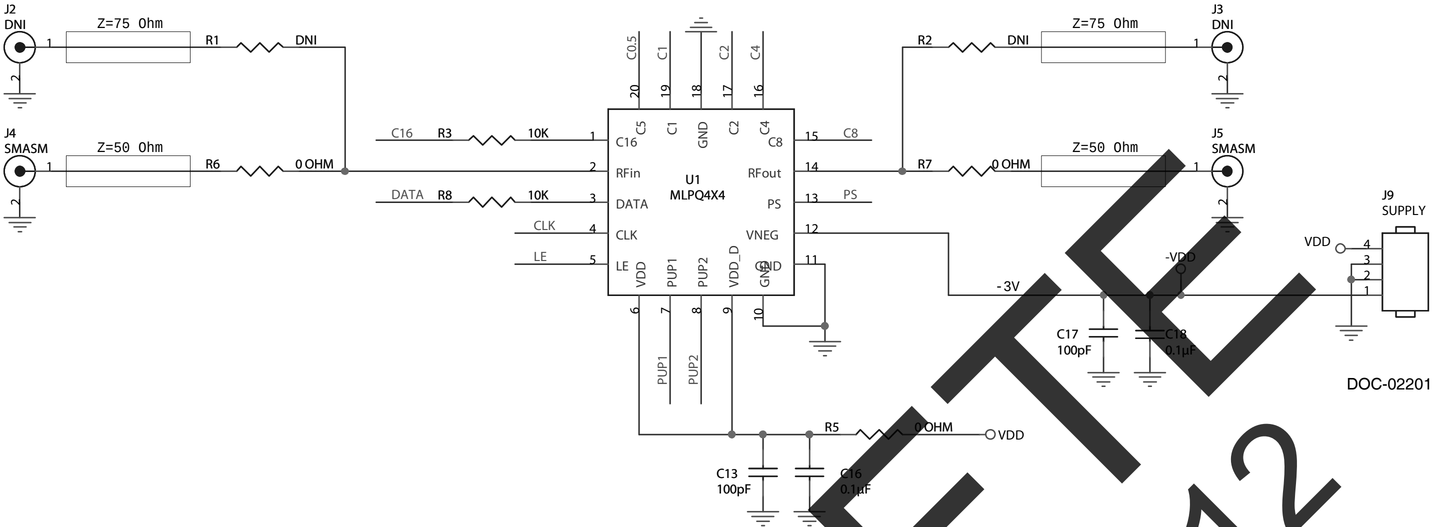
A 10 kΩ resistor on the inputs to pins 1 & 3 (Figure 16) will eliminate package resonance between the RF input pin and the two digital inputs. Specified attenuation error versus frequency performance is dependent upon this condition.

Figure 15. Evaluation Board Layout



DOC-02344

Figure 16. Evaluation Board Schematic



Note: Resistors on pins 1 and 3 are required and should be placed as close to the part as possible to avoid package resonance and meet error specifications over frequency

Figure 17. Serial Interface Timing Diagram

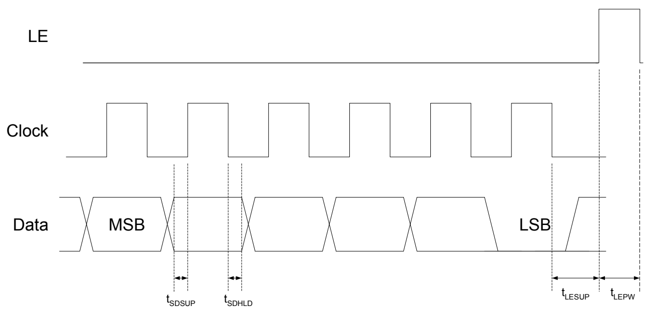


Table 7. 5-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	0

↑ MSB (first in) ↑ LSB (last in)

Note: The stop bit (B0) must always be low to prevent the attenuator from entering an unknown state.

Figure 18. Parallel Interface Timing Diagram

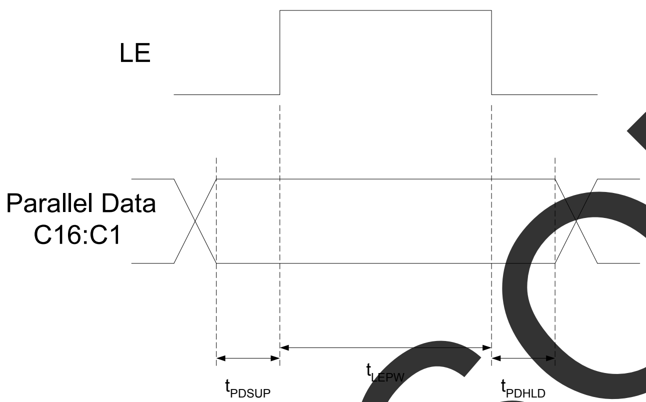


Table 8. Serial Interface AC Characteristics

V_{DD} = 3.0V, -40°C < T_A < 85°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
f_{Clk}	Serial data clock frequency (Note 1)		10	MHz
t_{ClkH}	Serial clock HIGH time	30		ns
t_{ClkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note 1: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification

Table 9. Parallel Interface AC Characteristics

V_{DD} = 3.0V, -40°C < T_A < 85°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Data set-up time before rising edge of LE	10		ns
t_{PDHLD}	Data hold time after falling edge of LE	10		ns

Figure 19. Package Drawing
20-lead 4 x 4 mm QFN

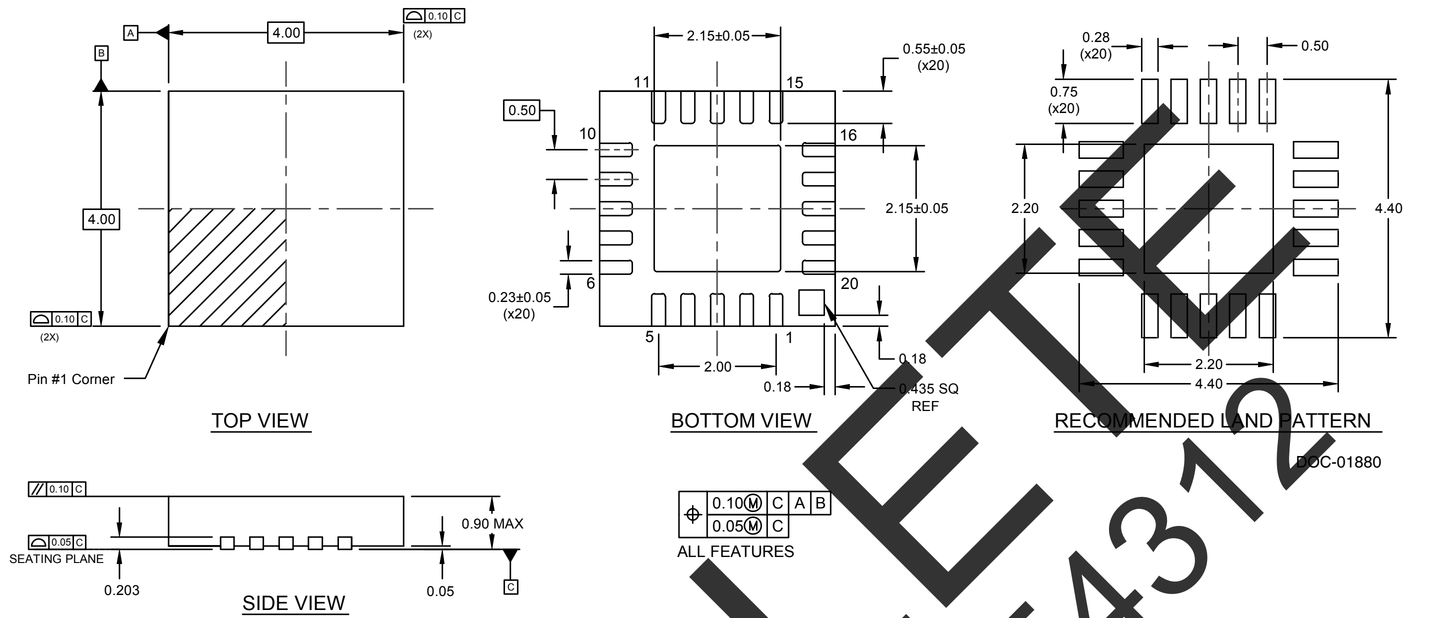
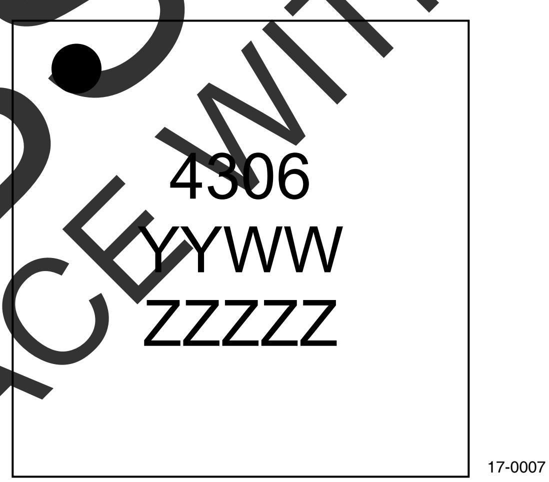
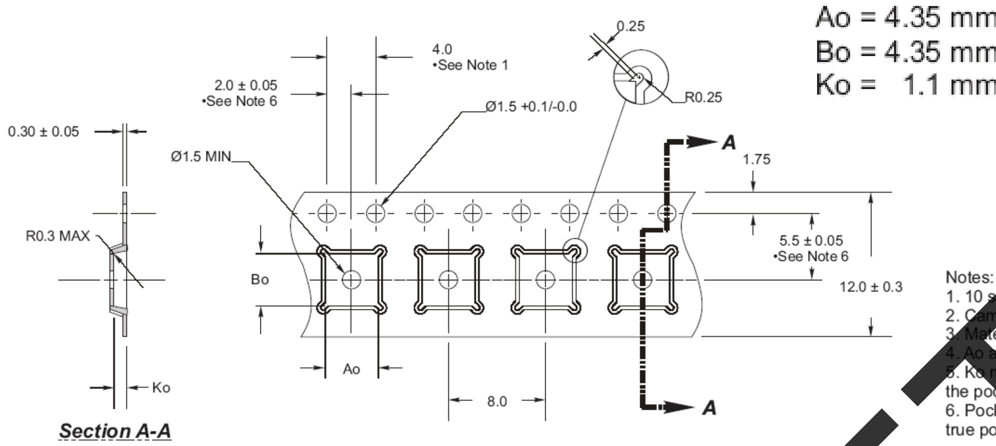


Figure 20. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of PSC Lot Number

Figure 21. Tape and Reel Drawing



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Table 10. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4306-00	PE4306-EK	PE4306-20MLP 4x4mm-EK	Evaluation Kit	1 / Box
4306-52	4306	PE4306G-20MLP 4x4mm-3000C	Green 20-lead 4x4mm QFN	3000 units / T&R

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. ***Preliminary Specification:*** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).
The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
The Peregrine name, logo, UltraCMOS and UTSi are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com.