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REVISION HISTORY

4/13—Rev. G to Rev. H

Combined Figure 2 and Figure 3; Combined Figure 4 and Figure 5	1
Changes to Figure 12	9

5/12—Rev. F to Rev. G

Deleted MSOP Throughout	1
Deleted Figure 2; Renumbered Sequentially	1
Deleted Spice-Macro Model Section	18
Updated Outline Dimensions	18
Changes to Ordering Guide	20

1/05—Rev. E to Rev. F

Changes to Absolute Maximum Ratings Table 4 and Table 5	6
Change to Figure 36	13
Changes to Ordering Guide	20

12/04—Rev. D to Rev. E

Updated Format	Universal
Changes to General Description	1
Changes to Specifications	3
Changes to Package Type	6
Change to Figure 16	8
Change to Figure 22	9
Change to Figure 36	13
Change to Figure 37	14
Changes to Ordering Guide	20

10/02—Rev. C to Rev. D

Deleted 8-Lead Plastic DIP (N-8)	Universal
Deleted 14-Lead Plastic DIP (N-14)	Universal
Edits to ORDERING GUIDE	19
Edits to Figure 30	19
Edits to Figure 31	19
Updated Outline Dimensions	19

SPECIFICATIONS

@ $V_S = 5.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}	OP162G, OP262G, OP462G −40°C ≤ T _A ≤ +125°C H grade, −40°C ≤ T _A ≤ +125°C D grade −40°C ≤ T _A ≤ +125°C		45 0.8	325 800 1 3 5	μV μV mV mV mV
Input Bias Current	I _B	−40°C ≤ T _A ≤ +125°C		360	600 650	nA nA
Input Offset Current	I _{OS}	−40°C ≤ T _A ≤ +125°C		±2.5	±25 ±40	nA nA
Input Voltage Range	V _{CM}		0		4	V
Common-Mode Rejection	CMRR	0 V ≤ V _{CM} ≤ 4.0 V, −40°C ≤ T _A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A _{VO}	R _L = 2 kΩ, 0.5 ≤ V _{OUT} ≤ 4.5 V		30		V/mV
		R _L = 10 kΩ, 0.5 ≤ V _{OUT} ≤ 4.5 V	65	88		V/mV
		R _L = 10 kΩ, −40°C ≤ T _A ≤ +125°C	40			V/mV
Long-Term Offset Voltage ¹	V _{OS}	G grade			600	μV
Offset Voltage Drift ²	ΔV _{OS} /ΔT			1		μV/°C
Bias Current Drift	ΔI _B /ΔT			250		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V _{OH}	I _L = 250 μA, −40°C ≤ T _A ≤ +125°C I _L = 5 mA	4.95 4.85	4.99 4.94		V V
Output Voltage Swing Low	V _{OL}	I _L = 250 μA, −40°C ≤ T _A ≤ +125°C I _L = 5 mA		14 65	50 150	mV mV
Short-Circuit Current	I _{SC}	Short to ground		±80		mA
Maximum Output Current	I _{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _S = 2.7 V to 7 V −40°C ≤ T _A ≤ +125°C	90	120		dB dB
Supply Current/Amplifier	I _{SY}	OP162, V _{OUT} = 2.5 V −40°C ≤ T _A ≤ +125°C		600	750	μA mA
		OP262, OP462, V _{OUT} = 2.5 V −40°C ≤ T _A ≤ +125°C		500	700	μA μA
					850	
DYNAMIC PERFORMANCE						
Slew Rate	SR	1 V < V _{OUT} < 4 V, R _L = 10 kΩ		10		V/μs
Settling Time	t _S	To 0.1%, A _V = −1, V _O = 2 V step		540		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	φ _m			61		Degrees
NOISE PERFORMANCE						
Voltage Noise	e _n p-p	0.1 Hz to 10 Hz		0.5		μV p-p
Voltage Noise Density	e _n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i _n	f = 1 kHz		0.4		pA/√Hz

¹ Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125°C , with an LTPD of 1.3.

² Offset voltage drift is the average of the -40°C to $+25^\circ\text{C}$ delta and the $+25^\circ\text{C}$ to $+125^\circ\text{C}$ delta.

@ $V_S = 3.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}	OP162G, OP262G, OP462G G, H grades, −40°C ≤ T _A ≤ +125°C D grade −40°C ≤ T _A ≤ +125°C		50 0.8	325 1 3 5	μV mV mV mV
Input Bias Current	I _B			360	600	nA
Input Offset Current	I _{OS}			±2.5	±25	nA
Input Voltage Range	V _{CM}		0		2	V
Common-Mode Rejection	CMRR	0 V ≤ V _{CM} ≤ 2.0 V, −40°C ≤ T _A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A _{VO}	R _L = 2 kΩ, 0.5 V ≤ V _{OUT} ≤ 2.5 V		20		V/mV
		R _L = 10 kΩ, 0.5 V ≤ V _{OUT} ≤ 2.5 V	20	30		V/mV
Long-Term Offset Voltage ¹	V _{OS}	G grade			600	μV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V _{OH}	I _L = 250 μA	2.95	2.99		V
Output Voltage Swing Low	V _{OL}	I _L = 5 mA	2.85	2.93		V
		I _L = 250 μA		14	50	mV
		I _L = 5 mA		66	150	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _S = 2.7 V to 7 V, −40°C ≤ T _A ≤ +125°C	60	110		dB
Supply Current/Amplifier	I _{SY}	OP162, V _{OUT} = 1.5 V		600	700	μA
		−40°C ≤ T _A ≤ +125°C			1	mA
		OP262, OP462, V _{OUT} = 1.5 V		500	650	μA
		−40°C ≤ T _A ≤ +125°C			850	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L = 10 kΩ		10		V/μs
Settling Time	t _s	To 0.1%, A _V = −1, V _O = 2 V step		575		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	φ _m			59		Degrees
NOISE PERFORMANCE						
Voltage Noise	e _n p-p	0.1 Hz to 10 Hz		0.5		μV p-p
Voltage Noise Density	e _n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i _n	f = 1 kHz		0.4		pA/√Hz

¹ Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125°C , with an LTPD of 1.3.

@ $V_S = \pm 5.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}	OP162G, OP262G, OP462G		25	325	μV
		−40°C ≤ T _A ≤ +125°C			800	μV
		H grade, −40°C ≤ T _A ≤ +125°C			1	mV
		D grade	0.8	3	mV	
		−40°C ≤ T _A ≤ +125°C			5	mV
Input Bias Current	I _B	−40°C ≤ T _A ≤ +125°C		260	500	nA
Input Offset Current	I _{OS}				650	nA
		−40°C ≤ T _A ≤ +125°C		±2.5	±25	nA
Input Voltage Range	V _{CM}		−5		±40	nA
					+4	V
Common-Mode Rejection	CMRR	−4.9 V ≤ V _{CM} ≤ +4.0 V, −40°C ≤ T _A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A _{VO}	R _L = 2 kΩ, −4.5 V ≤ V _{OUT} ≤ +4.5 V		35		V/mV
		R _L = 10 kΩ, −4.5 V ≤ V _{OUT} ≤ +4.5 V	75	120		V/mV
		−40°C ≤ T _A ≤ +125°C	25			V/mV
Long-Term Offset Voltage ¹	V _{OS}	G grade			600	μV
Offset Voltage Drift ²	ΔV _{OS} /ΔT			1		μV/°C
Bias Current Drift	ΔI _B /ΔT			250		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V _{OH}	I _L = 250 μA, −40°C ≤ T _A ≤ +125°C	4.95	4.99		V
		I _L = 5 mA	4.85	4.94		V
Output Voltage Swing Low	V _{OL}	I _L = 250 μA, −40°C ≤ T _A ≤ +125°C		−4.99	−4.95	V
		I _L = 5 mA		−4.94	−4.85	V
Short-Circuit Current	I _{SC}	Short to ground		±80		mA
Maximum Output Current	I _{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _S = ±1.35 V to ±6 V, −40°C ≤ T _A ≤ +125°C	60	110		dB
Supply Current/Amplifier	I _{SY}	OP162, V _{OUT} = 0 V		650	800	μA
		−40°C ≤ T _A ≤ +125°C			1.15	mA
		OP262, OP462, V _{OUT} = 0 V		550	775	μA
		−40°C ≤ T _A ≤ +125°C			1	mA
Supply Voltage Range	V _S		3.0 (±1.5)		12 (±6)	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	−4 V < V _{OUT} < 4 V, R _L = 10 kΩ		13		V/μs
Settling Time	t _S	To 0.1%, A _V = −1, V _O = 2 V step		475		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	φ _m			64		Degrees
NOISE PERFORMANCE						
Voltage Noise	e _n p-p	0.1 Hz to 10 Hz		0.5		μV p-p
Voltage Noise Density	e _n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i _n	f = 1 kHz		0.4		pA/√Hz

¹ Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at $+125^\circ\text{C}$, with an LTPD of 1.3.

² Offset voltage drift is the average of the -40°C to $+25^\circ\text{C}$ delta and the $+25^\circ\text{C}$ to $+125^\circ\text{C}$ delta.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Min
Supply Voltage	± 6 V
Input Voltage ¹	± 6 V
Differential Input Voltage ²	± 0.6 V
Internal Power Dissipation	
SOIC (S)	Observe Derating Curves
TSSOP (RU)	Observe Derating Curves
Output Short-Circuit Duration	Observe Derating Curves
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 10 sec)	300°C

¹ For supply voltages greater than 6 V, the input voltage is limited to less than or equal to the supply voltage.

² For differential input voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5.

Package Type	θ_{JA} ¹	θ_{JC}	Unit
8-Lead SOIC (S)	157	56	$^{\circ}\text{C}/\text{W}$
8-Lead TSSOP (RU)	208		$^{\circ}\text{C}/\text{W}$
14-Lead SOIC (S)	105		$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU)	148		$^{\circ}\text{C}/\text{W}$

¹ θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in circuit board for SOIC, and TSSOP packages.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

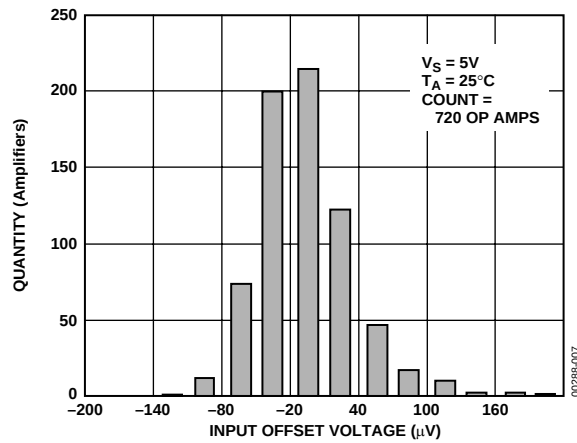


Figure 4. OP462 Input Offset Voltage Distribution

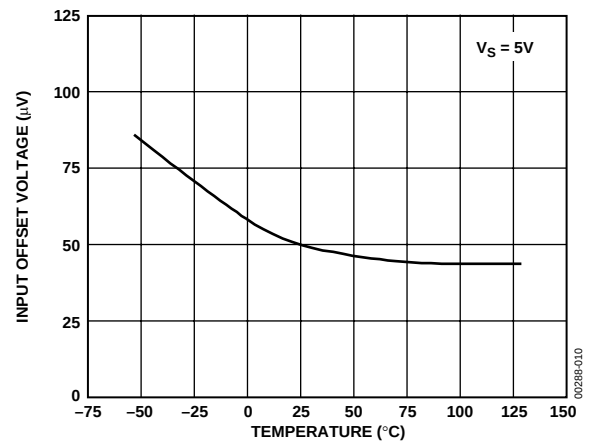


Figure 7. OP462 Input Offset Voltage vs. Temperature

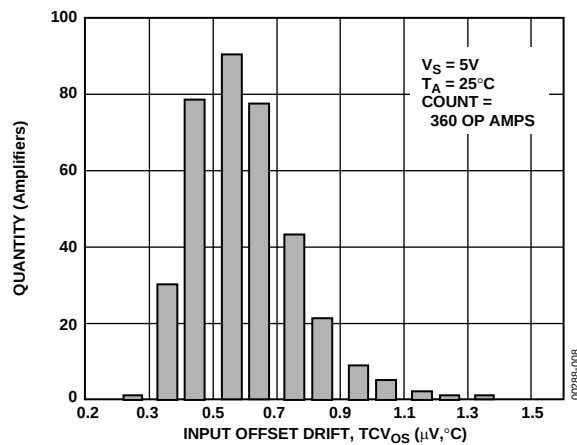
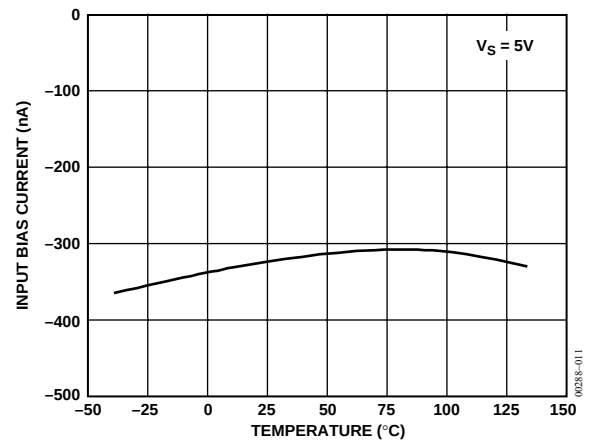
Figure 5. OP462 Input Offset Voltage Drift (TCV_{OS})

Figure 8. OP462 Input Bias Current vs. Temperature

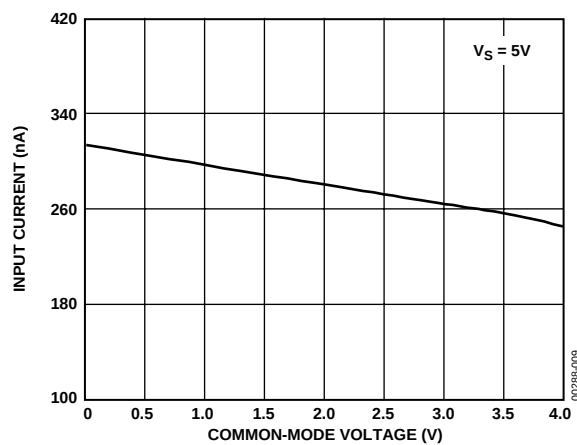


Figure 6. OP462 Input Bias Current vs. Common-Mode Voltage

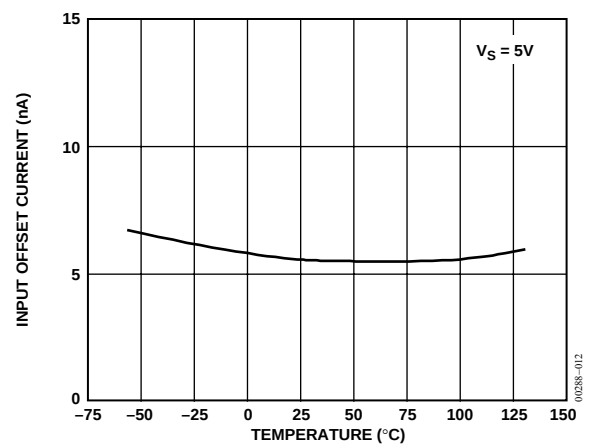


Figure 9. OP462 Input Offset Current vs. Temperature

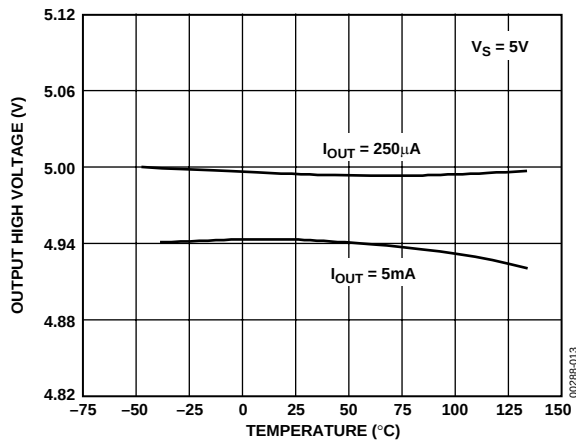


Figure 10. OP462 Output High Voltage vs. Temperature

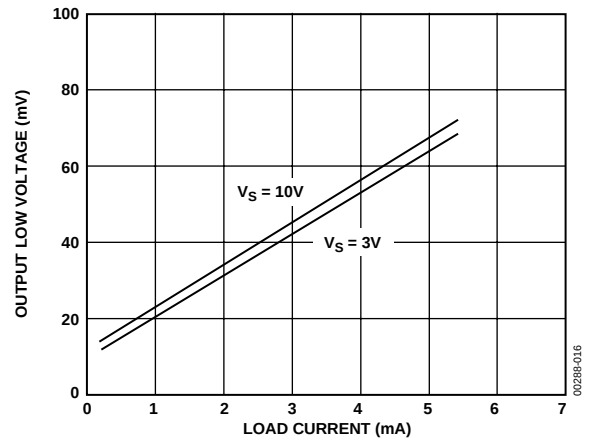


Figure 13. Output Low Voltage to Supply Rail vs. Load Current

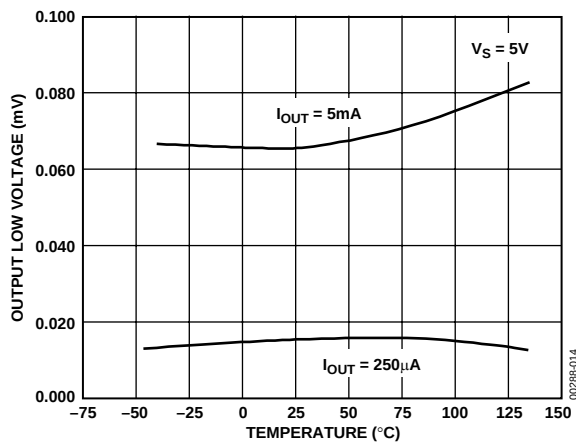


Figure 11. OP462 Output Low Voltage vs. Temperature

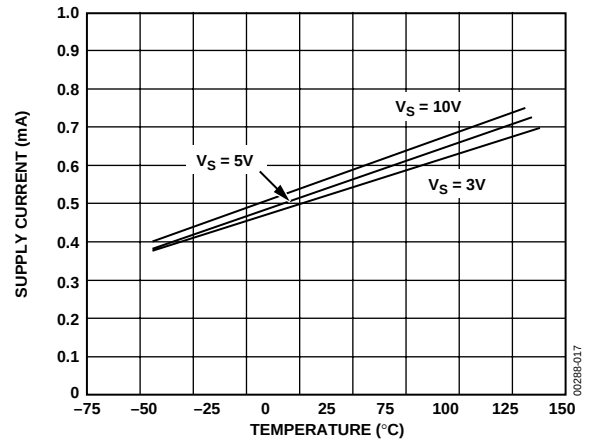


Figure 14. Supply Current/Amplifier vs. Temperature

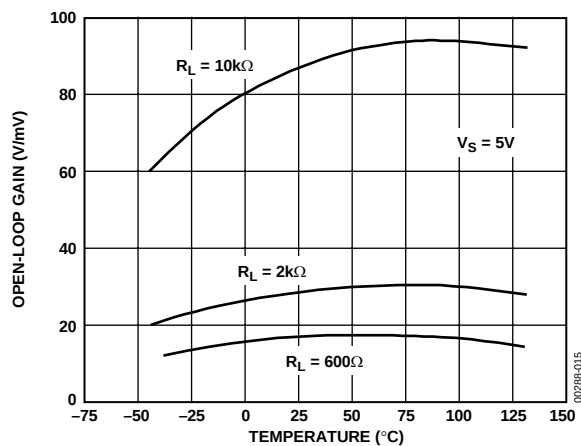


Figure 12. OP462 Open-Loop Gain vs. Temperature

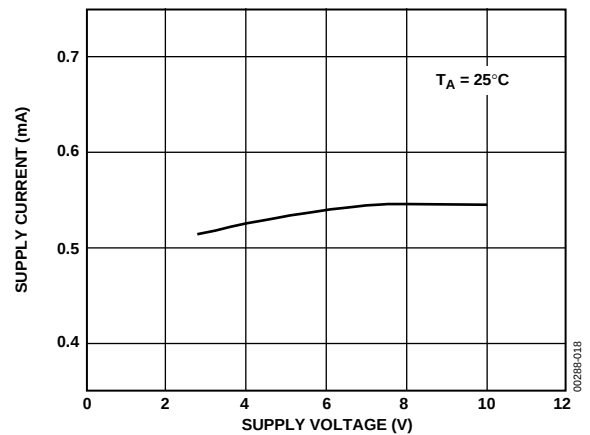


Figure 15. OP462 Supply Current/Amplifier vs. Supply Voltage

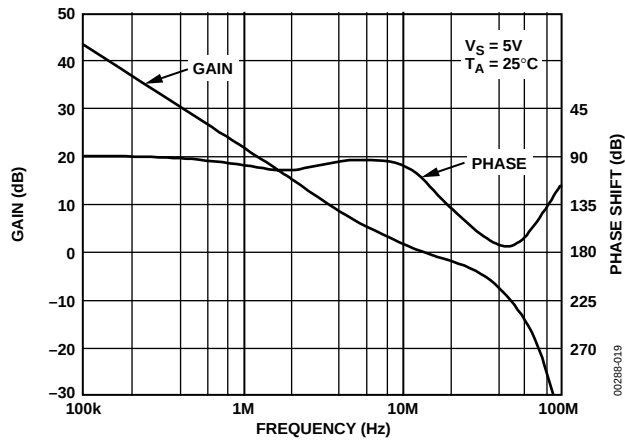


Figure 16. Open-Loop Gain and Phase vs. Frequency (No Load)

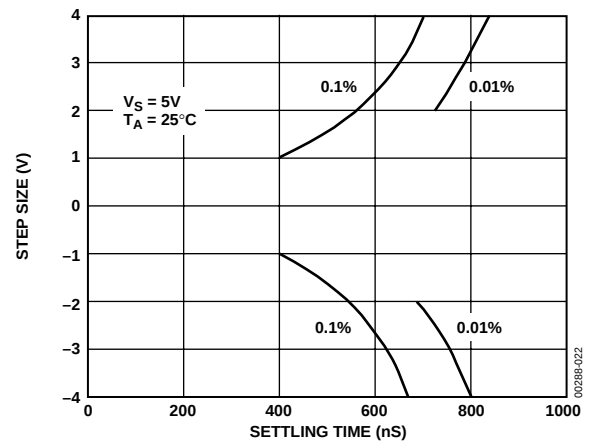


Figure 19. Step Size vs. Settling Time

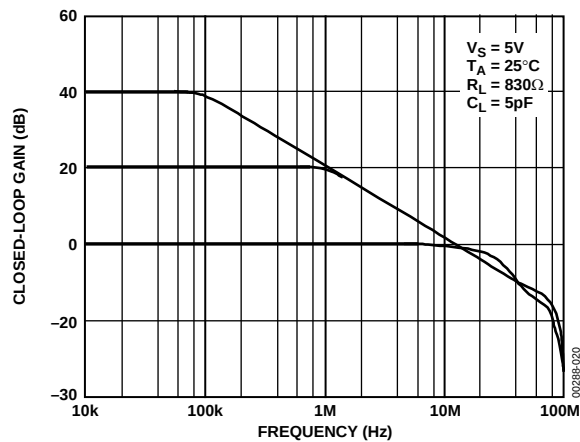


Figure 17. Closed-Loop Gain vs. Frequency

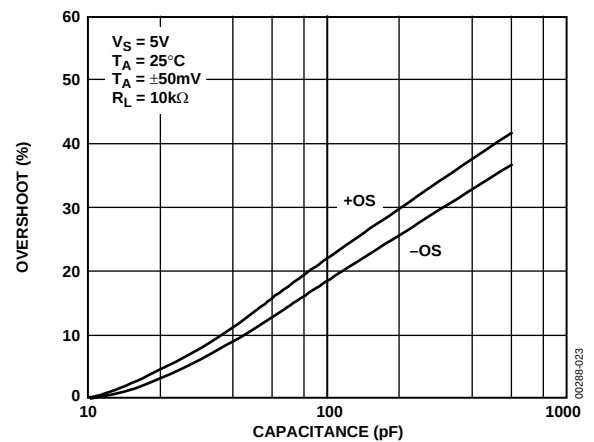


Figure 20. Small-Signal Overshoot vs. Capacitance

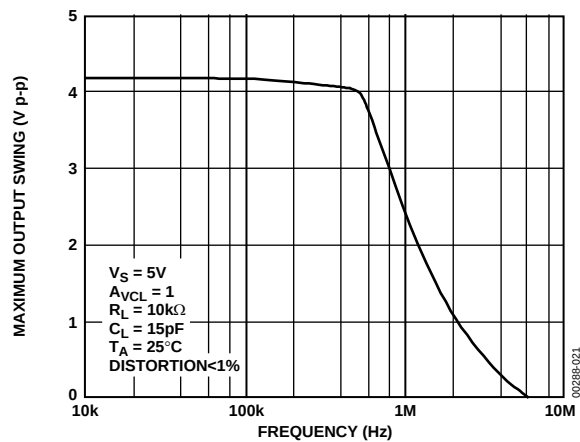


Figure 18. Maximum Output Swing vs. Frequency

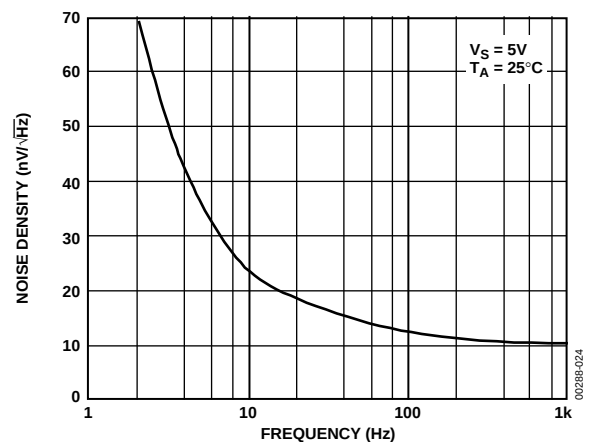


Figure 21. Voltage Noise Density vs. Frequency

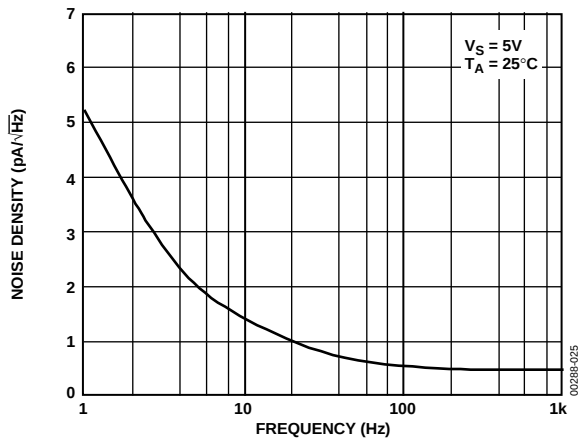


Figure 22. Current Noise Density vs. Frequency

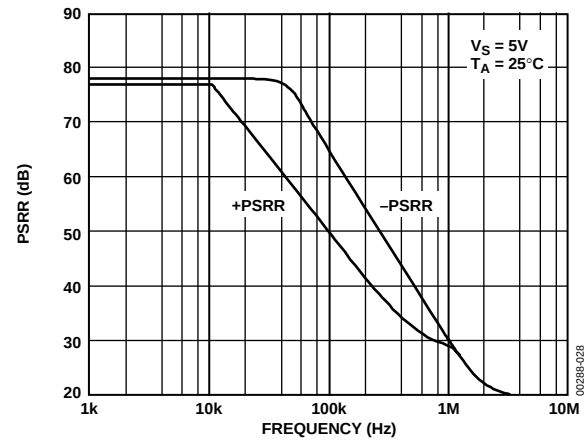


Figure 25. PSRR vs. Frequency

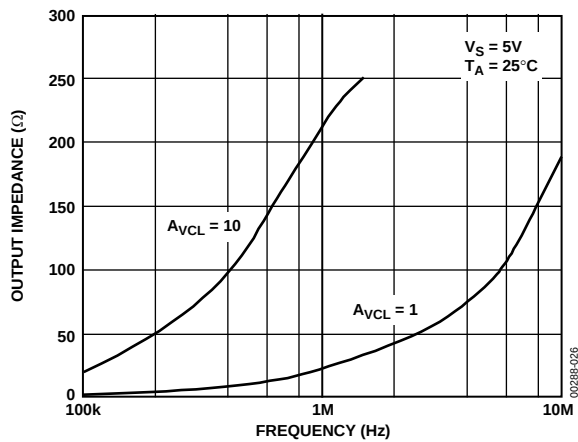


Figure 23. Output Impedance vs. Frequency

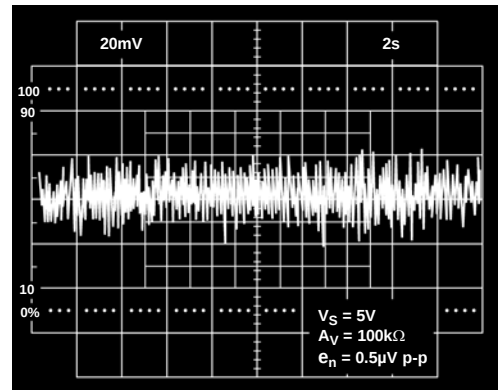


Figure 26. 0.1 Hz to 10 Hz Noise

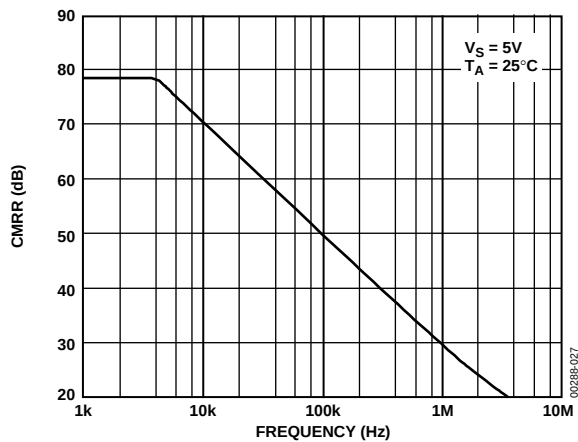


Figure 24. CMRR vs. Frequency

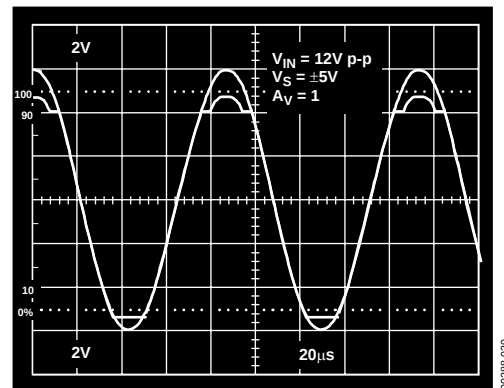


Figure 27. No Phase Reversal ($V_{IN} = 12V$ p-p, $V_S = \pm 5V$, $A_V = 1$)

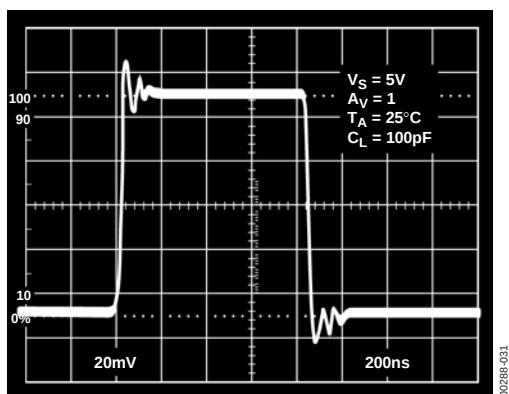


Figure 28. Small Signal Transient Response

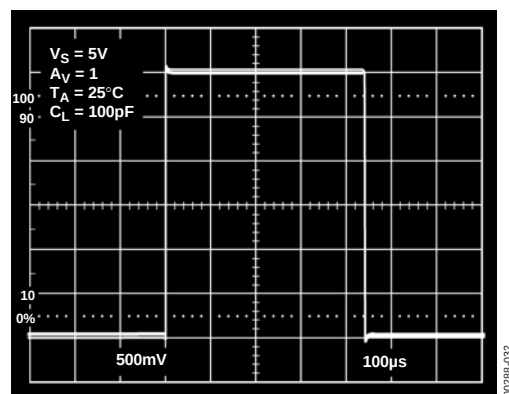


Figure 29. Large Signal Transient Response

APPLICATIONS

FUNCTIONAL DESCRIPTION

The OPx62 family is fabricated using Analog Devices' high speed complementary bipolar process, also called XFCB. This process trench isolates each transistor to lower parasitic capacitances for high speed performance. This high speed process has been implemented without sacrificing the excellent transistor matching and overall dc performance characteristic of Analog Devices' complementary bipolar process. This makes the OPx62 family an excellent choice as an extremely fast and accurate low voltage op amp.

Figure 30 shows a simplified equivalent schematic for the OP162. A PNP differential pair is used at the input of the device. The cross connecting of the emitters lowers the transconductance of the input stage improving the slew rate of the device. Lowering the transconductance through cross connecting the emitters has another advantage in that it provides a lower noise factor than if emitter degeneration resistors were used. The input stage can function with the base voltages taken all the way to the negative power supply, or up to within 1 V of the positive power supply.

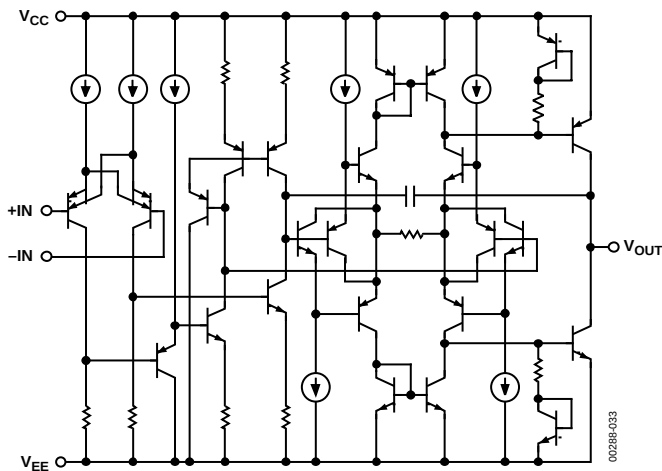


Figure 30. Simplified Schematic

Two complementary transistors in a common-emitter configuration are used for the output stage. This allows the output of the device to swing to within 50 mV of either supply rail at load currents less than 1 mA. As load current increases, the maximum voltage swing of the output decreases. This is due to the collector-to-emitter saturation voltages of the output transistors increasing. The gain of the output stage, and consequently the open-loop gain of the amplifier, is dependent on the load resistance connected at the output. Because the dominant pole frequency is inversely proportional to the open-loop gain, the unity-gain bandwidth of the device is not affected by the load resistance. This is typically the case in rail-to-rail output devices.

OFFSET ADJUSTMENT

Because the OP162/OP262/OP462 have an exceptionally low typical offset voltage, adjustment to correct offset voltage may not be needed. However, the OP162 has pinouts to attach a nulling resistor. Figure 31 shows how the OP162 offset voltage can be adjusted by connecting a potentiometer between Pin 1 and Pin 8, and connecting the wiper to V_{CC} . It is important to avoid accidentally connecting the wiper to V_{EE} , as this can damage the device. The recommended value for the potentiometer is 20 k Ω .

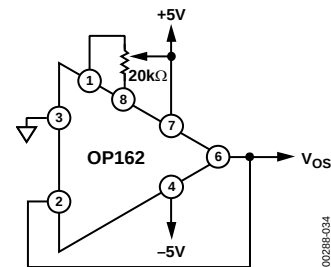


Figure 31. Offset Adjustment Schematic

RAIL-TO-RAIL OUTPUT

The OP162/OP262/OP462 have a wide output voltage range that extends to within 60 mV of each supply rail with a load current of 5 mA. Decreasing the load current extends the output voltage range even closer to the supply rails. The common-mode input range extends from ground to within 1 V of the positive supply. It is recommended that there be some minimal amount of gain when a rail-to-rail output swing is desired. The minimum gain required is based on the supply voltage and can be found as

$$A_{V,min} = \frac{V_s}{V_s - 1}$$

where V_s is the positive supply voltage. With a single-supply voltage of 5 V, the minimum gain to achieve rail-to-rail output should be 1.25.

OUTPUT SHORT-CIRCUIT PROTECTION

To achieve a wide bandwidth and high slew rate, the output of the OP162/OP262/OP462 are not short-circuit protected. Shorting the output directly to ground or to a supply rail may destroy the device. The typical maximum safe output current is ± 30 mA. Steps should be taken to ensure the output of the device will not be forced to source or sink more than 30 mA.

In applications where some output current protection is needed, but not at the expense of reduced output voltage headroom, a low value resistor in series with the output can be used. This is shown in Figure 32. The resistor is connected within the feedback loop of the amplifier so that if V_{OUT} is shorted to ground

and V_{IN} swings up to 5 V, the output current will not exceed 30 mA. For single 5 V supply applications, resistors less than 169 Ω are not recommended.

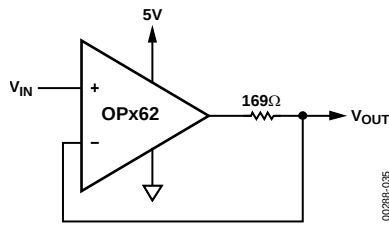


Figure 32. Output Short-Circuit Protection

INPUT OVERVOLTAGE PROTECTION

The input voltage should be limited to ± 6 V, or damage to the device can occur. Electrostatic protection diodes placed in the input stage of the device help protect the amplifier from static discharge. Diodes are connected between each input as well as from each input to both supply pins as shown in the simplified equivalent circuit in Figure 30. If an input voltage exceeds either supply voltage by more than 0.6 V, or if the differential input voltage is greater than 0.6 V, these diodes energize causing overvoltage damage.

The input current should be limited to less than 5 mA to prevent degradation or destruction of the device by placing an external resistor in series with the input at risk of being overdriven. The size of the resistor can be calculated by dividing the maximum input voltage by 5 mA. For example, if the differential input voltage could reach 5 V, the external resistor should be $5 \text{ V} / 5 \text{ mA} = 1 \text{ k}\Omega$. In practice, this resistor should be placed in series with both inputs to balance any offset voltages created by the input bias current.

OUTPUT PHASE REVERSAL

The OP162/OP262/OP462 are immune to phase reversal as long as the input voltage is limited to ± 6 V. Figure 27 shows the output of a device with the input voltage driven beyond the supply voltages. Although the device's output does not change phase, large currents due to input overvoltage could result, damaging the device. In applications where the possibility of an input voltage exceeding the supply voltage exists, overvoltage protection should be used, as described in the previous section.

POWER DISSIPATION

The maximum power that can be safely dissipated by the OP162/OP262/OP462 is limited by the associated rise in junction temperature. The maximum safe junction temperature is 150°C; device performance suffers when this limit is exceeded. If this maximum is only momentarily exceeded, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in an "overheated" condition for an extended period can result in permanent damage to the device.

To calculate the internal junction temperature of the OPx62, use the formula

$$T_J = P_{DISS} \times \theta_{JA} + T_A$$

where:

T_J is the OPx62 junction temperature.

P_{DISS} is the OPx62 power dissipation.

θ_{JA} is the OPx62 package thermal resistance, junction-to-ambient temperature.

T_A is the ambient temperature of the circuit.

The power dissipated by the device can be calculated as

$$P_{DISS} = I_{LOAD} \times (V_S - V_{OUT})$$

where:

I_{LOAD} is the OPx62 output load current.

V_S is the OPx62 supply voltage.

V_{OUT} is the OPx62 output voltage.

Figure 33 and Figure 34 provide a convenient way to determine if the device is being overheated. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature around the package. By using the previous equation, it is a simple matter to see if P_{DISS} exceeds the device's power derating curve. To ensure proper operation, it is important to observe the recommended derating curves shown in Figure 33 and Figure 34.

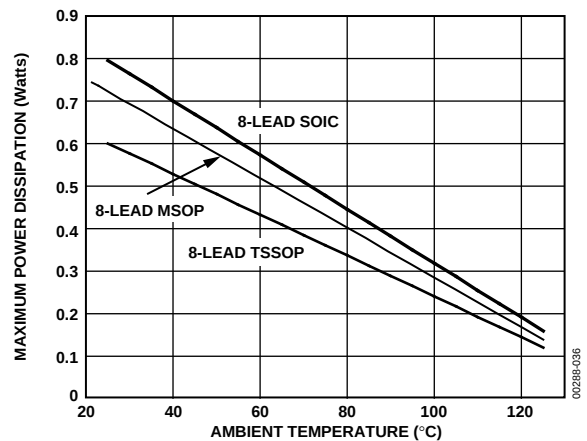


Figure 33. Maximum Power Dissipation vs. Temperature for 8-Lead Package Types

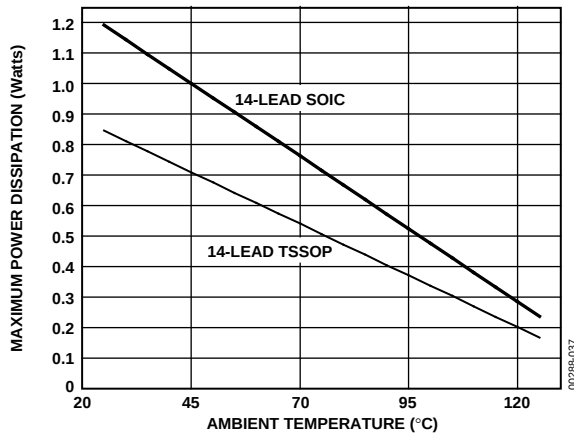


Figure 34. Maximum Power Dissipation vs. Temperature for 14-Lead Package Types

UNUSED AMPLIFIERS

It is recommended that any unused amplifiers in a dual or a quad package be configured as a unity-gain follower with a 1 k Ω feedback resistor connected from the inverting input to the output, and the noninverting input tied to the ground plane.

POWER-ON SETTLING TIME

The time it takes for the output of an op amp to settle after a supply voltage is delivered can be an important consideration in some power-up-sensitive applications. An example of this would be in an A/D converter where the time until valid data can be produced after power-up is important.

The OPx62 family has a rapid settling time after power-up. Figure 35 shows the OP462 output settling times for a single-supply voltage of $V_S = +5$ V. The test circuit in Figure 36 was used to find the power-on settling times for the device.

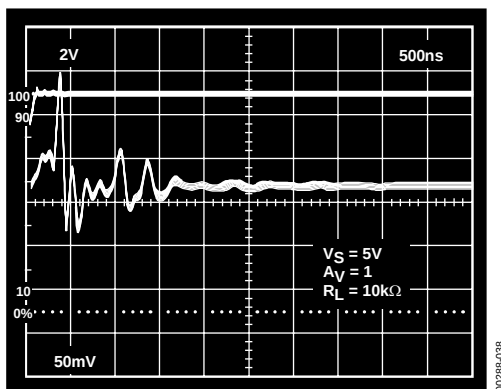


Figure 35. Oscilloscope Photo of V_S and V_{OUT}

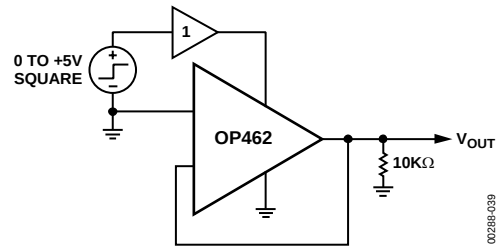


Figure 36. Test Circuit for Power-On Settling Time

CAPACITIVE LOAD DRIVE

The OP162/OP262/OP462 are high speed, extremely accurate devices that tolerate some capacitive loading at their outputs. As load capacitance increases, unity-gain bandwidth of an OPx62 device decreases. This also causes an increase in overshoot and settling time for the output. Figure 38 shows an example of this with the device configured for unity gain and driving a 10 k Ω resistor and 300 pF capacitor placed in parallel.

By connecting a series R-C network, commonly called a “snubber” network, from the output of the device to ground, this ringing can be eliminated and overshoot can be significantly reduced. Figure 37 shows how to set up the snubber network, and Figure 39 shows the improvement in output response with the network added.

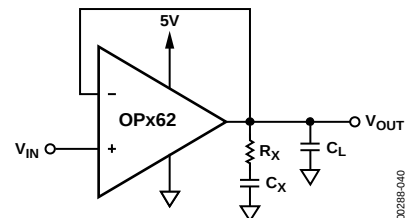


Figure 37. Snubber Network Compensation for Capacitive Loads

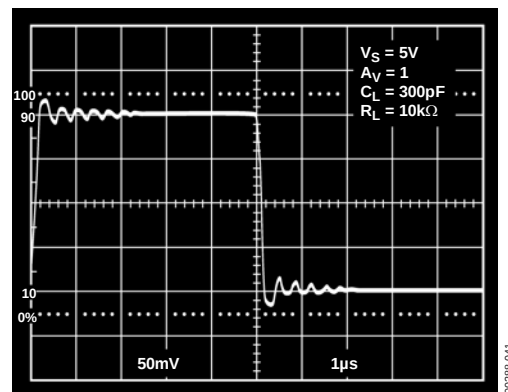


Figure 38. A Photo of a Ringing Square Wave

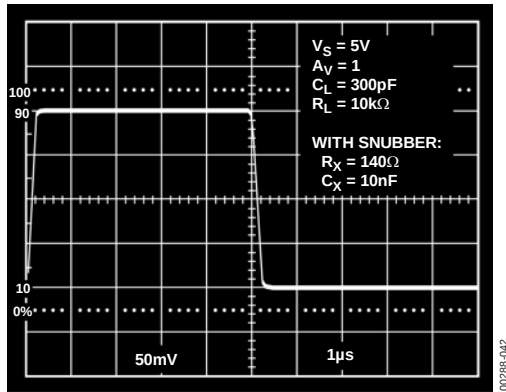


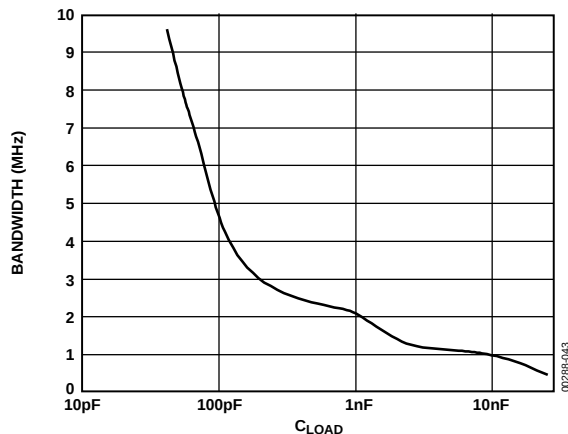
Figure 39. A Photo of a Nice Square Wave at the Output

The network operates in parallel with the load capacitor, C_L , and provides compensation for the added phase lag. The actual values of the network resistor and capacitor are empirically determined to minimize overshoot and maximize unity-gain bandwidth. Table 6 shows a few sample snubber networks for large load capacitors.

Table 6. Snubber Networks for Large Capacitive Loads

C_{LOAD}	R_X	C_X
< 300 pF	140 Ω	10 nF
500 pF	100 Ω	10 nF
1 nF	80 Ω	10 nF
10 nF	10 Ω	47 nF

Higher load capacitance will reduce the unity-gain bandwidth of the device. Figure 40 shows unity-gain bandwidth vs. capacitive load. The snubber network does not provide any increase in bandwidth, but it substantially reduces ringing and overshoot, as shown between Figure 38 and Figure 39.

Figure 40. Unity-Gain Bandwidth vs. C_{LOAD}

TOTAL HARMONIC DISTORTION AND CROSSTALK

The OPx62 device family offers low total harmonic distortion making it an excellent choice for audio applications. Figure 41 shows a graph of THD plus noise figures at 0.001% for the OP462.

Figure 42 shows the worst case crosstalk between two amplifiers in the OP462. A 1 V rms signal is applied to one amplifier while measuring the output of an adjacent amplifier. Both amplifiers are configured for unity gain and supplied with ± 2.5 V.

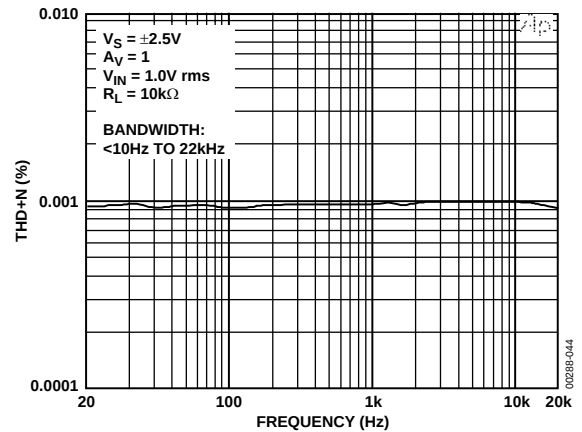


Figure 41. THD + N vs. Frequency

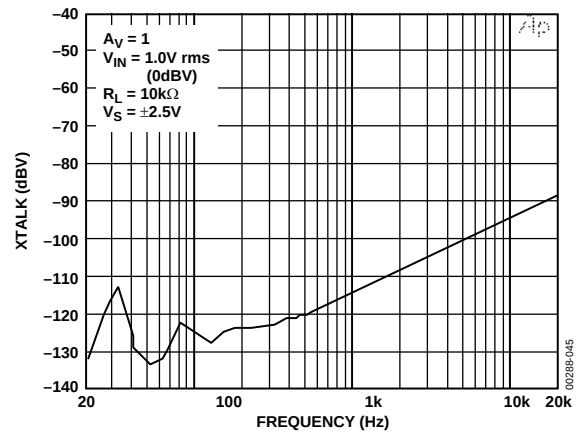


Figure 42. Crosstalk vs. Frequency

PCB LAYOUT CONSIDERATIONS

Because the OP162/OP262/OP462 can provide gains at high frequency, careful attention to board layout and component selection is recommended. As with any high speed application, a good ground plane is essential to achieve the optimum performance. This can significantly reduce the undesirable effects of ground loops and $I \times R$ losses by providing a low impedance reference point. Best results are obtained with a multilayer board design with one layer assigned to ground plane.

Use chip capacitors for supply bypassing, with one end of the capacitor connected to the ground plane and the other end connected within 1/8 inch of each power pin. An additional large tantalum electrolytic capacitor (4.7 μ F to 10 μ F) should be connected in parallel. This capacitor provides current for fast, large-signal changes at the device's output; therefore, it does not need to be placed as close to the supply pins.

APPLICATIONS CIRCUITS

SINGLE-SUPPLY STEREO HEADPHONE DRIVER

Figure 43 shows a stereo headphone output amplifier that can operate from a single 5 V supply. The reference voltage is derived by dividing the supply voltage down with two 100 kΩ resistors. A 10 μF capacitor prevents power supply noise from contaminating the audio signal and establishes an ac ground for the volume control potentiometers.

The audio signal is ac-coupled to each noninverting input through a 10 μF capacitor. The gain of the amplifier is controlled by the feedback resistors and is $(R_2/R_1) + 1$. For this example, the gain is 6. By removing R_1 , the amplifier would have unity gain. To short-circuit protect the output of the device, a 169 Ω resistor is placed at the output in the feedback network. This prevents any damage to the device if the headphone output becomes shorted. A 270 μF capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of headphones, which can range from 32 Ω to 600 Ω or more.

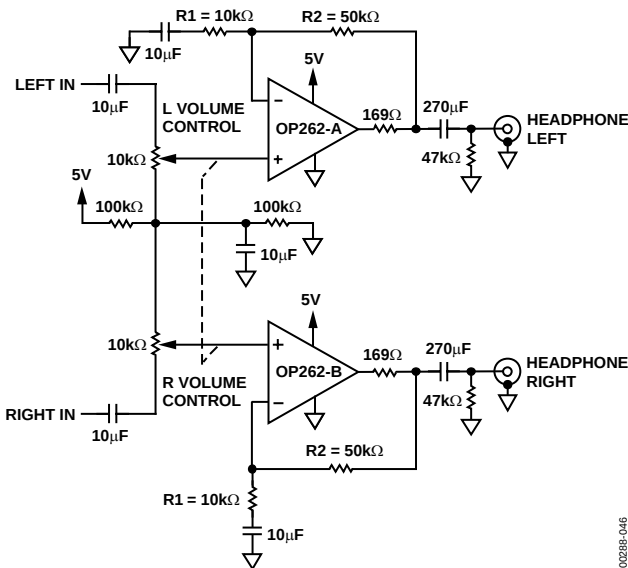


Figure 43. Headphone Output Amplifier

INSTRUMENTATION AMPLIFIER

Because of their high speed, low offset voltages, and low noise characteristics, the OP162/OP262/OP462 can be used in a wide variety of high speed applications, including precision instrumentation amplifiers. Figure 44 shows an example of such an application.

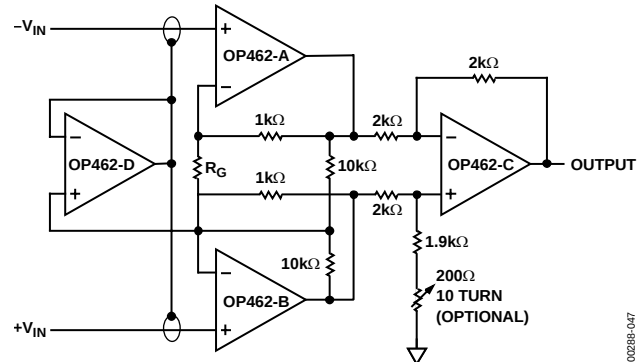


Figure 44. High Speed Instrumentation Amplifier

The differential gain of the circuit is determined by R_G , where

$$A_{DIFF} = 1 + \frac{2}{R_G}$$

with the R_G resistor value in kΩ. Removing R_G sets the circuit gain to unity.

The fourth op amp, OP462-D, is optional and is used to improve CMRR by reducing any input capacitance to the amplifier. By shielding the input signal leads and driving the shield with the common-mode voltage, input capacitance is eliminated at common-mode voltages. This voltage is derived from the midpoint of the outputs of OP462-A and OP462-B by using two 10 kΩ resistors followed by OP462-D as a unity-gain buffer.

It is important to use 1% or better tolerance components for the 2 kΩ resistors, as the common-mode rejection is dependent on their ratios being exact. A potentiometer should also be connected in series with the OP462-C noninverting input resistor to ground to optimize common-mode rejection.

The circuit in Figure 44 was implemented to test its settling time. The instrumentation amp was powered with -5 V, so the input step voltage went from -5 V to +4 V to keep the OP462 within its input range. Therefore, the 0.05% settling range is when the output is within 4.5 mV. Figure 45 shows the positive slope settling time to be 1.8 μs, and Figure 46 shows a settling time of 3.9 μs for the negative slope.

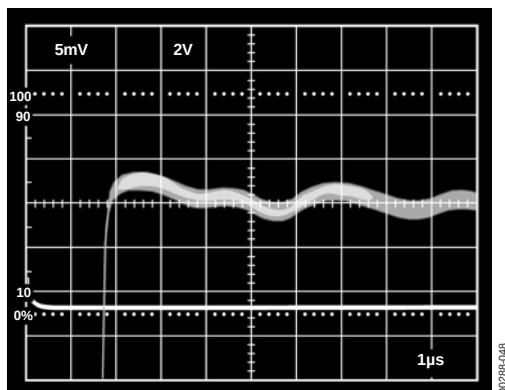


Figure 45. Positive Slope Settling Time

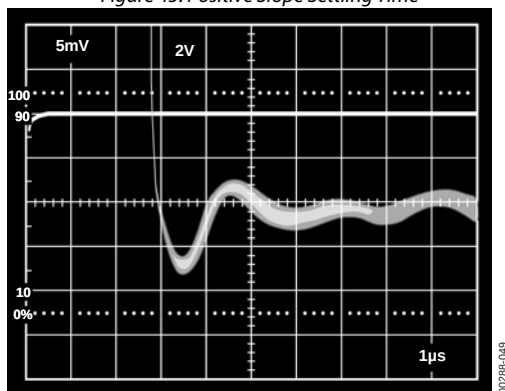


Figure 46. Negative Slope Settling Time

DIRECT ACCESS ARRANGEMENT

Figure 47 shows a schematic for a 5 V single-supply transmit/receive telephone line interface for 600 Ω transmission systems. It allows full-duplex transmission of signals on a transformer-coupled 600 Ω line. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible differential signal to the transformer. The largest signal available on a single 5 V supply is approximately 4.0 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier to extract the receive information from the transmission line for amplification by A4. A3 also prevents the transmit signal from interfering with the receive signal. The gain of A4 can be adjusted in the same manner as A1 to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (single in-line package) format resistor arrays. Couple this with the OP462 14-lead SOIC or TSSOP package and this circuit offers a compact solution.

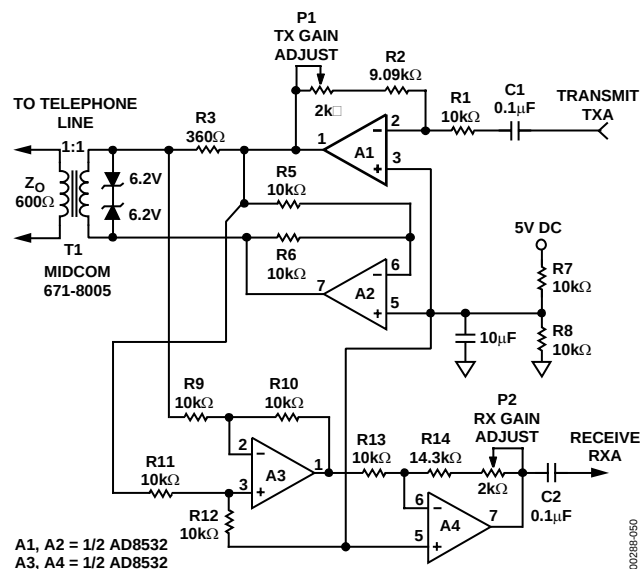
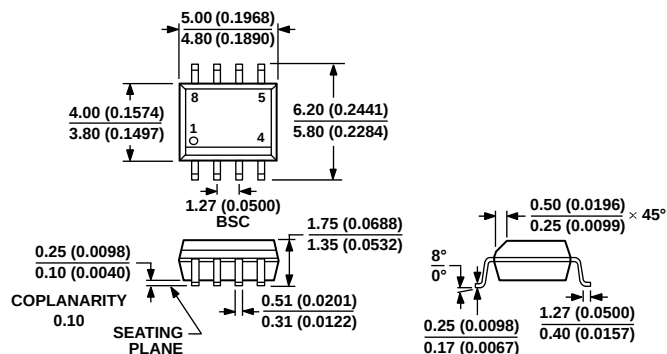


Figure 47. Single-Supply Direct Access Arrangement for Modems

OUTLINE DIMENSIONS

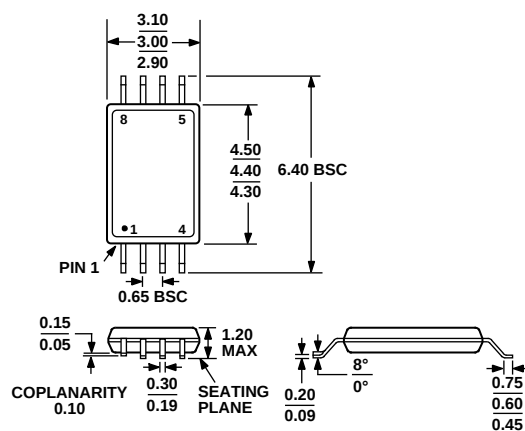


COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012807-A

Figure 48. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body
S-Suffix (R-8)

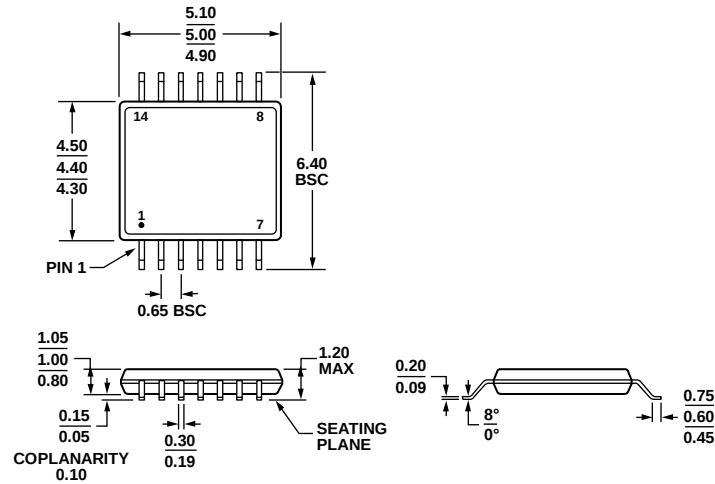
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AA

Figure 49. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)

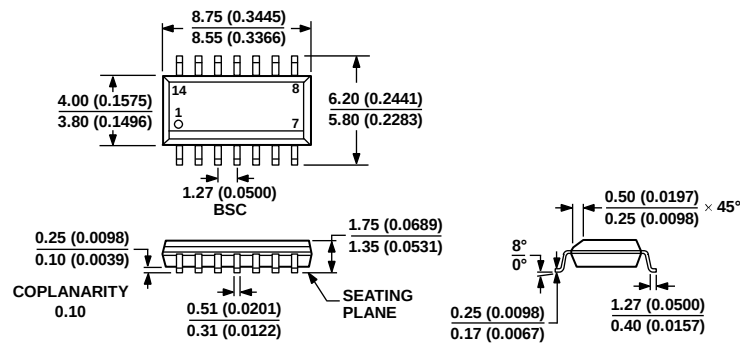
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 50. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 51. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body
S-Suffix (R-14)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
OP162GSZ	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP162GSZ-REEL	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP162GSZ-REEL7	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP262DRUZ-REEL	–40°C to +125°C	8-Lead TSSOP	RU-8
OP262GS	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP262GS-REEL	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP262GS-REEL7	–40°C to +125°C	8-Lead SOIC_	S-Suffix (R-8)
OP262GSZ	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP262GSZ-REEL	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP262GSZ-REEL7	–40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP262HRU-REEL	–40°C to +125°C	8-Lead TSSOP	RU-8
OP262HRUZ	–40°C to +125°C	8-Lead TSSOP	RU-8
OP262HRUZ-REEL	–40°C to +125°C	8-Lead TSSOP	RU-8
OP462GS	–40°C to +125°C	14-Lead SOIC_	S-Suffix (R-14)
OP462GS-REEL	–40°C to +125°C	14-Lead SOIC_N	S-Suffix (R-14)
OP462GS-REEL7	–40°C to +125°C	14-Lead SOIC_N	S-Suffix (R-14)
OP462GSZ	–40°C to +125°C	14-Lead SOIC_N	S-Suffix (R-14)
OP462GSZ-REEL	–40°C to +125°C	14-Lead SOIC_N	S-Suffix (R-14)
OP462GSZ-REEL7	–40°C to +125°C	14-Lead SOIC_N	S-Suffix (R-14)
OP462HRU-REEL	–40°C to +125°C	14-Lead TSSOP	RU-14
OP462HRUZ-REEL	–40°C to +125°C	14-Lead TSSOP	RU-14

¹ Z = RoHS Compliant Part.