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1 Pin description

Figure 1: Pin connections

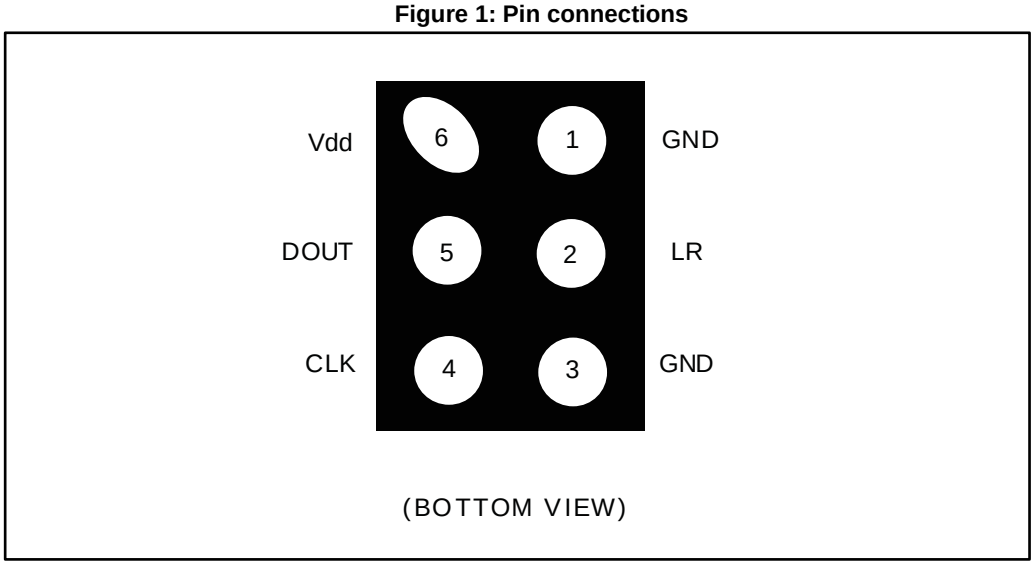


Table 2: Pin description

Pin n°	Pin name	Function
1	GND	0 V supply
2	LR	Left/right channel selection; MIC1 LR is connected to GND or Vdd and MIC2 LR is connected to Vdd or GND (see *Figure 5: "MP45DT02-M electrical connections for stereo configuration"*
3	GND	0 V supply
4	CLK	Synchronization input clock
5	DOUT	Left/right PDM data output
6	Vdd	Power supply

2 Acoustic and electrical specifications

2.1 Acoustic and electrical characteristics

The values listed in the table below are specified for Vdd = 1.8 V, Clock = 2.4 MHz, T = 25 °C, unless otherwise noted.

Table 3: Acoustic and electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.64	1.8	3.6	V
Idd	Current consumption in normal mode	No load on data line		0.65		mA
IddPdn	Current consumption in power-down mode (2)			20		µA
Scc	Short-circuit current		1		10	mA
AOP	Acoustic overload point			120		dBSPL
So	Sensitivity		-29	-26	-23	dBFS
SNR	Signal-to-noise ratio	A-weighted @1 kHz, 1 Pa		61		dB
PSR	Power supply rejection	Guaranteed by design (3)		-70		dBFS
Clock	Input clock frequency (4)		1	2.4	3.25	MHz
TWK	Wake-up time (5)	Guaranteed by design			10	ms
Top	Operating temperature range		-30		+85	°C
V_{IOL}	Low level logic input/output voltage	I_{out} = 1 mA	-0.3		0.35xVdd	V
V_{IOH}	High level logic input/output voltage	I_{out} = 1 mA	0.65xVdd		Vdd+0.3	V

Notes:

(1)Typical specifications are not guaranteed.

(2)Input clock in static mode.

(3)Test signal: 217 Hz square wave, 100 mVpp on Vdd pin.

(4)Duty cycle: min = 40% max = 60%.

(5)Time from the first clock edge to valid output data.

Table 4: Distortion specifications

Parameter	Test condition	Value
Distortion	100 dBSPL (50 Hz - 4 kHz)	< 1% THD + N
Distortion	115 dBSPL (1 kHz)	< 5% THD + N

2.2 Timing characteristics

Table 5: Timing characteristics

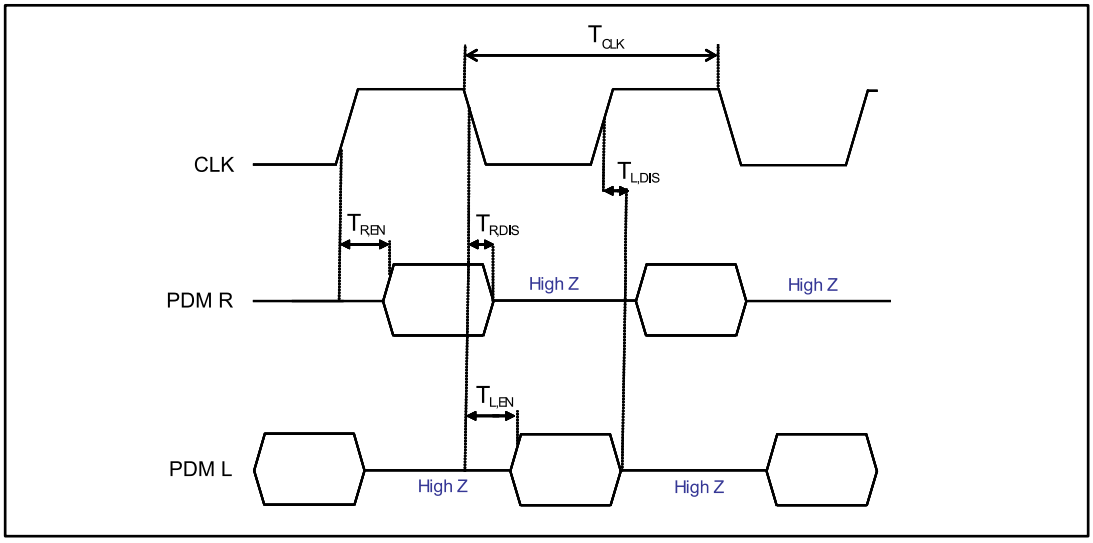
Parameter	Description	Min	Max	Unit
f_{CLK}	Clock frequency for normal mode	1	3.25	MHz
f_{PD}	Clock frequency for power-down mode		0.23	MHz
T_{CLK}	Clock period for normal mode	308	1000	ns
$T_{R,EN}$	Data enabled on DATA line, L/R pin = 1	30 (1)		ns
$T_{R,DIS}$	Data disabled on DATA line, L/R pin = 1		16(1)(2)	ns
$T_{L,EN}$	Data enabled on DATA line, L/R pin = 0	30(1)		ns
$T_{L,DIS}$	Data disabled on DATA line, L/R pin = 0		16(1)(2)	ns

Notes:

(1)From design simulations

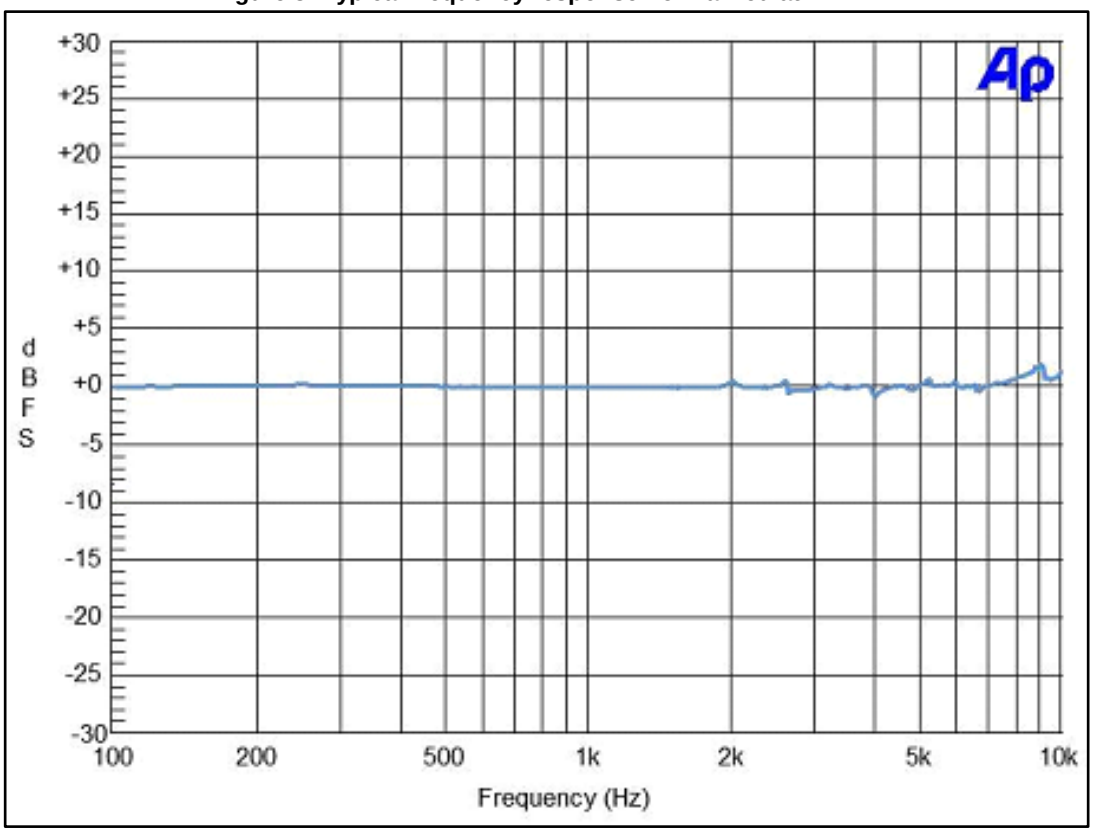
(2)In order to measure the disable time, a 1 kΩ pull-down resistor must be added to the DOUT pin.

Figure 2: Timing waveforms



2.3 Frequency response

Figure 3: Typical frequency response normalized at 1 kHz



3 Sensing element

The sensing element shall mean the acoustic sensor consisting of a conductive movable plate and a fixed plate placed in a tiny silicon chip. This sensor transduces the sound pressure into the changes of coupled capacity between those two plates.

Omron Corporation supplies this element for STMicroelectronics.

4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6: Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin	-0.3 to Vdd +0.3	V
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

5 Functionality

5.1 L/R channel selection

The L/R digital pad lets the user select the DOUT signal pattern as explained in *Table 7: "L/R channel selection"*. The L/R pin must be connected to Vdd or GND.

Table 7: L/R channel selection

L/R	CLK low	CLK high
GND	Data valid	High impedence
Vdd	High impedence	Data valid

6 Application recommendations

Figure 4: MP45DT02-M electrical connections

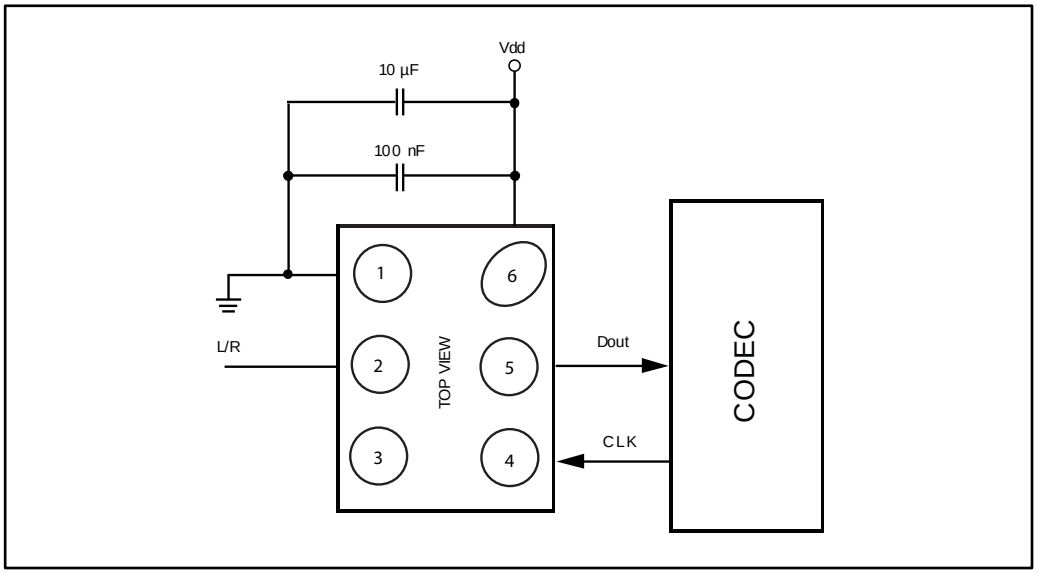
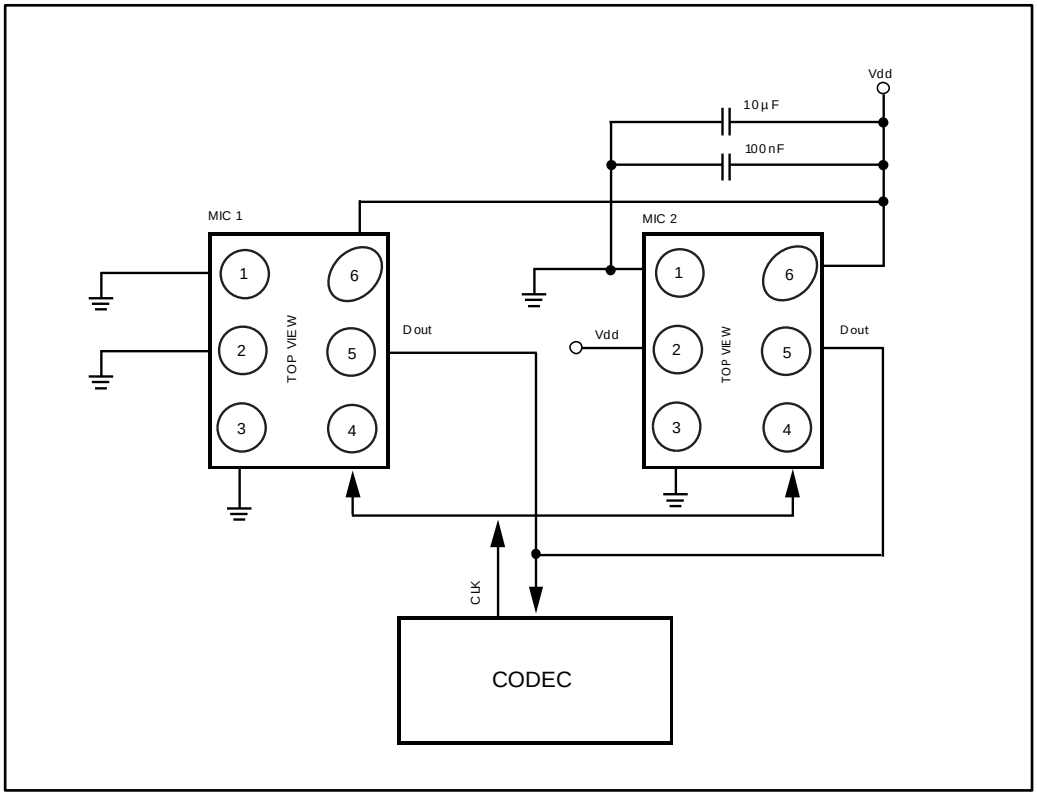


Figure 5: MP45DT02-M electrical connections for stereo configuration



Power supply decoupling capacitors (100 nF ceramic, 10 µF ceramic) should be placed as near as possible to pin 6 of the device (common design practice).

The L/R pin must be connected to Vdd or GND (refer to *Table 7: "L/R channel selection"*).

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 Soldering information

The HLGA (4.72 x 3.76 x 1.25) mm package is also compliant with the RoHS and “Green” standards and is qualified for soldering heat resistance according to JEDEC J-STD-020.

Landing pattern and soldering recommendations are available at www.st.com.

Figure 6: Recommended soldering profile limits

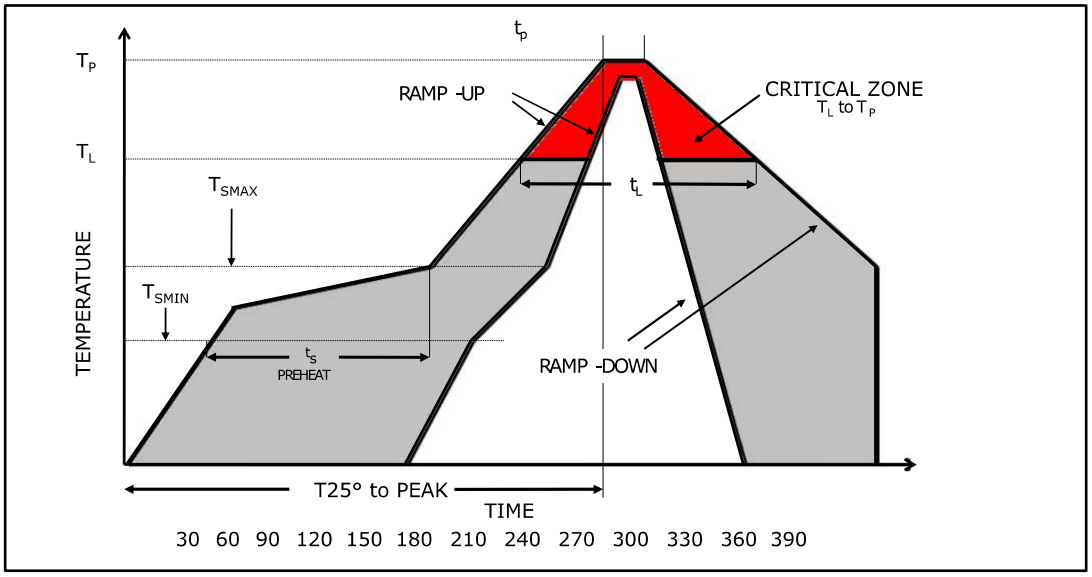
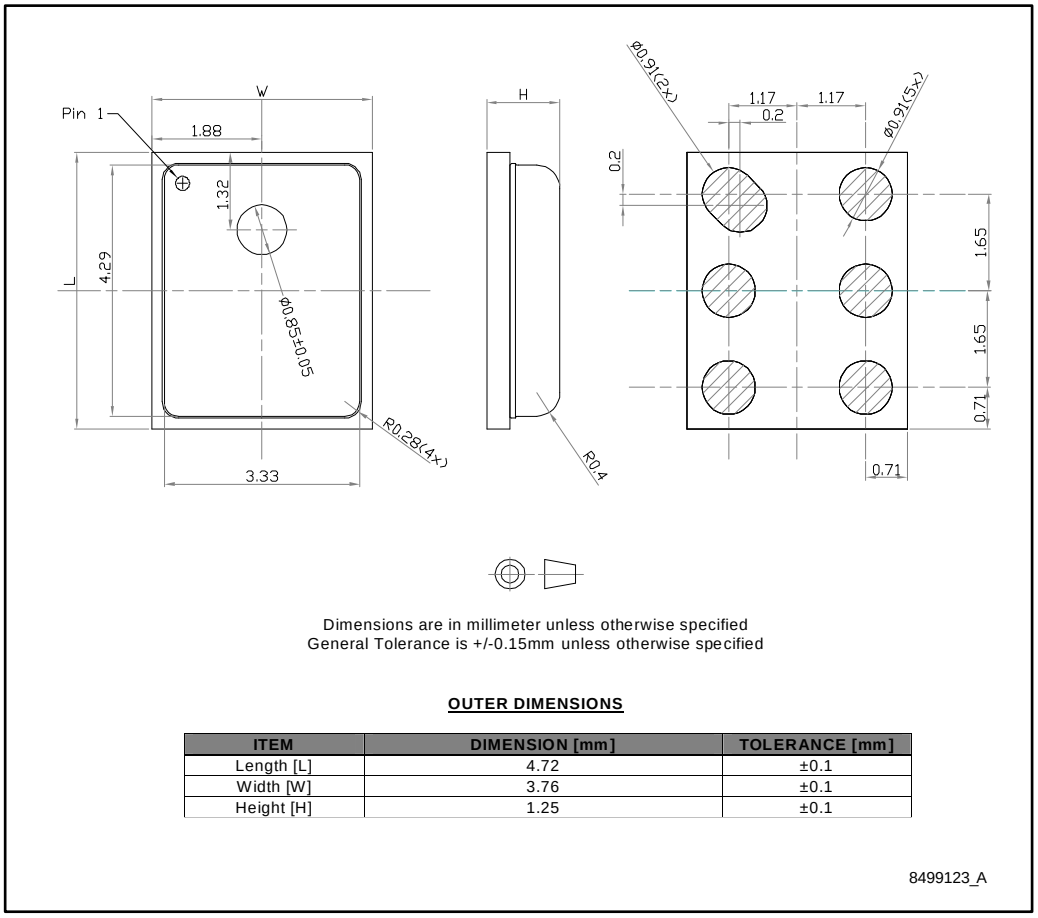


Table 8: Recommended soldering profile limits

Description	Parameter	Pb free
Average ramp rate	T_L to T_P	3 °C/sec max
Preheat Minimum temperature Maximum temperature Time (T_{SMIN} to T_{SMAX})	 T_{SMIN} T_{SMAX} t_S	 150 °C 200 °C 60 sec to 120 sec
Ramp-up rate	T_{SMAX} to T_L	
Time maintained above liquidus temperature Liquidus temperature	t_L T_L	60 sec to 150 sec 217 °C
Peak temperature	T_P	260 °C max
Time within 5 °C of actual peak temperature		20 sec to 40 sec
Ramp-down rate		6 °C/sec max
Time 25 °C (t25 °C) to peak temperature		8 minutes max

7.2 HLGA (4.72 x 3.76 mm) 6L (metal) package information

Figure 7: HLGA (4.72 x 3.76 mm) 6-lead package outline and mechanical data



ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	4.72	±0.1
Width [W]	3.76	±0.1
Height [H]	1.25	±0.1

Note: The MEMS microphone metal cap can exhibit some level of variation in color when the device is subjected to a thermal process.

8 Revision history

Table 9: Document revision history

Date	Revision	Changes
13-Jun-2016	1	Initial release

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