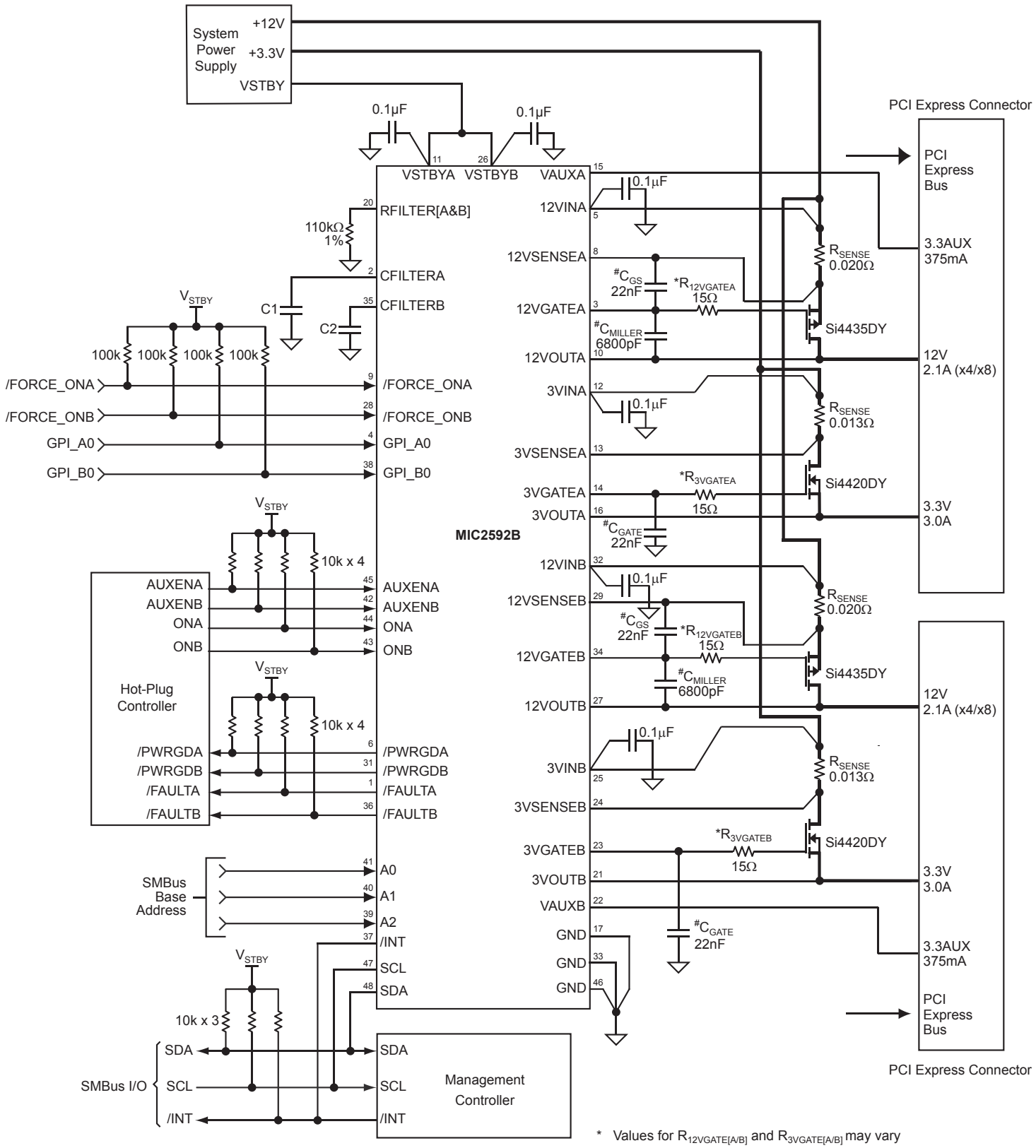
Typical Application

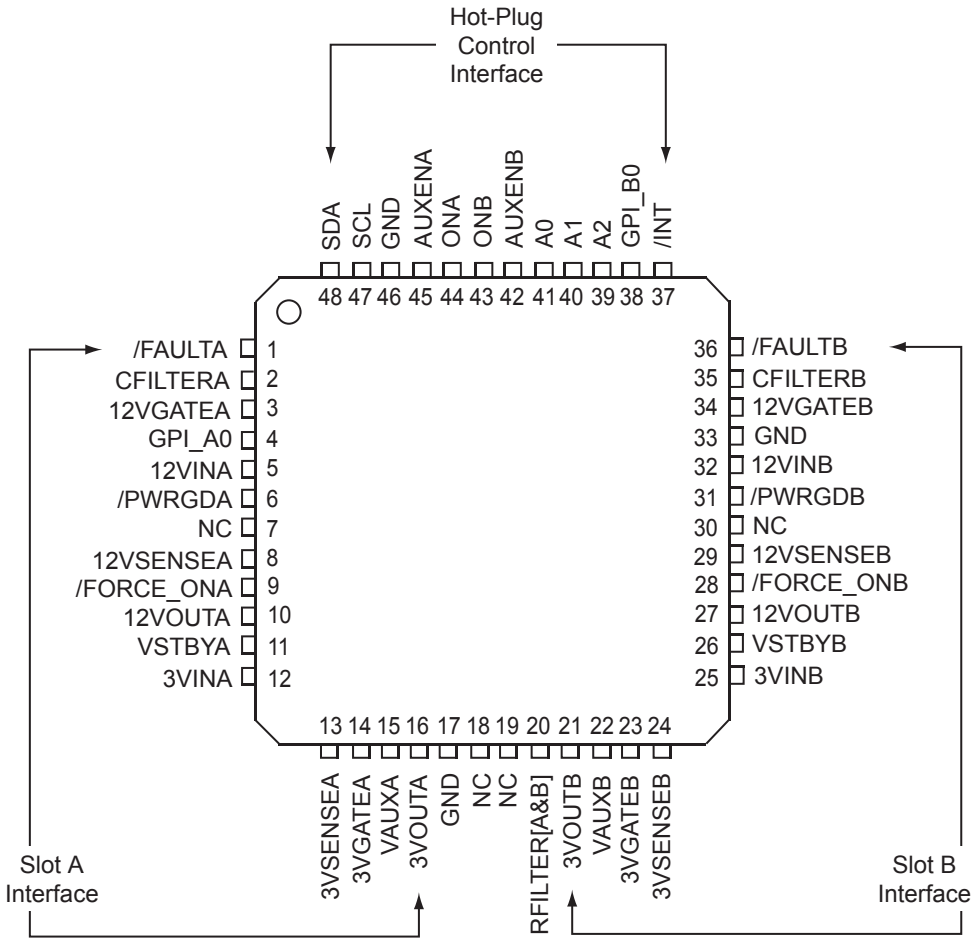


* Values for $R_{12VGATE[A/B]}$ and $R_{3VGATE[A/B]}$ may vary depending upon the C_{GS} of the external MOSFETs.

\# These components are not required for MIC2592B operation but can be implemented for GATE output slew rate control (application specific)

¥ Bold lines indicate high current paths

Pin Configuration



48-Pin TQFP

Pin Description

Pin Number	Pin Name	Pin Function
5 32	12VINA 12VINB	12V Supply Power and Sense Inputs [A/B]: Two pins are provided for Kelvin. connection (one for each slot). Pin 5 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 12V Slot A. Pin 32 is the (+) Kelvin sense connection to the supply side of the sense resistor for 12V Slot B. These two pins must ultimately connect to each other as close as possible at the MIC2592B controller in order to eliminate any IR drop between these pins. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
12 25	3VINA 3VINB	3.3V Supply Power and Sense Inputs [A/B]: Two pins are provided for connection (one for each slot). Pin 12 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 3V Slot A. Pin 25 is the (+) Kelvin sense connection to the supply side of the sense resistor for 3V Slot B. These two pins must ultimately connect to each other as close as possible at the MIC2592B controller in order to eliminate any IR drop between these pins. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
16 21	3VOUTA 3VOUTB	3.3V Power-Good Sense Inputs: Connect to 3.3V[A/B] outputs. Used to monitor the 3.3V output voltages for Power-is-Good status.
10 27	12VOUTA 12VOUTB	12V Power-Good Sense Inputs: Connect to 12V[A/B] outputs. Used to monitor the 12V output voltages for Power-is-Good status.
8 29	12VSENSEA 12VSENSEB	12V Circuit Breaker Sense Inputs: The current limit thresholds are set by connecting sense resistors between these pins and 12VIN[A/B]. When the current limit threshold of IR = 50mV is reached, the 12VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT}, the circuit breaker is tripped and the GATE pin for the affected 12V supply's external MOSFET is immediately pulled high.
13 24	3VSENSEA 3VSENSEB	3V Circuit Breaker Sense Inputs: The current limit thresholds are set by connecting sense resistors between these pins and 3VIN[A/B]. When the current limit threshold of IR = 50mV is reached, the 3VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT}, the circuit breaker is tripped and the GATE pin for the affected 3V supply's external MOSFET is immediately pulled low.
3 34	12VGATEA 12VGATEB	12V Gate Drive Outputs: Each pin connects to the gate of an external P-Channel MOSFET. During power-up, the C_{GATE} and the C_{GS} of the MOSFETs are connected to a 25µA current sink. This controls the value of dv/dt seen at the source of the MOSFETs. During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of t_{FLT}. Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the GATE pin for the affected slot is immediately brought high. These pins are charged by an internal current source during power-down. Also, the 3V supply for the affected slot is shut-down.
14 23	3VGATEA 3VGATEB	3V Gate Drive Outputs: Each pin connects to the gate of an external N-Channel MOSFET. During power-up, the C_{GATE} and the C_{GS} of the MOSFETs are connected to a 25µA current source. This controls the value of dv/dt seen at the source of the MOSFETs, and hence the current flowing into the load capacitance. During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of t_{FLT}. Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the GATE pin for the affected slot is immediately brought low. During power-down, these pins are discharged by an internal current source. Also, the 12V supply for the affected slot is shut down.

Pin Description (continued)

Pin Number	Pin Name	Pin Function
11 26	VSTBYA VSTBYB	3.3V Standby Input Voltage: Required to support PCI Express VAUX output. Additionally, the SMBus logic and internal registers run off of VSTBY[A/B] to ensure that the chip is accessible during standby modes. A UVLO circuit prevents turn-on of this supply until VSTBY[A/B] rises above its UVLO threshold. Both pins must be externally connected together at the MIC2592B controller.
15 22	VAUXA VAUXB	3.3VAUX[A/B] Outputs to PCI Express Card Slots: These outputs connect the 3.3AUX pin of the PCI Express connectors to VSTBY[A/B] via internal 400mΩ MOSFETs. These outputs are current limited and protected against short-circuit faults.
44 43	ONA ONB	Enable Inputs: Rising-edge triggered. Used to enable or disable the MAINA and MAINB (+3.3V and +12V) outputs. The outputs can be switched on by these controls only after the V_{STBY} input supply is valid and stabe (i.e., t_{POR} elapses - See the Electrical Characteristics Table). Taking ON[A/B] low after a fault resets the +12V and/or +3.3V fault latches for the affected slot. Tie these pins to GND if using SMI power control. Also, see pin description for /FAULTA and /FAULTB.
45 42	AUXENA AUXENB	Enable Inputs: Rising-edge triggered. Used to enable or disable the VAUX[A/B] outputs. The outputs can be switched on by these controls only after the V_{STBY} input supply is valid and stabe (i.e., t_{POR} elapses - See the Electrical Characteristics Table). Taking AUXEN[A/B] low after a fault resets the respective slot's Aux Output Fault Latch. Tie these pins to GND if using SMI power control. Also, see pin description for /FAULTA and /FAULTB.
2 35	CFILTERA CFILTERB	Overcurrent Timers: Capacitors connected between these pins and GND set the duration of t_{FLT} for each slot. The overcurrent filter delay (t_{FLT}) is the amount of time for which a slot remains in current limit before its circuit breaker is tripped.
6 31	/PWRGDA /PWRGDB	/PWRGD[A/B] Outputs: Open-drain, active-low. Asserted when a slot has been commanded to turn on and has successfully begun delivering power to its respective +12V, +3.3V, and VAUX outputs. Each pin requires an external pull-up resistor to V_{STBY}.
1 36	/FAULTA /FAULTB	/FAULT[A/B] Outputs: Open-drain, active-low. Asserted whenever the circuit breaker trips due to a fault condition (overcurrent, input undervoltage, overtemperature). Each pin requires an external pull-up resistor to V_{STBY}. Bringing the slot's ON[A/B] pin low resets /FAULT[A/B] if /FAULT[A/B] was asserted in response to a fault condition on one of the slot's MAIN outputs (+12V or +3.3V). /FAULT[A/B] is reset by bringing the slot's AUXEN[A/B] pin low if /FAULT[A/B] was asserted in response to a fault condition on the slot's VAUX output. If a fault condition occurred on both the MAIN and VAUX outputs of the same slot, then both ON[A/B] and AUXEN[A/B] must be brought low to deassert the /FAULT[A/B] output.
9 28	/FORCE_ONA /FORCE_ONB	Enable Inputs: Active-low, level-sensitive. Asserting a /FORCE_ON[A/B] input will turn on all three of the respective slot's outputs (+12V, +3.3V, and VAUX), while specifically defeating all protections on those supplies. This explcitly includes all overcurrent and short circuit protections, and on-chip thermal protection for the VAUX[A/B] supplies. Additionally included are the UVLO protections for the +3.3V and +12V main supplies. The /FORCE_ON[A/B] pins do not disable UVLO protection for the VAUX[A/B] supplies. These input pins are intended for diagnostic purposes only. Asserting /FORCE_ON[A/B] will cause the respective slot's /PWRGD[A/B] and /FAULT[A/B] pins to enter their open-drain state. Note that the SMBus register set will continue to reflect the actual state of each slot's supplies. There is a pair of register bits, accessible via the SMBus, which can be set to disable (unconditionally deassert) either or both of the /FORCE_ON[A/B] pins -- See CNTRL[A/B] Register Bit D[2].
4 38	GPI_A0 GPI_B0	General Purpose Inputs: The states of these two inputs are available by reading the Common Status Register, Bits [4:5]. If not used, connect each pin to GND.

Pin Description (continued)

Pin Number	Pin Name	Pin Function
39 40 41	A2 A1 A0	SMBus Address Select Pins: Connect to ground or leave open in order to program device SMBus base address. These inputs have internal pull-up resistors to VSTBY[A/B].
48	SDA	SMBus Data: Bidirectional SMBus data line.
47	SCL	SMBus Clock: Input.
37	/INT	Interrupt Output: Open-drain, active-low. Asserted whenever a power fault is detected if the INTMSK bit (CS Register Bit D[3]) is a logical "0". This output is cleared by performing an "echo reset" to the appropriate fault bit(s) in the STAT[A/B] and/or CS registers. This pin requires an external pull-up resistor to V_{STBY}.
17 33 46	GND	3 Pins, IC Ground Connections: Tie directly to the system's analog GND plane directly at the device.
20	RFILTER[A&B]	Connecting this pin to GND through a 110kΩ, 1% resistor will provide a significant improvement in timeout duration accuracy for slow overcurrent faults on Slot A and Slot B. If left floating (NC), overcurrent timeout duration accuracy is determined by the specification for V_{FILTER} and I_{FILTER}. Please see the "Circuit Breaker Function" text in the "Functional Description" section for more detail.
7 18 19 30	NC	Reserved: Make no external connections to these pins.

Absolute Maximum Ratings[1]

Supply Voltages
- 12VIN[A/B] 14V
- 3VIN[A/B], VSTBY[A/B] 7V
- Any Logic Pin..... –0.5V (min) to 3.6V (max)

Output Current (/FAULT[A/B], /INT, SDA)..... 10mA
Power Dissipation..... Internally Limited
Lead Temperature
- (IR Reflow, Peak Temperature)..... 240°C +0°C/–5°C

Pb-Free Package (-xYTQ)
- (IR Reflow, Peak Temperature)..... 260°C +0°C/–5°C

Storage Temperature..... –65°C to +150°C
ESD Rating[3]

Operating Ratings[2]

Supply Voltages
- 12VIN[A/B]..... 11.0V to 13.0V
- 3VIN[A/B]..... 3.0V to 3.6V
- VSTBY[A/B]..... 3.0V to 3.6V

Ambient Temperature (T_A)..... 0°C to + 70°C
Junction Temperature (T_J)..... 125°C
Package Thermal Resistance
- TQFP (θ_{JA})..... 56.5°C/W

Electrical Characteristics[4]

$12V_{IN[A/B]}$ = 12V, $3V_{IN[A/B]}$ = 3.3V, $V_{STBY[A/B]}$ = 3.3V, T_A = 25°C, unless otherwise noted. **Bold** indicates specification applies over the full operating temperature range from 0°C to +70°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Control and Logic Sections						
I_{CC12}	Supply Current			2.5	**5**	mA
$I_{CC3.3}$				0.5	**1**	mA
I_{CCSTBY}				2.5	**5**	mA
	Undervoltage Lockout Thresholds					
$V_{UVLO(12V)}$	12VIN[A/B]	$12V_{IN[A/B]}$ increasing	**8**	9	**10**	V
$V_{UVLO(3V)}$	3VIN[A/B]	$3V_{IN[A/B]}$ increasing	**2.2**	2.5	**2.75**	V
$V_{UVLO(STBY)}$	VSTBY[A/B]	$V_{STBY[A/B]}$ increasing	**2.8**	2.9	**3.0**	V
V_{HYSUV}	Undervoltage Lockout Hysteresis $12V_{IN}$, $3V_{IN}$			180		mV
$V_{HYSSTBY}$	Undervoltage Lockout Hysteresis $V_{STBY[A/B]}$			50		mV
	Power-Good Undervoltage Thresholds					
$V_{UVTH(12V)}$	12VOUT[A/B]	$12V_{OUT[A/B]}$ decreasing	**10.2**	10.5	**10.8**	V
$V_{UVTH(3V)}$	3VOUT[A/B]	$3V_{OUT[A/B]}$ decreasing	**2.7**	2.8	**2.9**	V
$V_{UVTH(VAUX)}$	VAUX[A/B]	$V_{AUX[A/B]}$ decreasing	**2.7**	2.8	**2.9**	V
V_{HYSPG}	Power-Good Detect Hysteresis			30		mV
$V_{GATE(12V)}$	12VGATE Voltage		**0**		**1.5**	V
$I_{GATE(12VSINK)}$	12VGATE Sink Current	Start Cycle	**15**	25	**35**	µA
$I_{GATE(12VPULLUP)}$	12VGATE Pull-up Current (Fault Off)	Any fault condition $(V_{DD} - V_{GATE})$ = 2.5V	**–20**			mA
$V_{GATE(3V)}$	3VGATE Voltage		**$12V_{IN}$–1.5**		**$12V_{IN}$**	V
$I_{GATE(3VCHARGE)}$	3VGATE Charge Current	Start Cycle	**15**	25	**35**	µA
$I_{GATE(3VSINK)}$	3VGATE Sink Current (Fault Off)	Any fault condition V_{GATE} = 2.5V	**40**			mA
CFILTER[A/B] Overcurrent Delay Time, Pin 20 (RFILTER[A&B]) Floating or NC						
V_{FILTER}	CFILTER[A/B] Threshold Voltage		**1.20**	1.25	**1.30**	V
I_{FILTER}	CFILTER[A/B] Charging Current $\text{Delay(ms)} = \frac{C_{FILTER}(\mu F) \times V_{FILTER}(V)}{I_{FILTER}(\mu A)} \times 10^3$	$V_{12VIN} - V_{12VSENSE} > V_{THILIMIT}$ and/or $V_{3VIN} - V_{3VSENSE} > V_{THILIMIT}$	**1.80**	2.5	**5.0**	µA

Notes:

1. Exceeding measurements given within the “Absolute Maximum Ratings” section may damage the device.
2. The device is not guaranteed to function outside of the measurements given in the “Operating Ratings" section.
3. Devices are ESD sensitive. Employ proper handling precautions. The human body model is 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Electrical Characteristics (continued)[5]

Symbol	Parameter	Condition		Min	Typ	Max	Units
C_{FILTER} Overcurrent DelayTime, Pin 20 grounded through RFILTER[A&B] = 110 kΩ, 1%							
SF	C_{FILTER} Overcurrent Delay Scaling Factor Delay(ms)=C_{FILTER}(µF)×R_{FILTER}(kΩ)×SF	$V_{12VIN} - V_{12VSENSE} > V_{THILIMIT}$ and/or $V_{3VIN} - V_{3VSENSE} > V_{THILIMIT}$		**4.4**	5	**5.6**	
$V_{THILIMIT}$	Current Limit Threshold Voltages 12V[A/B] supplies	$V_{12VIN} - V_{12VSENSE}$		**45**	50	**55**	mV
	3.3V[A/B] supplies	$V_{3VIN} - V_{3VSENSE}$		**45**	50	**55**	mV
V_{THFAST}	12VOUT[A/B] and 3VOUT[A/B] Fast-Trip Threshold Voltages	$V_{12VIN} - V_{12VSENSE}$ / $V_{3VIN} - V_{3VSENSE}$	MIC2592B-2BTQ	**90**	100	**110**	mV
			MIC2592B-3BTQ	**135**	150	**165**	mV
			MIC2592B-5BTQ		Disabled		
$I_{12VSENSE[A/B]}$	12VSENSE[A/B] Input current				0.35		µA
$I_{3VSENSE[A/B]}$	3VSENSE[A/B] Input current				0.35		µA
V_{IL}	LOW-Level Input Voltage ON[A/B], AUXEN[A/B], GPI_[A0/B0], /FORCE_ON[A/B]			**–0.5**		**0.8**	V
V_{OL}	Output LOW Voltage /FAULT[A/B], /PWRGD[A/B], /INT, SDA	I_{OL} = 3mA				**0.4**	V
V_{IH}	HIGH-Level Input Voltage ON[A/B], AUXEN[A/B], GPI_[A0/B0], /FORCE_ON[A/B], A[0-2], SCL, SDA			**2.1**		**3.6**	V
$R_{PULLUP(A0 - A2)}$	Internal Pull-ups from A[0-2] to $V_{STBY[A/B]}$				40		kΩ
$I_{LKG,OFF(12VIN[A/B])}$	12VIN[A/B] Input leakage current 12VIN[A/B] = OFF; 3VIN[A/B] = OFF	V_{STBY} = VSTBY[A/B] = +3.3V,			1		µA
$I_{LKG,OFF(3VIN[A/B])}$	3VIN[A/B] Input leakage current 3VIN[A/B] = OFF; 12VIN[A/B] = OFF	V_{STBY} = VSTBY[A/B] = +3.3V,			1		µA
I_{IL}	Input Leakage Current SCL, ON[A/B], AUXEN[A/B], /FORCE_ON[A/B]					**±5**	µA
$I_{LKG(OFF)}$	Off-State Leakage Current /FAULT[A/B], /PWRGD[A/B], /INT, SDA, GPI_[A0/B0]	GPI_[A0/B0]: I_{LKG} for these two pins measured with V_{AUX} OFF				**±5**	µA
T_{OV}	Overtemperature Shutdown and Reset Thresholds, with overcurrent on slot	T_J increasing, each slot[6]			140		°C
		T_J decreasing, each slot[6]			130		°C
	Overtemperature Shutdown and Reset Thresholds, all other conditions (all outputs will latch OFF)	T_J increasing, both slots[6]			160		°C
		T_J decreasing, both slots[6]			150		°C
$R_{DS(AUX)}$	Output MOSFET Resistance VAUX[A/B] MOSFET	I_{DS} = 375mA, T_J = 125°C				**400**	mΩ
$V_{OFF(VAUX)}$	Off-State Output Offset Voltage $V_{AUX[A/B]}$	$V_{AUX[A/B]}$ = Off, T_J = 125°C				**50**	mV

Notes:

5. Specification for packaged product only.
6. Parameters guaranteed by design. Not 100% production tested.

Electrical Characteristics (continued)[7]

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{AUX(THRESH)}$	Auxiliary Output Current Limit Threshold (Figure 4)	Current which must be drawn from V_{AUX} to register as a fault		0.84		A
$I_{SC(TRAN)}$	Maximum Transient Short Circuit Current	V_{AUX} Enabled, then Grounded	$I_{MAX} = \frac{V_{STBY[A/B]}}{R_{DS(AUX)}}$			A
$I_{LIM(AUX)}$	Regulated Current after Transient	From end of $I_{SC(TRAN)}$ to C_{FILTER} time-out	0.375	0.7	1.35	A
$R_{DIS(12V)}$ $R_{DIS(3V)}$ $R_{DIS(VAUX)}$	Output Discharge Resistance 12VOUT[A/B] 3VOUT[A/B] 3VAUX[A/B]	 $12V_{OUT[A/B]}$ = 6.0V $3V_{OUT[A/B]}$ = 1.65V $3V_{AUX[A/B]}$ = 1.65V		 1600 150 430		 Ω Ω Ω
$t_{OFF(12V)}$	12V Current Limit Response Time (Figure 2)	MIC2592B-2BTQ C_{GATE} = 25pF $V_{IN} - V_{SENSE}$ = 140mV		1	**2.0**	µs
$t_{OFF(3V)}$	3.3V Current Limit Response Time (Figure 3)	MIC2592B-2BTQ C_{GATE} = 25pF $V_{IN} - V_{SENSE}$ = 140mV[8]		1	**2.0**	µs
$t_{SC(TRAN)}$	VAUX[A/B] Current Limit Response Time (Figure 5)	$V_{AUX[A/B]}$ = 0V, V_{STBYA} = V_{STBYB} = +3.3V		2.5	**5**	µs
$t_{PROP(12VFAULT)}$	Delay from 12V[A/B] Overcurrent Limit to /FAULT output	MIC2592B-2BTQ C_{FILTER} = 0 $V_{IN} - V_{SENSE}$ = 140mV[8]		1		µs
$t_{PROP(3VFAULT)}$	Delay from 3V[A/B] Overcurrent Limit to /FAULT[A/B] Output	MIC2592B-2BTQ C_{FILTER} = 0 $V_{IN} - V_{SENSE}$ = 140mV[8]		1		µs
$t_{PROP(VAUXFAULT)}$	Delay from VAUX[A/B] Overcurrent	MIC2592B-2BTQ limit to /FAULT[A/B] output C_{FILTER} = 0 V_{AUX} Output Grounded[8]		1		µs
t_W	ON[A/B], AUXEN[A/B] Pulse Width	**Note 8**		100		ns
t_{POR}	MIC2592B Power-On Reset Time after VSTBY[A/B] becomes valid	**Note 8**		250		µs
SMBus Timing						
t_1	SCL (clock) period	Figure 1	**2.5**			µs
t_2	Data In setup time to SCL HIGH	Figure 1	**100**			ns
t_3	Data Out stable after SCL LOW	Figure 1	**300**			ns
t_4	Data LOW setup time to SCL LOW	Start condition, Figure 1	**100**			ns
t_5	Data HIGH hold time after SCL HIGH	Stop condition, Figure 1	**100**			ns

Notes:

7. Specification for packaged product only.
8. Parameters guaranteed by design. Not 100% production tested.

Timing Diagrams

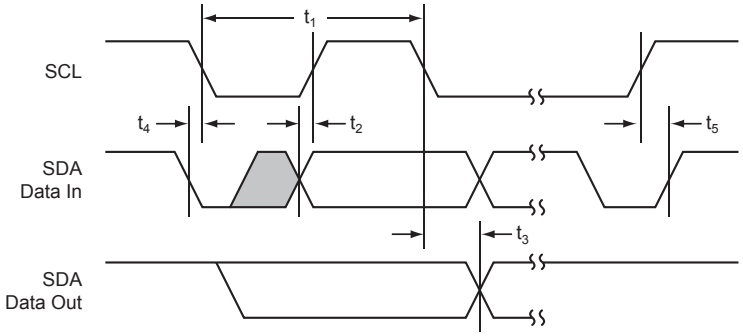


Figure 1. SMBus Timing

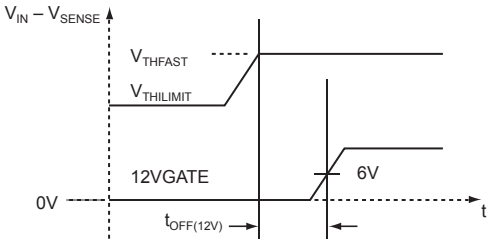


Figure 2. 12V Current Limit Response Timing

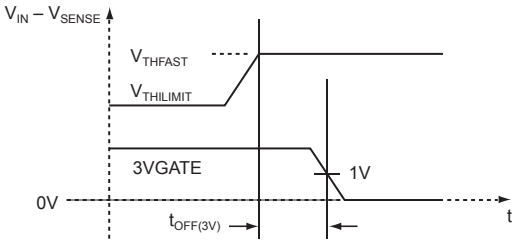


Figure 3. 3V Current Limit Response Timing

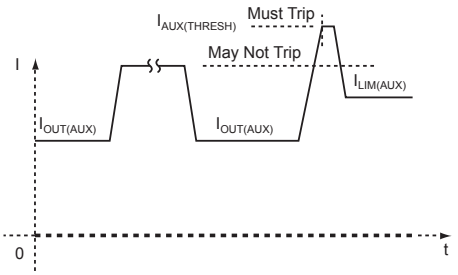


Figure 4. VAUX Current Limit Threshold

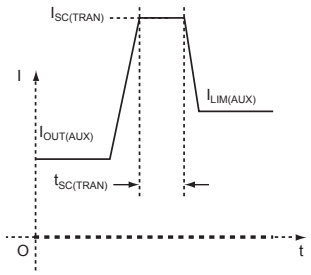
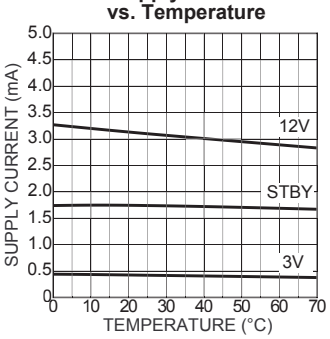


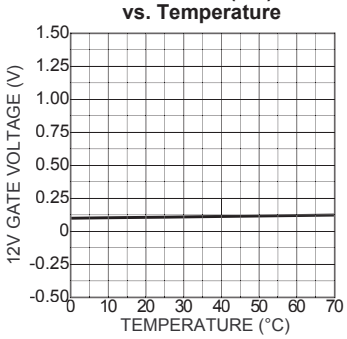
Figure 5. VAUX Current Limit Response Timing

Typical Characteristics

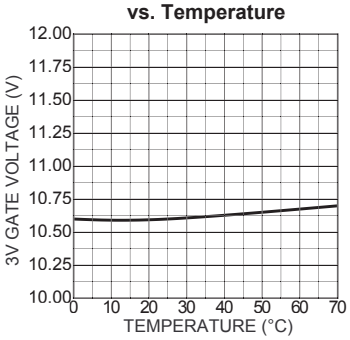
Supply Current vs. Temperature



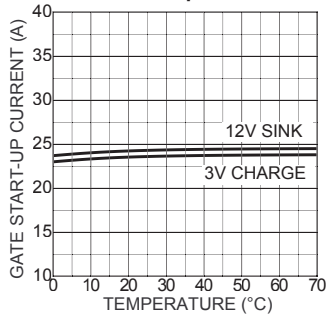
12V GATE(ON) vs. Temperature



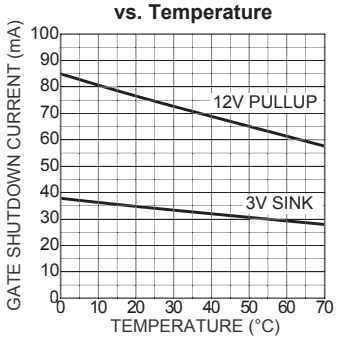
3V GATE vs. Temperature



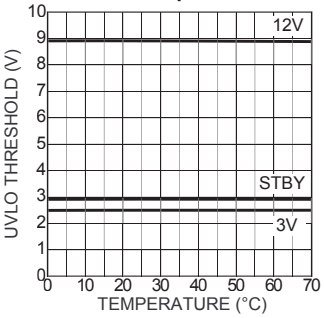
GATE Start-Up Curent vs. Temperature



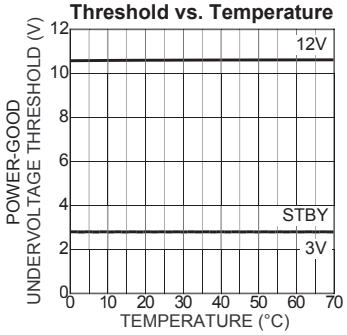
GATE Shutdown Current vs. Temperature



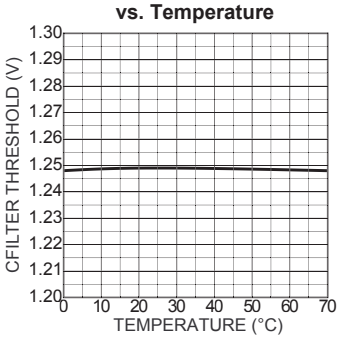
UVLO Threshold vs. Temperature



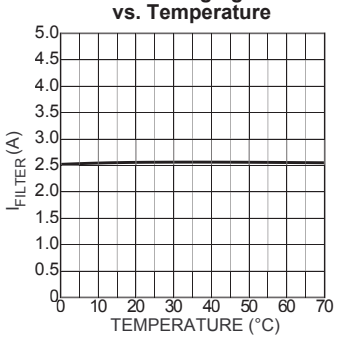
Power-Good Undervoltage Threshold vs. Temperature



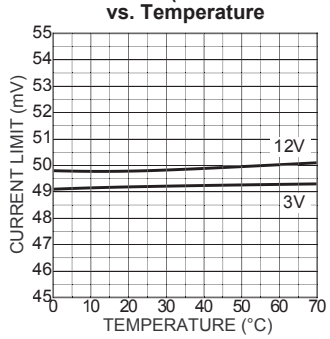
CFILTER Threshold vs. Temperature



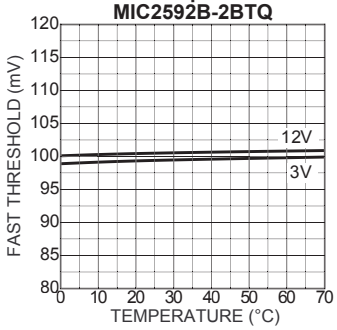
CFILTER Charging Current vs. Temperature



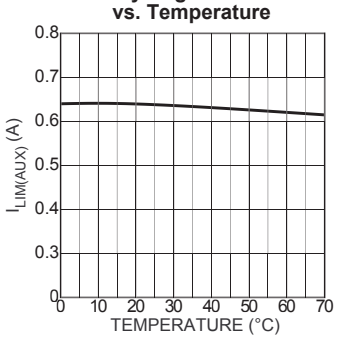
Current Limit (Slow Threshold) vs. Temperature



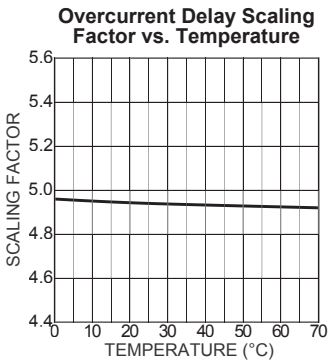
Current Limit (Fast Threshold) vs. Temperature MIC2592B-2BTQ

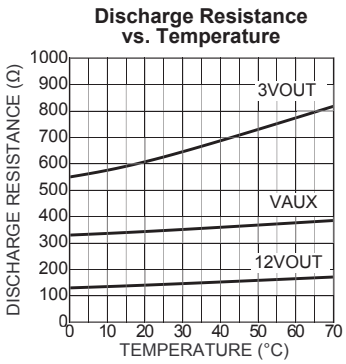


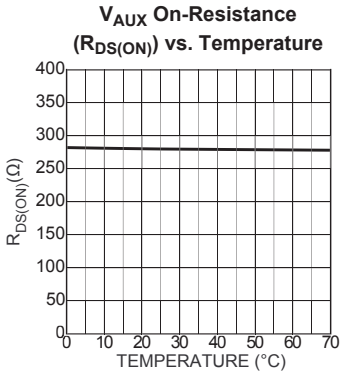
Auxiliary Regulated Current vs. Temperature



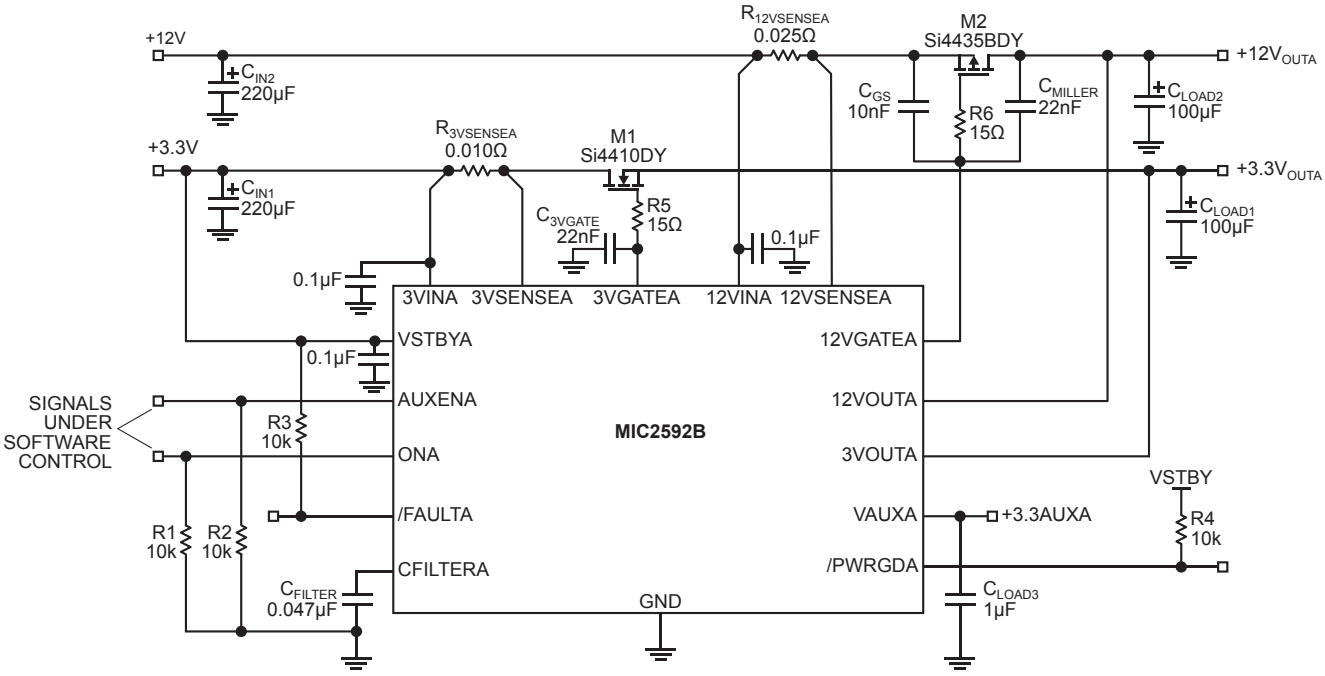
Typical Characteristics (cont.)







Test Circuit

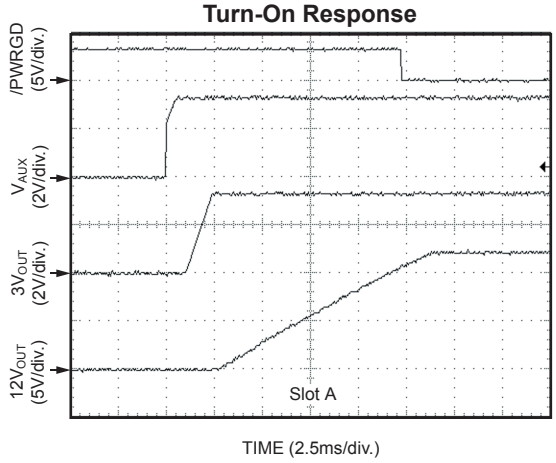


(Additional pins omitted for clarity - Slot A shown only)

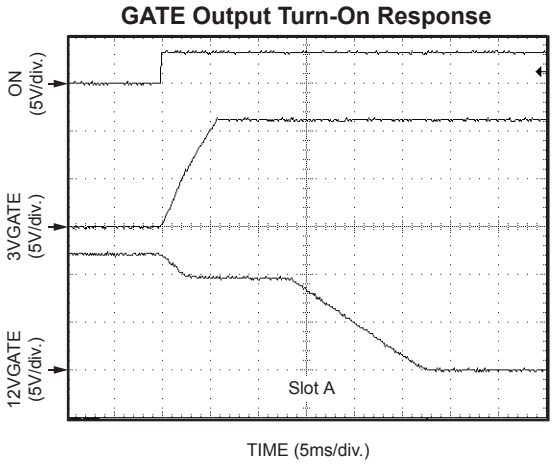
MIC2592B Test Circuit

Functional Characteristics

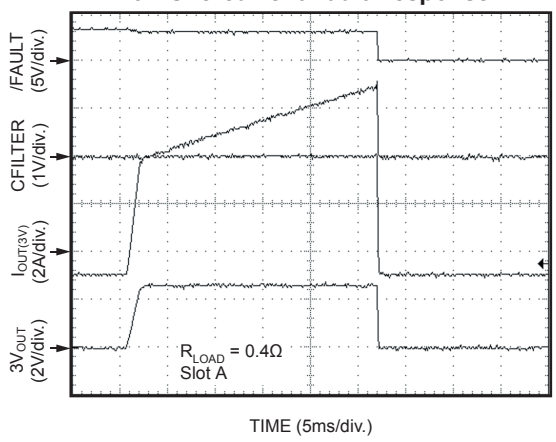
Turn-On Response



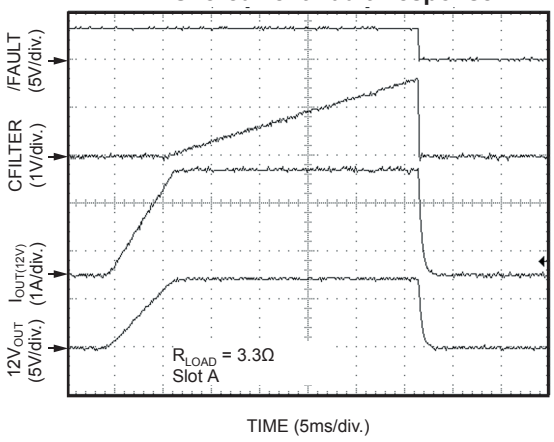
GATE Output Turn-On Response



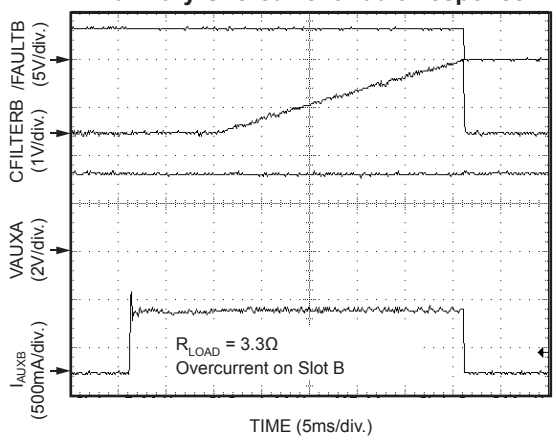
3V Overcurrent Fault Response



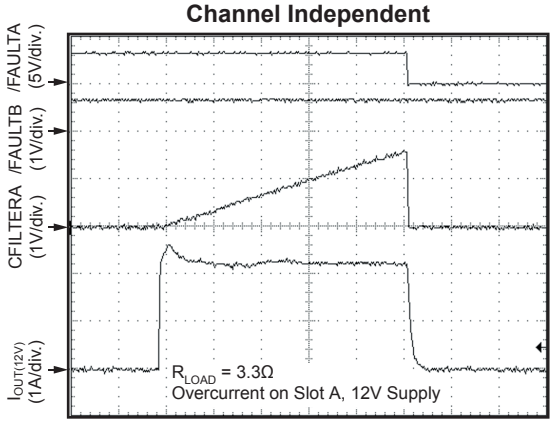
12V Overcurrent Fault Response



Auxiliary Overcurrent Fault Response

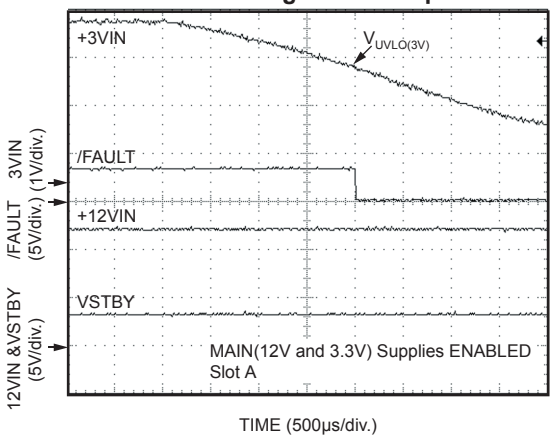


Overcurrent Fault Response Channel Independent

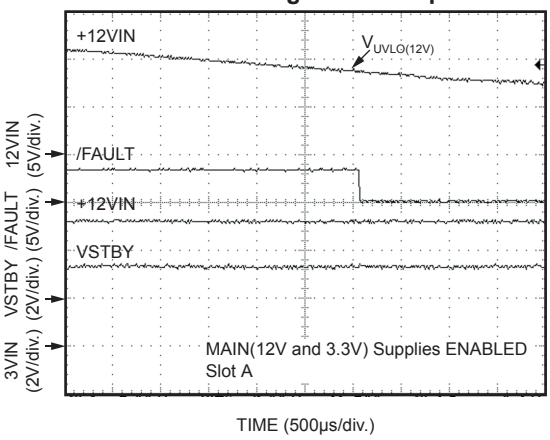


Functional Characteristics cont.

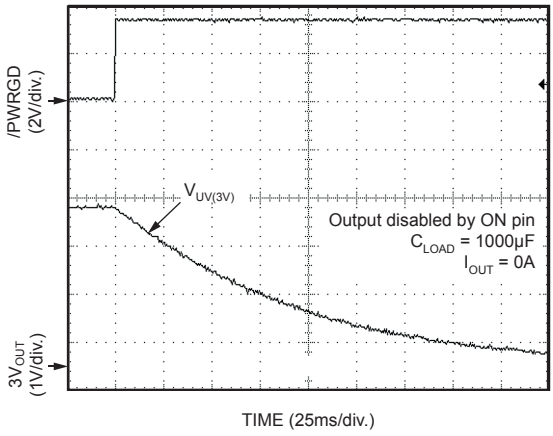
3V Undervoltage Fault Response



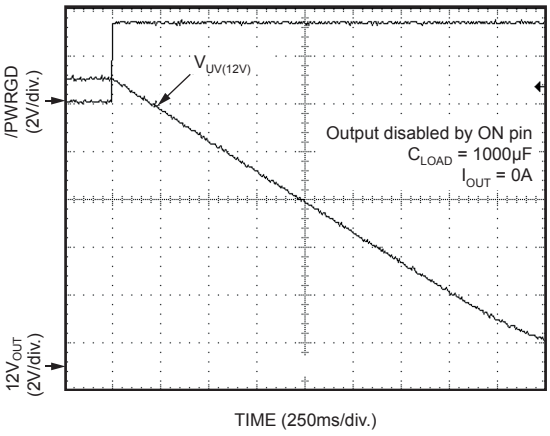
12V Undervoltage Fault Response



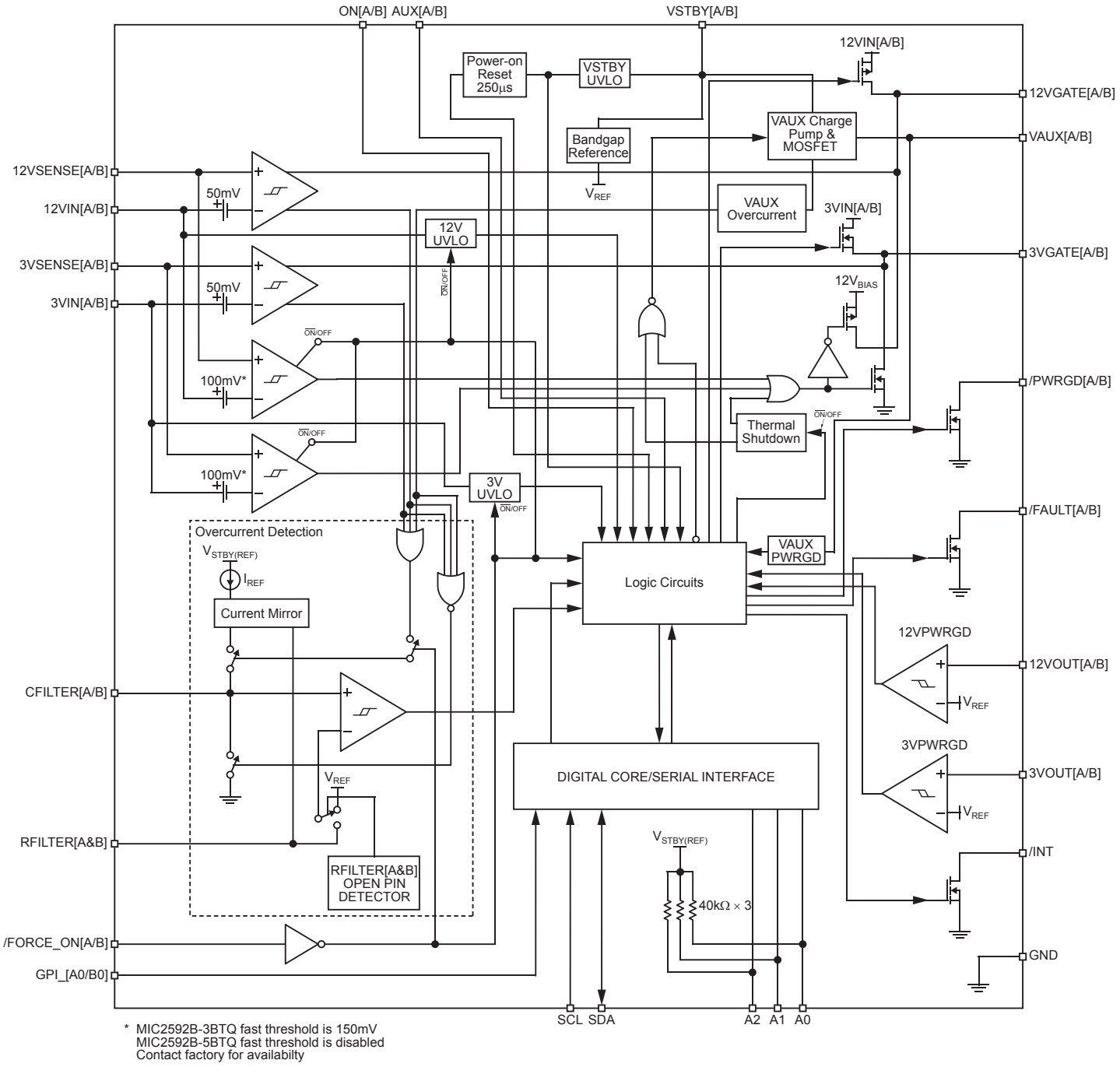
3V Ouput Discharge Response



12V Ouput Discharge Response



Functional Block Diagram



* MIC2592B-3BTQ fast threshold is 150mV
MIC2592B-5BTQ fast threshold is disabled
Contact factory for availabilty

MIC2592B Block Diagram

Functional Description

Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages (“hot-plugged”), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board’s supply pins. This transient inrush current can cause the system’s supply voltages to temporarily go out of regulation, causing data loss or system lock-up. In more extreme cases, the transients occurring during a hot-plug event may cause permanent damage to connectors or on-board components.

The MIC2592B addresses these issues by limiting the in-rush currents to the load (PCI Express Board), and thereby controlling the rate at which the load’s circuits turn-on. In addition to this inrush current control, the MIC2592B offers input and output voltage supervisory functions and current limiting to provide robust protection for both the system and circuit board.

System Interface

The MIC2592B employs two system interfaces: the hardware Hot-Plug Interface (HPI) and the System Management Interface (SMI). The HPI includes ON[A/B], AUXEN[A/B], as well as /FAULT[A/B]; the SMI consists of SDA, SCL, and /INT, whose signals conform to the levels and timing of the SMBus specification. The MIC2592B can be operated exclusively from the SMI, or can employ the HPI for power control while continuing to use the SMI for access to all but the power control registers.

In addition to the basic power control features of the MIC2592B accessible by the HPI, the SMI also gives the host access to the following information from the part:

- Fault conditions occurring on each supply.
- GPI_[A0/B0] pin status

When using the System Management Interface for power control, do not use the Hot-Plug Interface. Conversely, when using the Hot-Plug Interface for power control, do not execute power control commands over the System Management Interface bus (all other register accesses via the SMI bus remain permissible while in the HPI control mode). When utilizing the SMI exclusively, the HPI input pins (ON[A/B], AUXEN[A/B], and /FORCE_ON[A/B]) should be configured as shown below in Figure 6 (Disabling HPI when SMI control is used). This configuration safeguards the power slots in the event that the SMBus communication link is disconnected for any reason.

Additionally, when utilizing the HPI exclusively, the SMBus (or SMI) will be inactive if the input pins (SDA, SCL, A0, A1, and A2) are configured as shown in Figure 6 below (Disabling SMI when HPI Control is used).

Power Stability and Power-On Reset

The MIC2592B utilizes VSTBY[A/B] as the main supply input source. VSTBY[A/B] is required for proper operation of the MIC2592B’s SMBus and registers and must be applied at all times. To ensure that the MIC2592B controller operates properly, the V_{STBY} input must be stable and remain above the undervoltage lockout (UVLO) threshold once applied. Sufficient input bulk capacitance should be used to prevent the supply from "drooping", causing VSTBY[A/B] to fall below the UVLO threshold. Also, decoupling capacitors should be placed at each of the MIC2592B inputs in order to filter high frequency noise transients.

V_{STBY} must be the first supply input applied followed by the MAIN supply inputs of $12V_{IN}$ and $3V_{IN}$. A Power-On Reset (POR) cycle is initiated after VSTBY[A/B] rises above its UVLO threshold and remains valid at that voltage for 250µs. All internal registers are cleared after POR. If VSTBY[A/B] is recycled, the MIC2592B enters a new power-on-reset cycle. The SMBus is ready for access at the end of the POR cycle (250µs after VSTBY[A/B] is valid). During t_{POR}, all outputs remain off. In most applications, the total POR interval will consist of the time required to charge the V_{STBY} input (by-pass) capacitance to the UVLO threshold plus the internal t_{POR}. The following equation is used to approximate the total POR interval:

$$t_{POR\_TOTAL(\mu S)} = \left\{ \left\lceil \frac{\left(C_{STBY(\mu F)} \times V_{ULVO(STBY)} \right)}{I_{CHARGE(STBY)}(A)} \right\rceil \times 10^{-6} \right\} + t_{POR}(\mu S)$$

where C_{STBY} is the V_{STBY} input bulk bypass capacitance and $I_{CHARGE(STBY)}$ is the current supplied by the V_{STBY} source to charge the capacitance.

Power-Up Cycle

Enabling the GATE output

When a slot's MAIN supplies are off, the 12VGATE pin is held high with an internal pull-up. Similarly, the 3VGATE pin is internally held low. When the MAIN supplies of the MIC2592B are enabled by asserting ON[A/B], the 3VGATE[A/B] and 12VGATE[A/B] pins are each connected to a constant current supply. These supplies are each nominally 25µA. For a slot’s 3VGATE pin, this is a current source; for the 12VGATE pin, this is a current sink.

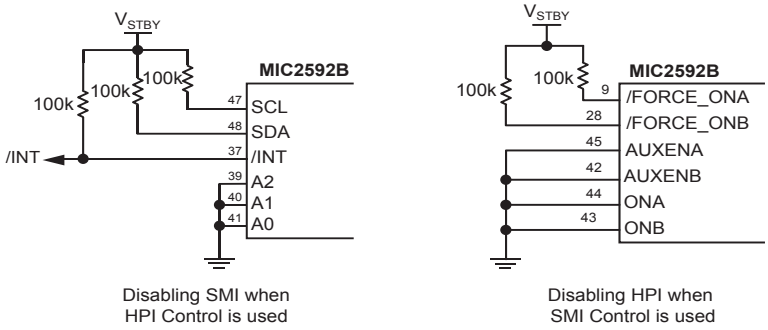


Figure 6. Input Pin Configuration for Disabling HPI/SMI Control

Inrush Current and Load Dominated Start-up

The expected maximum inrush current can be calculated by using the following equation:

$$INRUSH \cong \left|I_{GATE}\right| \times \frac{C_{LOAD}}{C_{GATE}} \cong 25\mu A \times \frac{C_{LOAD}}{C_{GATE}}$$

where $|I_{GATE}|$ is the GATE pin current, $I_{GATE(3VCHARGE)}$ or $I_{GATE(12VSINK)}$, C_{LOAD} is the load capacitance, and C_{GATE} is the total GATE capacitance (C_{ISS} of the external MOSFET and any external capacitance connected from the GATE output pin to the GATE reference – GND or source).

For the 3.3V outputs and 12V outputs (if no external 12VGATE output capacitors are implemented), the following equation is used to determine the output slew rate.

$$dV_{OUT} / dt = \frac{I_{LIM(3V/12V)}}{C_{LOAD(3V/12V)}}$$

Consequently, the overcurrent timer delay must be programmed to exceed the time it will take to charge the output load to the input rail voltage level.

MAIN Outputs (Start-up Delay and Slew-Rate Control)

The 3.3V outputs act as source followers. In this mode of operation, $V_{SOURCE} = [V_{GATE} - V_{TH(ON)}]$ until the associated output reaches 3.3V. The voltage on the gate of the MOSFET will then continue to rise until it reaches 12V, which ensures minimum $R_{DS(ON)}$. Note that a delay exists between the ON command to a slot and the appearance of voltage at the slot's 3.3V output. This delay is the time required to charge the 3VGATE output up to the threshold voltage of the external MOSFET (typically about 3V).

$$t_{3VDLY} = \frac{\left(C_{GATE} \times V_{GS(TH)}\right)}{I_{GATE(3VCHARGE)}}$$

The source (output) side of the external MOSFET will reach the drain voltage in a time given by:

$$t_{3V(SOURCE\_DRAIN)} = t_{3VDLY} + \frac{\left(C_{LOAD} \times V_{DRAIN}\right)}{I_{LIM(3V)}}$$

For the 12V outputs, each MOSFET is configured as a Miller integrator (by virtue of C_{MILLER}, which is connected between the MOSFET's gate and drain). In this configuration, the feedback action from drain to gate of the MOSFET causes the voltage at the drain of the MOSFET to slew in a linear fashion at a rate which satisfies the following equation:

$$dv / dt(12V) = -\left(\frac{I_{GATE}}{C_{MILLER}}\right)$$

A delay exists between the ON command to a slot and the appearance of voltage at the slot's 12V output. For a slot's 12V output, that delay is given by the time required for the capacitor from the gate of the MOSFET to its source (typically five times the value of C_{MILLER}) to charge to the threshold voltage of the MOSFET (typically about 3V). In this instance, the delay before the output voltage starts ramping can be approximated by:

$$t_{12VDLY} \cong \frac{\left(C_{GATE(TOTAL)} \times V_{GS(TH)}\right)}{\left|I_{GATE}\right|}$$

where $C_{GATE(TOTAL)}$ is the sum of the C_{GS} of the external MOSFET, any external capacitance from the GATE output of the MIC2592B to the source of the MOSFET, and C_{MILLER} (external, if used).

Table 1 approximates the output slew-rate for various values of C_{GATE} when start-up is dominated by GATE capacitance (external C_{GATE} from GATE pin to ground plus C_{GS} of the external MOSFET for the 3.3V rail; C_{MILLER} for the 12V rail).

$\|I_{GATE}\|$ = 25µA	
C_{GATE} or C_{MILLER}	**dv/dt (load)**
0.01µF*	2.5V/ms
0.022µF*	1.136V/ms
0.047µF	0.532 V/ms
0.1µF	0.250V/ms

* Values in this range will be affected by the internal parasitic capacitances of the MOSFETs used, and should be verified experimentally.

Table 1. 3.3V and 12V Output Slew-Rate Selection for Gate Capacitance Dominated Start-up

Power-Down Cycle

When one or more PCI slots are disabled via the MIC2592B output control pins, ON[A/B] or AUXEN[A/B], the output voltage for each supply will discharge as a function of the RC time constant produced by the controller's internal resistance (R_{DIS}) connected to the output and the load capacitance (C_{LOAD}). The typical value of R_{DIS} for each supply is listed in the Electrical Characteristics Table. The charts below in Figure 7 display curves of the fall time (90% - 10%) as a function of the output load capacitance for both the 3V and 12V MAIN outputs.

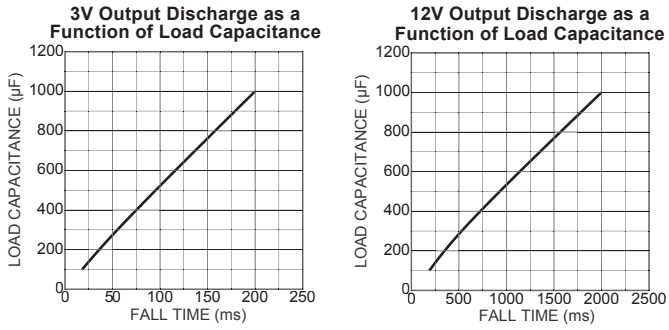


Figure 7. 3V and 12V Output Discharge vs. Load Capacitance

Standby Mode

Standby mode is entered when one or more of the MAIN supply inputs (12VIN and/or 3VIN) is below its respective UVLO threshold or OFF. The MIC2592B also supplies 3.3V auxiliary outputs (VAUX[A/B]), satisfying PCI Express specifications. These outputs are fed via the VSTBY[A/B] input pins and controlled by the AUXEN[A/B] input pins or via their respective bits in the Control Registers. These

outputs are independent of the MAIN outputs (12VIN[A/B] and 3VIN[A/B]). Should the MAIN supply inputs move below their respective UVLO thresholds, VAUX[A/B] will still function as long as VSTBY[A/B] is present. Prior to standby mode, ONA and ONB (or the Control Registers' MAINA and MAINB bits) inputs should be deasserted or the MIC2592B will assert /FAULT[A/B] and /INT (if interrupts are enabled) output signals, if an undervoltage condition on the MAIN supply inputs is detected.

Circuit Breaker Function

The MIC2592B provides an electronic circuit breaker function that protects against excessive loads, such as short circuits, at each supply. When the current from one or more of a slot's MAIN outputs exceeds the current limit threshold (I_{LIM} = 50mV/R_{SENSE}) for a duration greater than t_{FLT}, the circuit breaker is tripped and both MAIN supplies (all outputs except VAUX[A/B]) are shut off. Should the load current cause a MAIN output's V_{SENSE} to exceed V_{THFAST}, the outputs are immediately shut off with no delay. Undervoltage conditions on the MAIN supply inputs also trip the circuit breaker, but only when the MAIN outputs are enabled (to signal a supply input brown-out condition).

The VAUX[A/B] outputs have a different circuit-breaker function. The VAUX[A/B] circuit breakers do not incorporate a fast-trip detector, instead they regulate the output current into a fault to avoid exceeding their operating current limit. The circuit breaker will trip due to an overcurrent on VAUX[A/B] when the fault timer expires. This use of the t_{FLT} timer prevents the circuit breaker from tripping prematurely due to brief current transients.

Following a fault condition, the outputs can be turned on again via the ON inputs (if the fault occurred on one of the MAIN outputs), via the AUXEN inputs (if the fault occurred on the AUX outputs), or by cycling both ON and AUXEN (if faults occurred on both the MAIN and AUX outputs). A fault condition can alternatively be cleared under SMI control of the ENABLE bits in the CNTRL[A/B] registers (see Register Bits D[1:0]). When the circuit breaker trips, /FAULT[A/B] will be asserted if the outputs were enabled through the Hot-Plug Interface inputs. At the same time, /INT will be asserted (unless interrupts are masked). Note that /INT is deasserted by writing a Logic 1 back into the respective fault bit position(s) in the STAT[A/B] register or the Common Status Register.

The response time (t_{FLT}) of the MIC2592B's primary overcurrent detector is set by external capacitors at the CFILTER[A/B] pins to GND. For Slot A, CFILTER[A] is located at Pin 2; for Slot B, CFILTER[B] is located at Pin 35. For a given response time, the value for $C_{FILTER[A/B]}$ is given by:

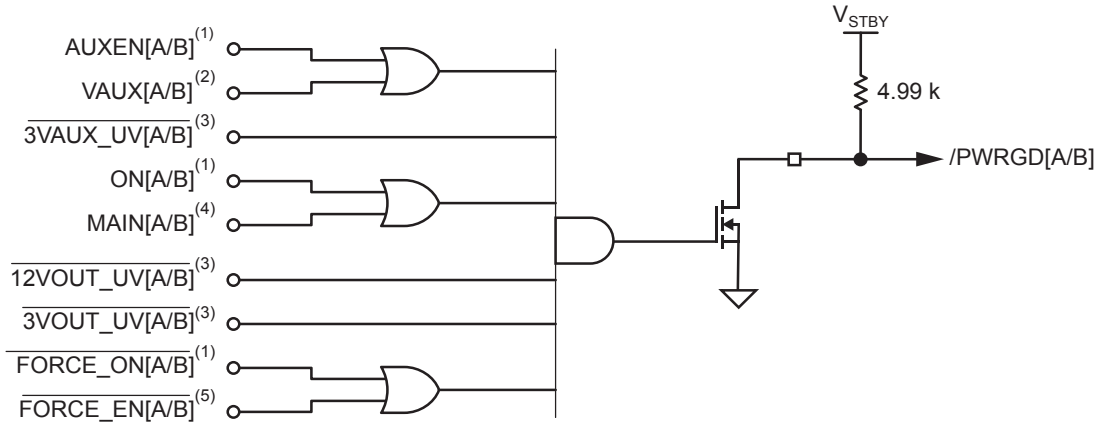
$$C_{FILTER[A/B]}(\mu F) = \frac{t_{FLT[A/B]}(ms) \times I_{FILTER}(\mu A)}{V_{FILTER}(V) \times 10^3}$$

where $t_{FLT[A/B]}$ is the desired response time and quantities I_{FILTER} and V_{FILTER} are specified in the MIC2592B's "Electrical Characteristics" table.

For applications that require a more accurate response time for a given $C_{FILTER[A/B]}$ tolerance, the MIC2592B employs a patent-pending technique that improves response time accuracy by more than a factor of two. A 110kΩ, 1% resistor connected from the MIC2592B's RFILTER[A&B] pin (Pin 20) to GND can be used. In this case, the value for $C_{FILTER[A/B]}$ for a desired response time (t_{FLT}) is given by:

$$C_{FILTER[A/B]}(\mu F) = \frac{t_{FLT}(ms)}{R_{FILTER[A\&B]}(k\Omega) \times SF}$$

where t_{FLT} is the desired response time, $R_{FILTER[A\&B]}$ is 110kΩ, and "SF" is the CFILTER[A/B] response time "Scaling Factor" in the "Electrical Characteristics" table.



(1) External pin
(2) CNTRL[A/B] Register Bit D[0]
(3) Internal flag
(4) CNTRL[A/B] Register Bit D[1]
(5) CNTRL[A/B] Register Bit D[2]

Figure 8. /PWRGD[A/B] Logic Diagram

Thermal Shutdown

The internal VAUX[A/B] MOSFETs are protected against damage not only by current limiting, but by dual-mode overtemperature protection as well. Each slot controller on the MIC2592B is thermally isolated from the other. Should an overcurrent condition raise the junction temperature of one slot's controller and pass elements to 140°C, all of the outputs for that slot (including VAUX) will be shut off and the slot's /FAULT output will be asserted. The other slot's operating condition will remain unaffected. However, should the MIC2592B's die temperature exceed 160°C, both slots (all outputs, including VAUXA and VAUXB) will be shut off, whether or not a current limit condition exists. A 160°C overtemperature condition additionally sets the overtemperature bit (OT_INT) in the Common Status Register.

/PWRGD[A/B] Outputs

The MIC2592B has two /PWRGD outputs, one for each slot. These are open-drain, active-low outputs that require an external pull-up resistor to V_{STBY}. Each output is asserted when a slot has been enabled and has successfully begun delivering power to its respective +12V, +3.3V, and VAUX outputs. An equivalent logic diagram for /PWRGD[A/B] is shown in Figure 8.

/FORCE_ON[A/B] Inputs

These level-sensitive, active-low inputs are provided to facilitate designing systems using the MIC2592B. Asserting /FORCE_ON[A/B] will turn on all three of the respective slot's outputs (+12V, +3.3V, and VAUX), while specifically defeating all protections for those outputs. This explicitly includes all overcurrent and short circuit protections, and on-chip thermal protection for the VAUX supplies. Additionally, asserting a slot's /FORCE_ON[A/B] input will disable all of its input and output UVLO protections, with the sole exception of that asserting either or both of the /FORCE_ON[A/B] inputs will not disable the VSTBY[A/B] input UVLO.

Asserting /FORCE_ON[A/B] will cause the respective slot's /PWRGD[A/B] and /FAULT[A/B] outputs to enter their open-drain state. Additionally, there are two SMBus accessible register bits (see CNTRL[A/B] Register Bit D[2]), which can be set to disable the corresponding slot's /FORCE_ON[A/B] pins. This allows system software to prevent these hardware overrides from being inadvertently activated during normal use. If not used, each pin should be connected to V_{STBY} using an external pull-up resistor. See Figure 6 for details.

General Purpose Input (GPI) Pins

Two pins on the MIC2592B are available for use as GPI pins. The logic state of each of these pins can be determined by polling Bits [4:5] of Common Status Register. Both of these inputs are compliant to 3.3V. If unused, connect each GPI_[A0/B0] pin to GND.

Hot-Plug Interface (HPI)

Once the input supplies are above their respective UVLO thresholds, the Hot-Plug Interface can be utilized for power control by enabling the control input pins (AUXEN[A/B] and ON[A/B]) for each slot. In order for the MIC2592B to switch on the VAUX supply for either slot, the AUXEN[A/B] control must be enabled after the power-on-reset delay, t_{POR} (typically, 250µs), has elapsed. The timing response diagram of Figure 9 illustrates a Hot-Plug Interface operation where an overcurrent fault is detected by the MIC2592B controller after initiating a power-up sequence. The MAIN (+12V & +3.3V) and VAUX[A/B] supply rails, /FAULT, /PWRGD and /INT output responses for both AUX and MAIN are shown in the figure.

System Management Interface (SMI)

The MIC2592B's System Management Interface uses the Read_Byte and Write_Byte subset of the SMBus protocols to communicate with its host via the System Management Interface bus. The /INT output signals the controlling processor that one or more events need attention, if an interrupt-driven architecture is used. Note that the MIC2592B does not participate in the SMBus Alert Response Address (ARA) portion of the SMBus protocol.

Fault Reporting and Interrupt Generation

SMI-only Control Applications

In applications where the MIC2592B is controlled only by the SMI, ON[A/B] and AUXEN[A/B] are connected to GND and the /FORCE_ON[A/B] pins are connected to V_{STBY} as shown in Figure 6. In this case, the MIC2592B's /FAULT[A/B] outputs and STAT[A/B] Register Bit D[7] (FAULT[A/B]) are not activated as fault status is determined by polling STAT[A/B] Register Bits D[4], D[2], D[0] and CS (Common Status) Register Bits D[2:1]. Individual fault bits in STAT[A/B] and CS registers are asserted after power-on-reset when:

- Either or both CNTRL[A/B] Register Bits D[1:0] are asserted, AND
- 12VIN[A/B], 3VIN[A/B], or VSTBY[A/B] input voltage is lower than its respective ULVO threshold, OR
- The fast OC circuit breaker[A/B] has tripped, OR
- The slow OC circuit breaker[A/B] has tripped AND its filter timeout has expired, OR
- The slow OC circuit breaker[A/B] has tripped AND Slot[A/B] die temperature > 140°C, OR
- The MIC2592B's global die temperature > 160°C

To clear any one or all STAT[A/B] Register Bits D[4], D[2], D[0] and/or CS Register Bits D[2], D[1] once asserted, a software subroutine can perform an "echo reset" where a Logical "1" is written back to those register bit locations that have indicated a fault. This method of "echo reset" allows data to be retained in the STAT[A/B] and/or CS registers until such time as the system is prepared to operate on that data.

The MIC2592B can operate in interrupt mode or polled mode. For interrupt-mode operation, the open-drain, active-LOW /INT output signal is activated after power-on-reset if the INTMSK bit (CS Register Bit D[3]) has been reset to Logical "0". Once activated, the /INT output is asserted by any one of the fault conditions listed above and deasserted when one or all STAT[A/B] Register Bits D[4], D[2], D[0] and/or CS Register Bits D[2], D[1] are reset upon the execution of an SMBus "echo reset" WRITE_BYTE cycle. For polled-mode operation, the INTMSK bit should be set to Logical "1," thereby inhibiting /INT output pin operation.

For those SMI-control applications where the /FORCE_ON[A/B]

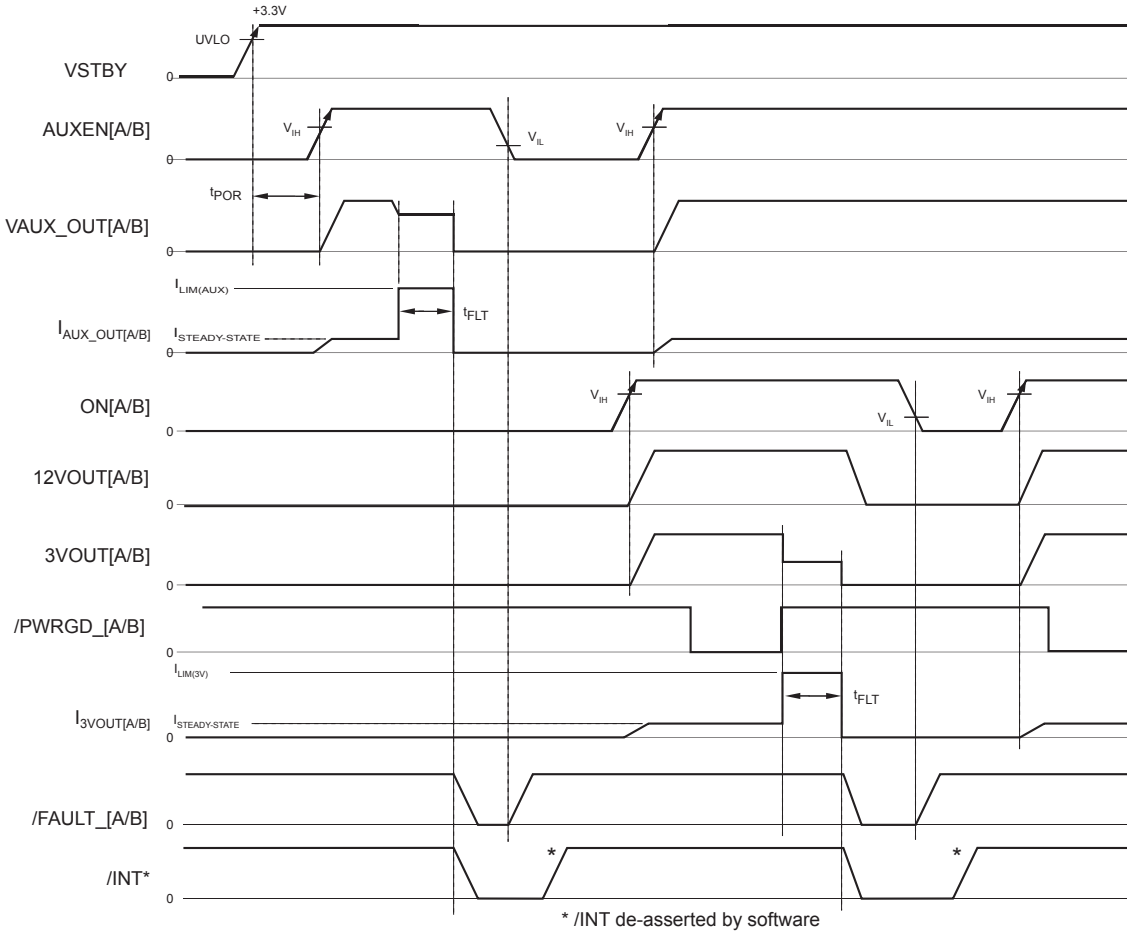


Figure 9. Hot-Plug Interface Operation

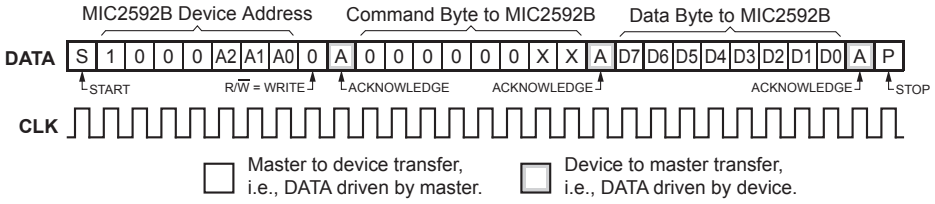


Figure 10. WRITE_BYTE Protocol

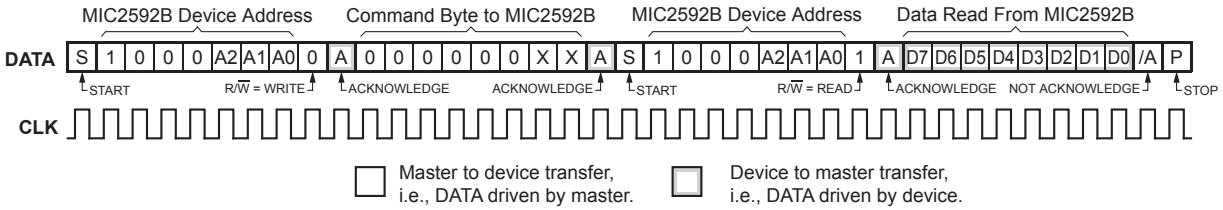


Figure 11. READ_BYTE Protocol

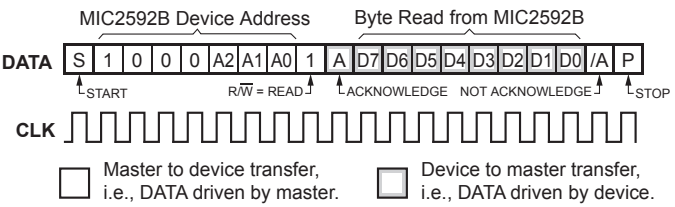


Figure 12. RECEIVE_BYTE Protocol

inputs are needed for diagnostic purposes, the /FORCE_ON[A/B] inputs must be enabled; that is, CNTRL[A/B] Register Bit D[2] should read Logical "0." Once /FORCE_ON[A/B] inputs are asserted, all output voltages are present with all circuit protection features disabled, including overtemperature protection on VAUX[A/B] outputs. To inhibit /FORCE_ON[A/B] operation, a Logical "1" shall be written to the CNTRL[A/B] Register Bit D[2] location(s).

HPI-only Control Applications

In applications where the MIC2592B is controlled only by the HPI, SMBus signals SCL, SDA, and /INT signals are connected to V_{STBY} as shown in Figure 6. In this configuration, the MIC2592B's /FAULT[A/B] outputs are activated after power-on-reset and become asserted when:

Either or both external ON[A/B] and AUXEN[A/B] input signals are asserted, AND

- 12VIN[A/B], 3VIN[A/B], or VSTBY[A/B] input voltage is lower than its respective ULVO threshold, OR
- The fast OC circuit breaker[A/B] has tripped, OR
- The slow OC circuit breaker[A/B] has tripped AND its filter timeout[A/B] has expired, OR
- The slow OC circuit breaker[A/B] has tripped AND Slot[A/B] die temperature > 140°C, OR
- The MIC2592B's global die temperature > 160°C

In order to clear /FAULT[A/B] outputs once asserted, either or both ON[A/B] and AUXEN[A/B] input signals must be deasserted. Please see /FAULT[A/B] pin description for additional information.

If the /FORCE_ON[A/B] inputs are used for diagnostic purposes, both /FAULT[A/B] and /PWRGD[A/B] outputs are deasserted once /FORCE_ON[A/B] inputs are asserted.

Serial Port Operation

The MIC2592B uses standard SMBus Write_Byte and Read_Byte operations for communication with its host. The SMBus Write_Byte operation involves sending the device's target address, with the R/$\overline{W}$ bit (LSB) set to the low (write) state, followed by a command byte and a data byte. The SMBus Read_Byte operation is similar, but is a composite write and read operation: the host first sends the device's target address followed by the command byte, as in a write operation. A new "Start" bit must then be sent to the MIC2592B, followed by a repeat of the device address with the R/$\overline{W}$ bit set to the high (read) state. The data to be read from the part may then be clocked out. There is one exception to this rule: If the location latched in the pointer register from the last write operation is known to be correct (i.e., points to the desired register within the MIC2592B), then the "Receive_Byte" procedure may be used. To perform a Receive_Byte operation, the host sends an address byte to select the target MIC2592B, with the R/$\overline{W}$ bit set to the high (read) state, and then retrieves the data byte. Figures 10 through 12 show the formats for these data read and data write procedures.

The Command Register is eight bits (one byte) wide. This byte carries the address of the MIC2592B's register to be operated upon. The command byte values corresponding to the various MIC2592B register addresses are shown in Table 2. Command byte values other than $0000\ 0XXX_b = 00_h - 07_h$ are reserved and should not be used.

MIC2592B SMBus Address Configuration

The MIC2592B responds to its own unique SMBus address, which is assigned using A2, A1, and A0. These represent the 3 LSBs of its 7-bit address, as shown in Table 3. These address bits are assigned only during power up of the VSTBY[A/B] supply input. These address bits allow up to eight MIC2592B devices in a single system. These pins are either grounded or left unconnected to specify a logical 0 or logical 1, respectively. A pin designated as a logical 1 may also be pulled up to V_{STBY}.

Inputs			MIC2592B Device Address	
A2	A1	A0	Binary	Hex
0	0	0	$1000\ 000X^*_b$	80_h
0	0	1	$1000\ 001X_b$	82_h
0	1	0	$1000\ 010X_b$	84_h
0	1	1	$1000\ 011X_b$	86_h
1	0	0	$1000\ 100X_b$	88_h
1	0	1	$1000\ 101X_b$	$8A_h$
1	1	0	$1000\ 110X_b$	$8C_h$
1	1	1	$1000\ 111X_b$	$8E_h$

* Where X = "1" for READ and "0" for Write

Table 3. MIC2592B SMBus Addressing

MIC2592B Register Set and Programmer's Model

Target Register		Command Byte Value		Power-On Default
Label	Description	Read	Write	
CNTRLA	Control Register Slot A	02_h	02_h	00_h
CNTRLB	Control Register Slot B	03_h	03_h	00_h
STATA	Slot A Status	04_h	04_h	00_h
STATB	Slot B Status	05_h	05_h	00_h
CS	Common Status Register	06_h	06_h	$xxxx\ 0000_b$
Reserved	Reserved / Do Not Use	$07h - FF_h$	$07h - FF_h$	Undefined

Table 2. MIC2592B Register Addresses

Detailed Register Descriptions

Control Register, Slot A (CNTRLA)

8-Bits, Read/Write

Control Register, Slot A (CNTRLA)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read only	read only	read-only	read/write	read/write	read/write
AUXAPG	MAINAPG	Reserved	Reserved	Reserved	/FORCE_A ENABLE	MAINA	VAUXA

Bit(s)	Function	Operation
AUXAPG	AUX output power-good status, Slot A	1 = Power-is-Good (VAUXA Output is above its UVLO threshold)
MAINAPG	MAIN output power-good status, Slot A	1 = Power-is-Good (MAINA Outputs are above their UVLO thresholds)
D[5]	Reserved	Always read as zero
D[4]	Reserved	Always read as zero
D[3]	Reserved	Always read as zero
/FORCE_A ENABLE	Allows or inhibits the operation of the /FORCE_ONA input pin	0 = /FORCE_ONA is enabled 1 = /FORCE_ONA is disabled
MAINA	MAIN enable control, Slot A	0 = Off, 1 = On
VAUXA	VAUX enable control, Slot A	0 = Off, 1 = On

Power-Up Default Value: 0000 0000b = 00h
Read Command_Byte Value (R/W): 0000 0010b = 02h

The power-up default value is 00h. Slot is disabled upon power-up, i.e., all supply outputs are off.

Notes:

1. The state of the /PWRGDA pin is the logical AND of the values of the AUXAPG and the MAINAPG bits, except when /FORCE_ONA is asserted. If /FORCE_ONA is asserted (the pin is pulled low), and /FORCE_AENABLE is set to a logic zero, the /PWRGDA pin will be unconditionally forced to its open-drain (“Power Not Good”) state.

Control Register, Slot B (CNTRLB)

8-Bits, Read/Write

Control Register, Slot B (CNTRLB)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read only	read only	read-only	read/write	read/write	read/write
AUXBPG	MAINBPG	Reserved	Reserved	Reserved	/FORCE_B ENABLE	MAINB	VAUXB

Bit(s)	Function	Operation
AUXBPG	AUX output power-good status, Slot B	1 = Power-is-Good (VAUXB Output is above its UVLO threshold)
MAINBPG	MAIN output power-good status, Slot B	1 = Power-is-Good (MAINB Outputs are above their UVLO thresholds)
D[5]	Reserved	Always read as zero
D[4]	Reserved	Always read as zero
D[3]	Reserved	Always read as zero
/FORCE_B ENABLE	Allows or inhibits the operation of the /FORCE_ONB input pin	0 = /FORCE_ONB is enabled 1 = /FORCE_ONB is disabled
MAINB	MAIN enable control, Slot B	0 = Off, 1 = On
VAUXB	VAUX enable control, Slot B	0 = Off, 1 = On

Power-Up Default Value: 0000 0000b = 00h
Command_Byte Value (R/W): 0000 0011b = 03h

The power-up default value is 00h. Slot is disabled upon power-up, i.e., all supply outputs are off.

Notes:

1. The state of the /PWRGDB pin is the logical AND of the values of the AUXBPG and the MAINBPG bits, except when /FORCE_ONB is asserted. If /FORCE_ONB is asserted (the pin is pulled low), and /FORCE_BENABLE is set to a logic zero, the /PWRGDB pin will be unconditionally forced to its open-drain (“Power Not Good”) state.

Status Register Slot A (STATA)

8-Bits, Read-Only

Status Register, Slot A (STATA)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read/write	read-only	read/write	read-only	read/write
FAULTA	MAINA	VAUXA	VAUXAF	Reserved	12VAF	Reserved	3VAF

Bit(s)	Function	Operation
FAULTA	FAULT Status - Slot A	1 = Fault pin asserted (/FAULTA pin is LOW) 0 = Fault pin deasserted (/FAULTA pin is HIGH) See Notes 1, 2, and 3.
MAINA	MAIN Enable Status - Slot A two Main Power outputs for Slot A	Represents the actual state (on/off) of the (+12V and +3.3V) 1 = Main Power ON 0 = Main Power OFF
VAUXA	VAUX Enable Status - Slot A Auxiliary Power output for Slot A	Represents the actual state (on/off) of the 1 = AUX Power ON 0 = AUX Power OFF
VAUXAF	Overcurrent Fault: VAUXA supply	1 = Fault 0 = No fault
D[3]	Reserved	Always read as zero
12VAF	Overcurrent Fault: +12V supply	1 = Fault 0 = No fault
D[1]	Reserved	Always read as zero
3VAF	Overcurrent Fault: 3.3V supply	1 = Fault 0 = No fault

Power-Up Default Value: 0000 0000b = 00h
Command_Byte Value (R/W): 0000 0100b = 04h

The power-up default value is 00h. Both slots are disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and deassert /INT. The status of the /FAULTA pin is not affected by reading the Status Register or by clearing active status bits.

Notes:

1. If FAULTA has been set by an overcurrent condition on one or more of the MAIN outputs, the ONA input must go LOW to reset FAULTA.

   If FAULTA has been set by a VAUXA overcurrent event, the AUXENA input must go LOW to reset FAULTA.

   If an overcurrent has occurred on both a MAIN output and the VAUX output of slot A, both ONA and AUXENA of the slot must go low to reset FAULTA.
2. Neither the FAULTA bits nor the /FAULTA pins are active when the MIC2592B power paths are controlled by the System Management Interface. When using SMI power path control, AUXENA and ONA pins for that slot must be tied to GND.

Status Register Slot B (STATB)

8-Bits, Read-Only

Status Register, Slot B (STATB)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read/write	read-only	read/write	read-only	read/write
FAULTB	MAINB	VAUXB	VAUXBF	Reserved	12VBF	Reserved	3VBF

Bit(s)	Function	Operation
FAULTB	FAULT Pin Status - Slot B	1 = Fault pin asserted (/FAULTB pin is LOW) 0 = Fault pin deasserted (/FAULTB pin is HIGH) See Notes 1, 2, and 3.
MAINB	MAIN Enable Status - Slot B	Represents the actual state (on/off) of the four Main Power outputs for Slot B (+12V and +3.3V) 1 = MAIN Power ON 0 = MAIN Power OFF
VAUXB	VAUX Enable Status - Slot B	Represents the actual state (on/off) of the Auxiliary Power output for Slot B 1 = AUX Power ON 0 = AUX Power OFF
VAUXBF	Overcurrent Fault: VAUXB supply	1 = Fault 0 = No fault
D[3]	Reserved	Always read as zero
12VBF	Overcurrent Fault: +12V supply	1 = Fault 0 = No fault
D[1]	Reserved	Always read as zero
3VBF	Overcurrent Fault: 3.3V supply	1 = Fault 0 = No fault

Power-Up Default Value: 0000 0000b = 00h
Command_Byte Value (R/W): 0000 0101b = 05h

The power-up default value is 00h. Both slots are disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and deassert /INT. The status of the /FAULTB pin is not affected by reading the Status Register or by clearing active status bits.

Notes:

1. If FAULTB has been set by an overcurrent condition on one or more of the MAIN outputs, the ONB input must go LOW to reset FAULTB.

   If FAULTB has been set by a VAUXB overcurrent event, the AUXENB input must go LOW to reset FAULTB.

   If an overcurrent has occurred on both a MAIN output and the VAUX output of slot B, both ONB and AUXENB of the slot must go low to reset FAULTB.
2. Neither the FAULTB bits nor the /FAULTB pins are active when the MIC2592B power paths are controlled by the System Management Interface. When using SMI power path control, the AUXENB and ONB pins for that slot must be tied to GND.

3:. If /FORCE_ONB is asserted (low), the /FAULTB pin will be unconditionally forced to its open-drain state. Note, though, that the value in the FAULTB

Common Status Register (CS)

8-Bits, Read/Write

Common Status Register (CS)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-write	read-write	read-only	read-only	read-write	read-write	read-write	read-only
Reserved	Reserved	GPI_B0	GPI_A0	INTMSK	UV_INT	OT_INT	Reserved

Bit(s)	Function	Operation
D[7]	Reserved	Always read as zero
D[6]	Reserved	Always read as zero
GPI_B0	General Purpose Input 0, Slot B	State of GPI_B0 pin
GPI_A0	General Purpose Input 0, Slot A	State of GPI_A0 pin
INTMSK	Interrupt Mask	0 = /INT generation is enabled 1 = /INT generation is disabled. The MIC2592B does not participate in the SMBus Alert Response Address (ARA) protocol
UV_INT	Undervoltage Interrupt	0 = No UVLO fault 1 = UVLO fault Set whenever a circuit breaker fault condition occurs as a result of an undervoltage lockout condition on one of the main supply inputs. This bit is only set if a UVLO condition occurs while the ON[A/B] pin is asserted or the MAIN[A/B] control bits are set
OT_INT	Overtemperature Interrupt	0 = Die Temp < 160°C. 1 = Fault: Die Temp > 160°C. Set if a fault occurs as a result of the MIC2592B's die temperature exceeding 160°C
D[0]	Reserved	Undefined

Power-Up Default Value: 00000000b = 00h
Command_Byte Value (R/W): 00000110b = 06h

Applications Information

Sense Resistor Selection

The 12V and the 3.3V supplies employ internal current sensing circuitry to detect overcurrent conditions that may trip the circuit breaker. An external sense resistor is used to monitor the current that passes through the external MOSFET for each slot of the 12V and 3.3V rails. The sense resistor is nominally valued at:

$$R_{SENSE(NOM)} = \frac{V_{THILIMIT}}{I_{LIMIT}}$$

where $V_{THILIMIT}$ is the typical (or nominal) circuit breaker threshold voltage (50mV) and I_{LIMIT} is the nominal inrush load current level to trip the internal circuit breaker.

To accommodate worse-case tolerances in the sense resistor (for a ±1% initial tolerance, allow ±3% tolerance for variations over time and temperature) and circuit breaker threshold voltages, a slightly more detailed calculation must be used to determine the minimum and maximum hot swap load currents.

As the MIC2592B's minimum current limit threshold voltage is 45mV, the minimum hot swap load current is determined where the sense resistor is 3% high:

$$I_{LIMIT(MIN)} = \frac{45mV}{(1.03 \times R_{SENSE(NOM)})} = \frac{43.7mV}{R_{SENSE(NOM)}}$$

Keep in mind that the minimum hot swap load current should be greater than the application circuit's upper steady-state load current boundary. Once the lower value of R_{SENSE} has been calculated, it is good practice to check the maximum hot swap load current ($I_{LIMIT(MAX)}$) which the circuit may let pass in the case of tolerance build-up in the opposite direction. Here, the worse-case maximum is found using a $V_{THILIMIT(MAX)}$ threshold of 55mV and a sense resistor 3% low in value:

$$I_{LIMIT(MAX)} = \frac{55mV}{(0.97 \times R_{SENSE(NOM)})} = \frac{56.7mV}{R_{SENSE(NOM)}}$$

In this case, the application circuits must be sturdy enough to operate up to approximately 1.25x the steady-state hot swap load currents. For example, if one of the 12V slots of the MIC2592B circuit must pass a minimum hot swap load current of 1.5A without nuisance trips, R_{SENSE} should be set to:

$$R_{SENSE(NOM)} = \frac{45mV}{1.5A} = 30m\Omega$$

where the nearest 1% standard value is 30.1mΩ. At the other tolerance extremes, $I_{LIMIT(MAX)}$ for the circuit in question is then simply:

$$I_{LIMIT(MAX)} = \frac{56.7mV}{30.1m\Omega} = 1.88A$$

With a knowledge of the application circuit's maximum hot swap load current, the power dissipation rating of the sense resistor can be determined using $P = I^2R$. Here, the current is $I_{LIMIT(MAX)}$ = 1.88A and the resistance $R_{SENSE(MAX)}$ = $(1.03)(R_{SENSE(NOM)})$ = 31.00mΩ. Thus, the sense resistor's maximum power dissipation is:

$P_{MAX} = (1.88A)^2 \times (31.00m\Omega) = 0.110W$

A 0.25W sense resistor is a good choice in this application.

PCB Layout Suggestions and Hints

4-Wire Kelvin Sensing

Because of the low value required for the sense resistor, special care must be used to accurately measure the voltage drop across it. Specifically, the measurement technique across R_{SENSE} must employ 4-wire Kelvin sensing. This is simply a means of ensuring that any voltage drops in the power traces connected to the resistors are not picked up by the signal conductors measuring the voltages across the sense resistors.

Figure 13 illustrates how to implement 4-wire Kelvin sensing. As the figure shows, all the high current in the circuit (from V_{IN} through R_{SENSE} and then to the drain of the N-channel power MOSFET) flows directly through the power PCB traces and through R_{SENSE}. The voltage drop across R_{SENSE} is sampled in such a way that the high currents through the power traces will not introduce significant parasitic voltage drops in the sense leads. It is recommended to connect the hot swap controller's sense leads directly to the sense resistor's metalized contact pads. The Kelvin sense signal traces should be symmetrical with equal length and width, kept as short as possible, and isolated from any noisy signals and planes.

Additionally, for designs that implement Kelvin sense connections that exceed 1" in length and/or if the Kelvin (signal) traces are vulnerable to noise possibly being injected onto these signals, the example circuit shown in Figure 14 can be implemented to combat noisy environments. This circuit implements a 1.6 MHz low-pass filter to attenuate higher frequency disturbances on the current sensing circuitry. However, individual system analysis should be used to determine if filtering is necessary and to select the appropriate cutoff frequency for each specific application.

Other Layout Considerations

Figure 15 is a suggested PCB layout diagram for the MIC2592B power traces, Kelvin sense connections, and capacitor components. In this illustration, only the 12V Slot B is shown but a similar approach is suggested for both slots of each Main power rail (12V and 3.3V). Many hot swap applications will require load currents of several amperes. Therefore, the power (12VIN and Return, 3VIN and Return) trace widths (W) need to be wide enough to allow the current to flow while the rise in temperature for a given copper plate (e.g., 1oz. or 2oz.) is kept to a maximum of 10°C to 25°C. The return (or power ground) trace should be the same width as the positive voltage power traces (input/load) and isolated from any ground and signal planes so that the controller's power is common mode. Also, these traces should be as short as possible in order to minimize the IR drops between the input and the load. As indicated in the Pin Description section, an external connection must be made that ties together both channel inputs ((+) Kelvin sense) of each Main power rail (i.e., 3VINA and 3VINB, 12VINA and 12VINB must be externally connected). These connections should be implemented directly at the chip. Insure that the voltage drop between the two (+) Kelvin sense inputs for each rail is no greater than 0.2mV by using a common power path for the two inputs

(e.g., 12VINA, 12VINB). Finally, the use of plated-through vias will be necessary to make circuit connection to the power, ground, and signal planes on multi-layer PCBs.

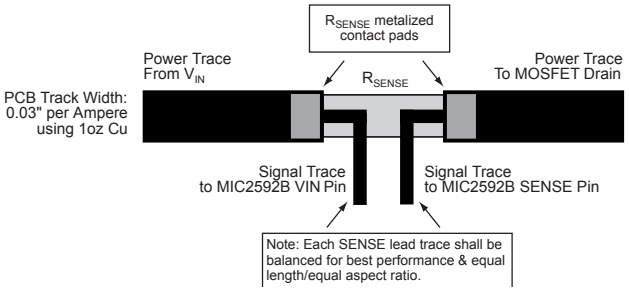


Figure 13. 4-Wire Kelvin Sense Connections for R_{SENSE}

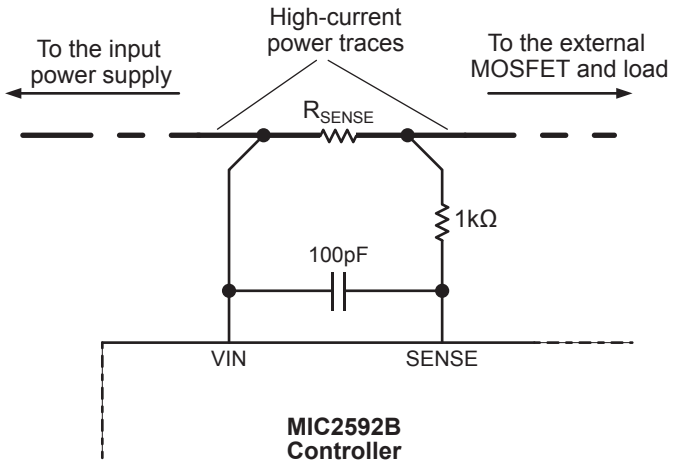
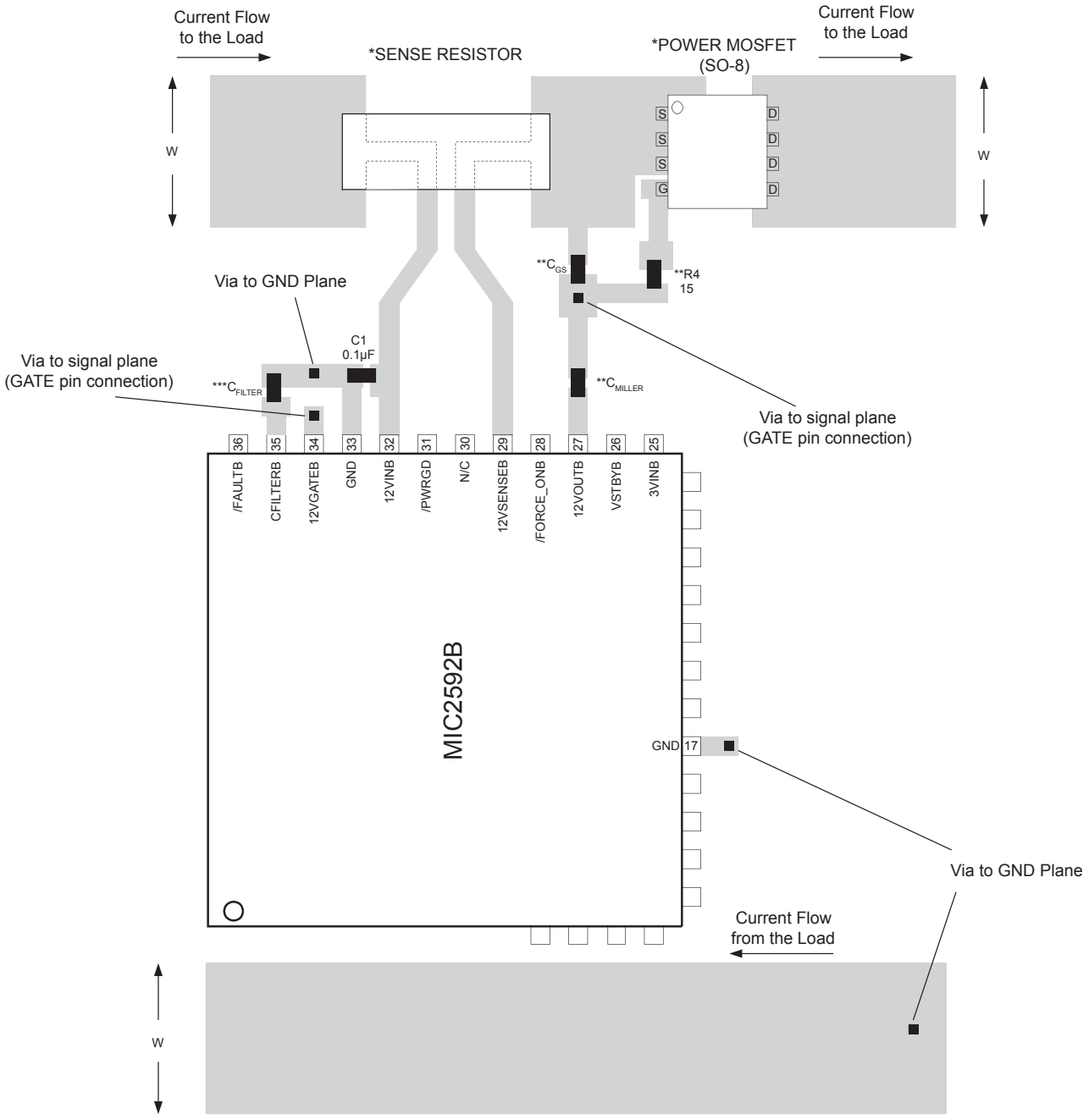


Figure 14. Current Limit Sense Filter for Noisy Systems



- DRAWING IS NOT TO SCALE AND NOT ALL PINS SHOWN FOR CLARITY-
*See Table 4 for part numbers and vendors
**Optional components
***Recommended components (variable in value, see Functional Description and Applications Information)
Trace width (W) guidelines given in "PCB Layout Recommendations" section of the datasheet
12V(Slot B) is illustrated in this example. A similar layout is suggested for the 3V supply and both slots

Figure 15. Suggested PCB Layout for Sense Resistor, Power MOSFET, and Capacitors

MOSFET and Sense Resistor Vendors

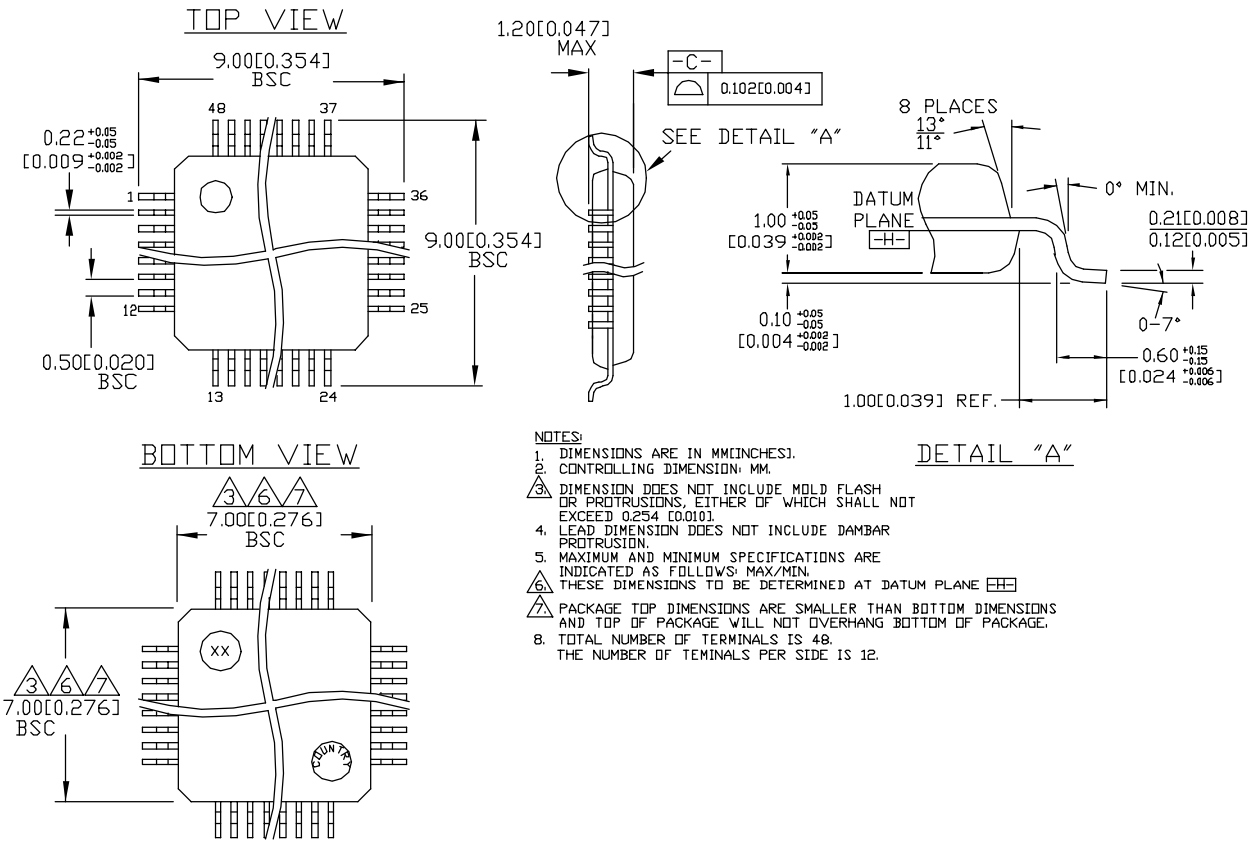
Device types, part numbers, and manufacturer contact information for power MOSFETs and sense resistors are provided in Table 4. Some of the recommended MOSFETs include a metal (tab) heat sink on the bottom side of the package. Contact the device manufacturer for package information.

MOSFET Vendors	Key Power MOSFET Type(s)		Package	Contact Information
	N-Channel	P-Channel		
Vishay - Siliconix	Si4420DY	Si4435BDY	SO-8	www.siliconix.com
	Si4442DY	Si4427BDY	SO-8	(203) 452-5664
	Si3442DV	Si4405DY	SO-8	
	Si4410DY	Si4425BDY	SO-8	
	Si7860ADP	Si7483ADP	PowerPAK SO-8	
	Si7344DP	Si7491DP	PowerPAK SO-8	
	Si7844DP (Dual)	Si7945DP (Dual)	PowerPAK SO-8	
	Si7114DN	Si7423DN	1212 SO-8	
	Si7806ADN	Si7421DN	1212 SO-8	
International Rectifier	IRF7882	IRF7424	SO-8	www.irf.com
	IRF7413	IRF7416	SO-8	(310) 322-3331
	IRF7313 (Dual)	IRF7328 (Dual)	SO-8	

Resistor Vendors	Sense Resistors	Contact Information
Vishay - Dale	“WSL” and “WSR” Series	www.vishay.com/docswsl_30100.pdf (203) 452-5664
IRC	“OARS” Series “LR” Series second source to “WSL”	www.irctt.com/pdf_files/OARS.pdf www.irctt.com/pdf_files/LRC.pdf (828) 264-8861

Table 4. MOSFET and Sense Resistor Vendors

Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. TOTAL NUMBER OF TERMINALS IS 48. THE NUMBER OF TEMINALS PER SIDE IS 12.

48-Pin TQFP

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