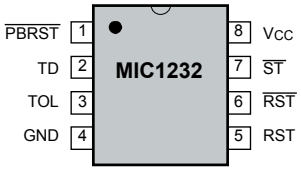
Pin Configuration



8-Pin PDIP Package
8-Pin SOIC Package

Pin Description

Pin Number	Pin Name	Pin Function
1	/PBRST	Pushbutton Reset Input: This input is debounced and can be driven with external logic signals or by means of a mechanical pushbutton to actively force a reset. All pulses less than 1ms in duration on the /PBRST pin are ignored, whereas, any pulse with a duration of 20ms or greater is guaranteed to cause a reset.
2	TD	Time Delay input: This input selects the timebase used by the watchdog timer. When TD = 0V, the watchdog timeout period is set to a normal value of 150ms, when TD = open, the watchdog timeout period is et to a nominal value of 600ms and when TD = V_{CC}, the watchdog period is 1.2s nominally.
3	TOL	Tolerance Select Input: Selects whether 5% or 10% of VCC is used as the reset threshold voltage. When TOL = 0V, the 5% tolerance level is selected and when TOL = V_{CC}, a 10% tolerance level is selected.
4	GND	IC ground pin, 0V reference
5	RST	RST is asserted high if either V_{CC} goes below the reset threshold, the watchdog times out or /PBRST is pulled low for a minimum of 20ms. RST remains asserted for one reset timeout period after VCC exceeds the reset threshold or after the watch times out or after /PBRST goes high.
6	/RST	/RST is asserted low if either V_{CC} goes below the reset threshold, the watchdog times out or /PBRST is pulled low for a minimum of 20ms. /RST remains asserted for one reset timeout period after V_{CC} exceeds the reset threshold or after the watch times out or after /PBRST goes high. Open-drain output
7	/ST	Input to watchdog timer. If /ST does not see a transition from high to low within the watchdog timeout period, RST and /RST will be asserted.
8	VCC	Primary supply input, +5V

Absolute Maximum Ratings (Note 1)

Terminal Voltage

V_{CC} .....–0.3V to +6.0V
All other inputs.....–0.3V to (V_{CC} + 0.3V)

Input Current

VCC 250mA
GND, all other inputs 25mA

Lead Temperature (soldering, 10 sec.)..... 300°C

Storage Temperature..... –65°C to 150°C

ESD Rating, **Note 3**

Operating Ratings (Note 2)

Operating Temperature Range

MIC1232M/N ..... –40°C to 85°C

Electrical Characteristics

V_{CC} = 4.5V to 5.5V; T_A = Operating Temperature Range, **bold** values indicate –40°C ≤ T_A ≤ +85°C; unless noted

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range	V_{CC}	4.5		5.5	V
Supply Current	I_{CC}, **(Note 4)**		18	40	µA
/ST and /PBRST Input Levels	V_{IH}, **(Note 5)**	2.0		V_{CC}+0.3	V
	V_{IL}	–0.3		0.8	V
Input Leakage	I_{IL}			±1	µA
Output Souce Current, RST	V_{OH} = 2.4V	1.0	10		mA
Output Sink Current, /RST. RST	V_{OL} = 0.4V	2.0	10		mA
V_{CC} 5% Trip Point (Reset Threshold Voltage)	TOL = GND	4.5	4.62	4.74	V
V_{CC} 10% Trip Point (Reset Threshold Voltage)	TOL = V_{CC}	4.25	4.37	4.49	V
Input Capacitance, /ST, TOL	C_{IN}, **(Note 6)**			5	pF
Output Capacitance, /RST, RST	C_{OUT}, **(Note 6)**			7	pF

AC Electrical Characteristics

V_{CC} = 4.5V to 5.5V; T_A = Operating Temperature Range, **bold** values indicate –40°C ≤ T_A ≤ +85°C; unless noted

/PBRST Min. Pulse Width, t_{PB}	/PBRST = V_{IL} **(Note 7)**	20			ms
/PBRST Delay, t_{PBD}		1	4	20	ms
Reset Active Time, t_{RST}		250	610	1000	ms
/ST Pulse Width, t_{ST}		20			ms
/ST Timeout Period, t_{TD}	TD = 0V	62.5	150	250	ms
	TD = Open	250	600	1000	ms
	TD = V_{CC}	500	1200	2000	ms
V_{CC} Fall Time, t_F		10			µs
V_{CC} Rise Time, t_R		0			ns
V_{CC} Detect to /RST Low and RST High, t_{RPD}	V_{CC} Falling **(Note 8)**		50	150	µs
V_{CC} Detect to /RST Low and RST Low, t_{RPD}	V_{CC} Falling **(Note 9)**	250	610	1000	µs

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4. I_{CC} is measured with outputs open and inputs within 0.5V of supply rails

Note 5. /PBRST has an internal pull-up resistor to V_{CC} (typ. 40kΩ)

Note 6. Guaranteed by design

Note 7. /PBRST must be held low for a minimum of 20ms to guarantee a reset

Note 8. V_{CC} falling at 1.66mV/µs

Note 9. /RST has an open drain output

Timing Diagrams

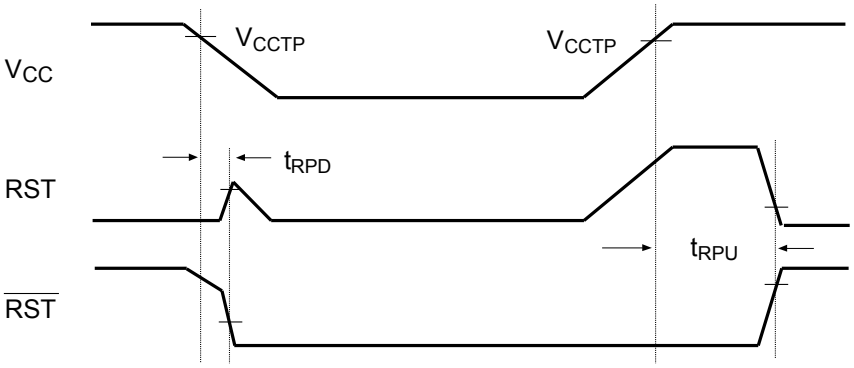


Figure 1. Power-Up/Power-Down Sequence

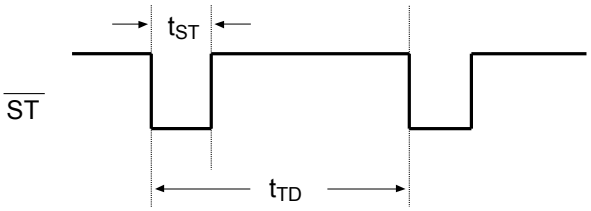


Figure 2. Watchdog Input

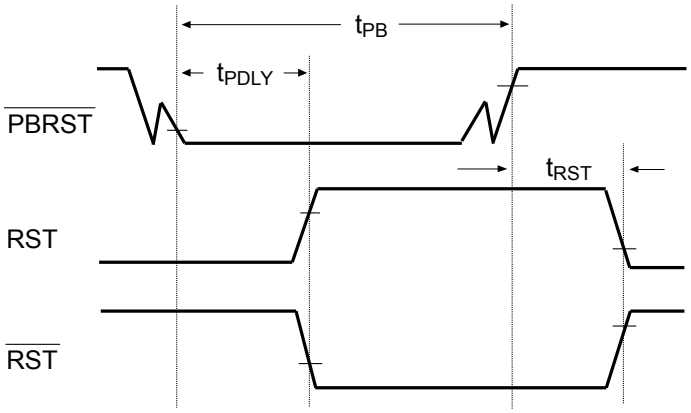


Figure 3. Pushbutton Reset

Applications Information

Power Monitor

The /RST and RST pins are asserted whenever V_{CC} falls below the reset threshold voltage as determined by the TOL pin. A 5% tolerance level (4.62V reset threshold voltage) can be selected by connecting the TOL pin to ground and a 10% tolerance can be selected by connecting the TOL pin to V_{CC}. The reset pins will remain asserted for a period of 250ms after V_{CC} has risen above the reset threshold voltage. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. /RST will remain valid with V_{CC} as low as 1.4V.

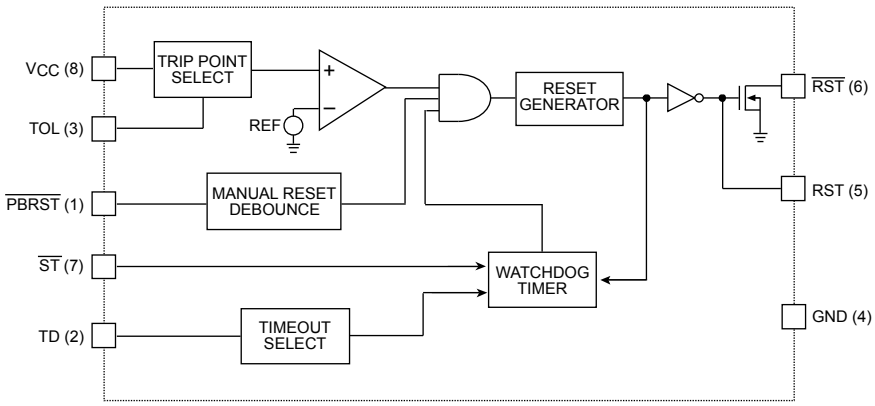
Watchdog Timer

The microprocessor can be mounted by connecting the /ST pin (watchdog input) to a bus line or I/O line. If a high-to-low does not occur on the/ST pin within the watchdog timeout period (determined by the TD pin, see Table 1.), the /RST and the RST will remain asserted for 250ms when this occurs. A minimum pulse of 75ns or any transition high-to-low on the /ST pin will reset the watchdog timer. The watchdog timer will be reset if /ST sees a valid transition within the watchdog timeout period.

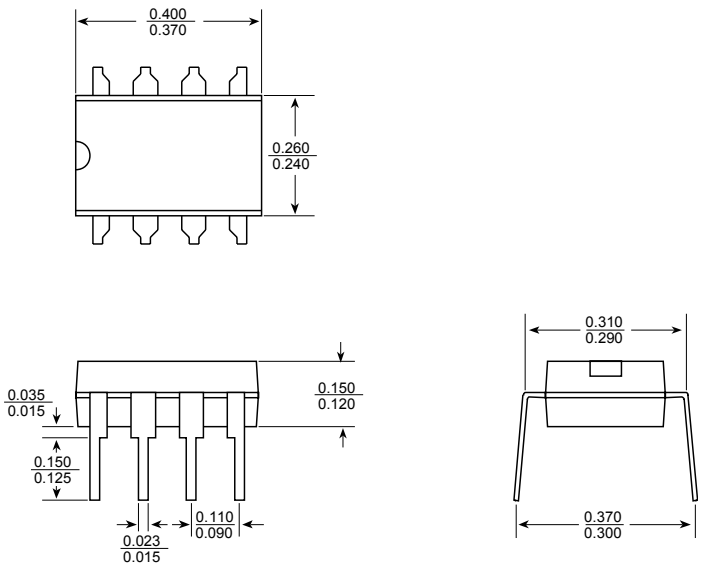
Pushbutton Reset Input

The /PBRST input can be driven with a manual pushbutton switch or with external logic signals. the input is internally debounced and requires an active low signal to force the reset outputs into their active states. The /PBRST input will recognize any pulse that is 20ms in duration or greater and will ignore all pulses that are less than 1ms in duration.

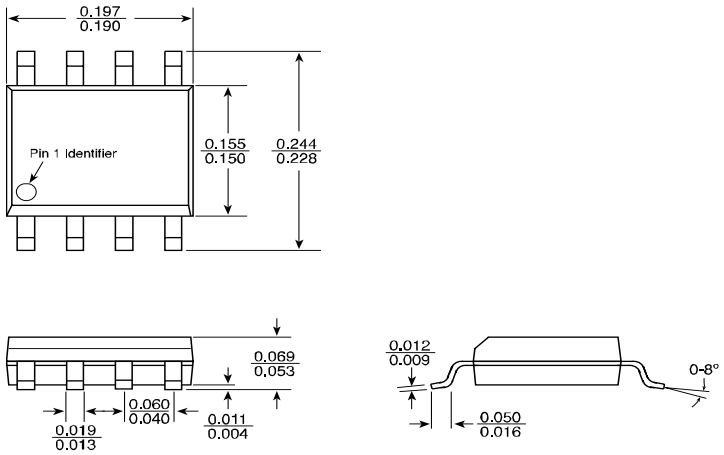
Block Diagram



Package Information



8-Pin PDIP (N)



8-Pin SOIC (M)

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