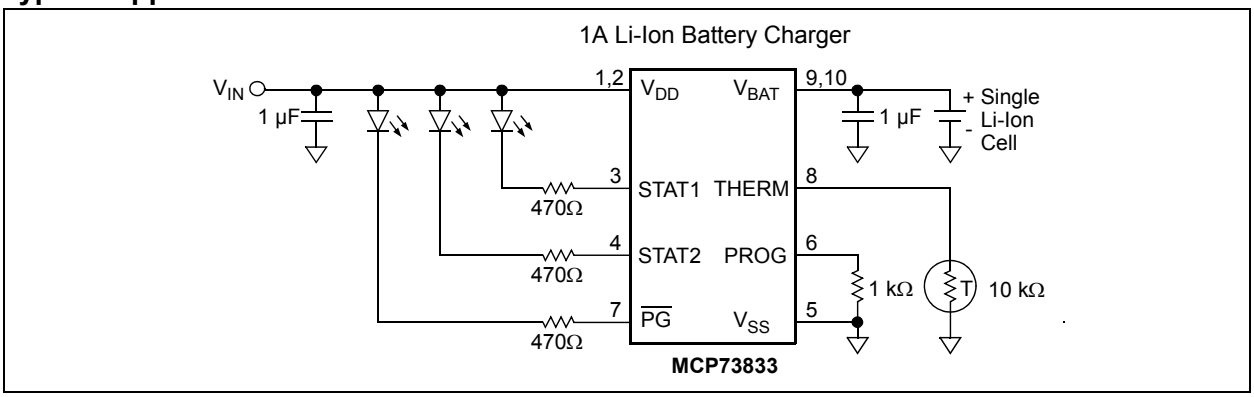
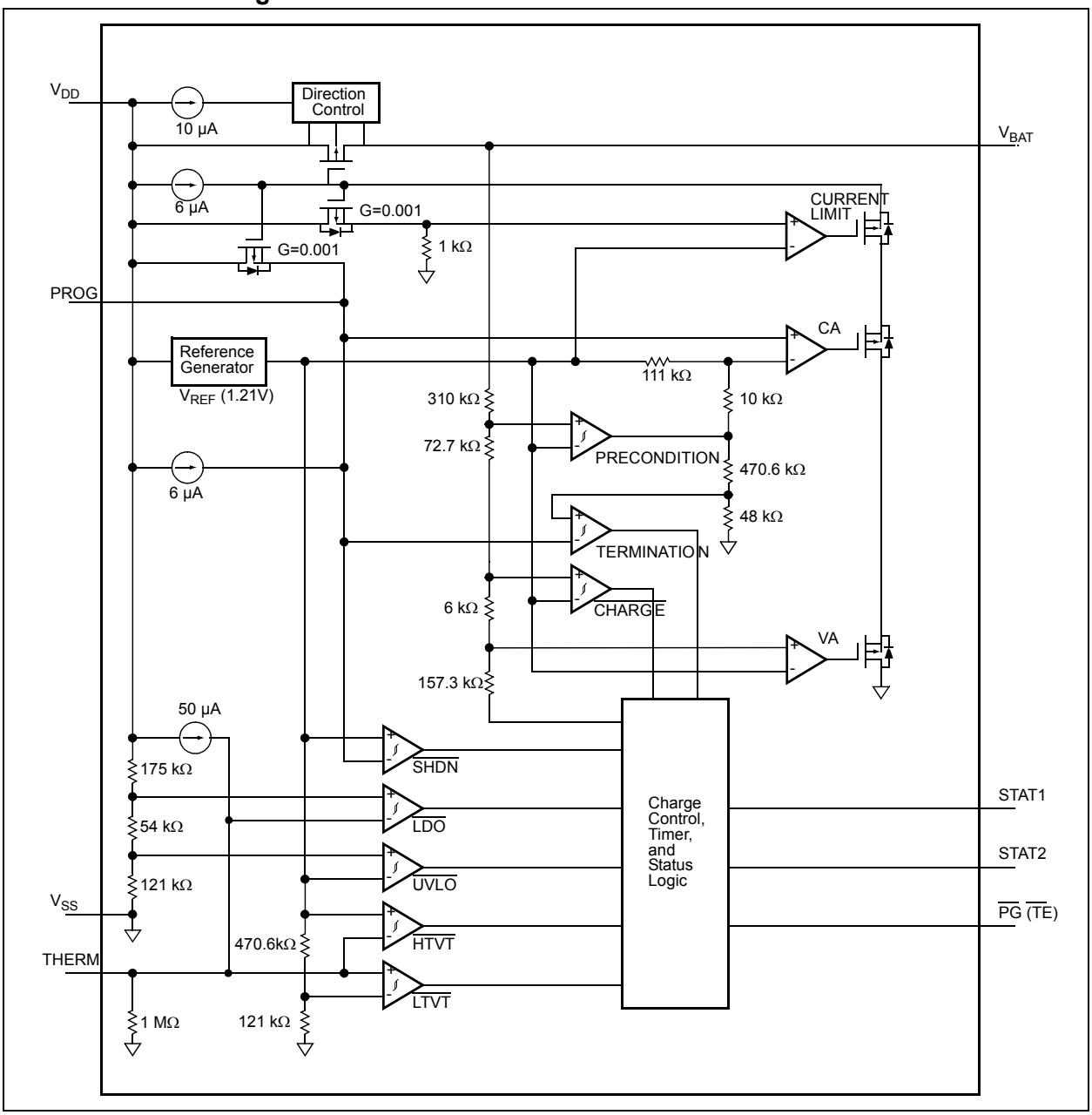
Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{DD}.....7.0V

All Inputs and Outputs w.r.t. V_{SS} .....-0.3 to (V_{DD}+0.3)V

Maximum Junction Temperature, T_J . Internally Limited

Storage temperature .....-65°C to +150°C

ESD protection on all pins:

Human Body Model (HBM)
(1.5 kΩ in Series with 100 pF)..... ≥ 4 kV

Machine Model (MM)
(200 pF, No Series Resistance) 300V

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Input						
Supply Voltage	V_{DD}	3.75	—	6	V	Charging
		V_{REG}(Typical)+0.3V	—	6	V	Charge Complete, Standby
Supply Current	I_{SS}	—	2000	3000	µA	Charging
		—	150	300	µA	Charge Complete
		—	100	300	µA	Standby (No Battery or PROG Floating)
		—	50	100	µA	Shutdown ($V_{DD} \le V_{BAT}$, or $V_{DD} < V_{STOP}$)
UVLO Start Threshold	V_{START}	3.4	3.55	3.7	V	V_{DD} Low-to-High
UVLO Stop Threshold	V_{STOP}	3.3	3.45	3.6	V	V_{DD} High-to-Low
UVLO Hysteresis	V_{HYS}	—	100	—	mV	
Voltage Regulation (Constant Voltage Mode, System Test Mode)						
Regulated Output Voltage	V_{REG}	4.168	4.20	4.232	V	V_{DD}=[V_{REG}(Typical)+1V]
		4.318	4.35	4.382	V	I_{OUT}=10 mA
		4.367	4.40	4.433	V	T_A=-5°C to +55°C
		4.467	4.50	4.533	V	
Line Regulation	$\lvert(\Delta V_{BAT}/V_{BAT})/\Delta V_{DD}\rvert$	—	0.10	0.30	%/V	V_{DD}=[V_{REG}(Typical)+1V] to 6V, I_{OUT}=10 mA
Load Regulation	$\lvert\Delta V_{BAT}/ V_{BAT}\rvert$	—	0.10	0.30	%	I_{OUT}=10 mA to 100 mA V_{DD}=[V_{REG}(Typical)+1V]
Supply Ripple Attenuation	PSRR	—	58	—	dB	I_{OUT}=10 mA, 10Hz to 1 kHz
		—	47	—	dB	I_{OUT}=10 mA, 10Hz to 10 kHz
		—	25	—	dB	I_{OUT}=10 mA, 10Hz to 1 MHz
Current Regulation (Fast Charge Constant Current Mode)						
Fast Charge Current Regulation	I_{REG}	90	100	110	mA	PROG = 10 kΩ
		900	1000	1100	mA	PROG = 1.0 kΩ
						T_A=-5°C to +55°C
Maximum Output Current Limit	I_{MAX}	—	1200	—	mA	PROG < 833Ω

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
Preconditioning Current Regulation (Trickle Charge Constant Current Mode)						
Precondition Current Ratio	I_{PREG} / I_{REG}	7.5	10	12.5	%	PROG = 1.0 kΩ to 10 kΩ
		15	20	25	%	T_A=-5°C to +55°C
		30	40	50	%	
		—	100	—	%	
Precondition Voltage Threshold Ratio	V_{PTH} / V_{REG}	64	66.5	70	%	V_{BAT} Low-to-High
		69	71.5	75	%	
Precondition Hysteresis	V_{PHYS}	—	100	—	mV	V_{BAT} High-to-Low
Charge Termination						
Charge Termination Current Ratio	I_{TERM} / I_{REG}	3.75	5	6.25	%	PROG = 1.0 kΩ to 10 kΩ
		5.6	7.5	9.4	%	T_A=-5°C to +55°C
		7.5	10	12.5	%	
		15	20	25	%	
Automatic Recharge						
Recharge Voltage Threshold Ratio	V_{RTH} / V_{REG}	—	94.0	—	%	V_{BAT} High-to-Low
		—	96.5	—	%	
Pass Transistor ON-Resistance						
ON-Resistance	R_{DSON}	—	300	—	mΩ	V_{DD} = 3.75V T_J = 105°C
Battery Discharge Current						
Output Reverse Leakage Current	$I_{DISCHARGE}$	—	0.15	2	µA	PROG Floating
		—	0.25	2	µA	$V_{DD} \leq V_{BAT}$
		—	0.15	2	µA	$V_{DD} < V_{STOP}$
		—	-5.5	-15	µA	Charge Complete
Status Indicators - STAT1, STAT2, $\overline{PG}$						
Sink Current	I_{SINK}	—	15	25	mA	
Low Output Voltage	V_{OL}	—	0.4	1	V	I_{SINK} = 4 mA
Input Leakage Current	I_{LK}	—	0.01	1	µA	High Impedance, 6V on pin
PROG Input						
Charge Impedance Range	R_{PROG}	1	—	20	kΩ	
Standy Impedance	R_{PROG}	70	—	200	kΩ	Minimum Impedance for Standby
Thermistor Bias						
Thermistor Current Source	I_{THERM}	47	50	53	µA	2 kΩ < R_{THERM} < 50 kΩ
Thermistor Comparator						
Upper Trip Threshold	V_{T1}	1.20	1.23	1.26	V	V_{THERM} Low-to-High
Upper Trip Point Hysteresis	V_{T1HYS}	—	-50	—	mV	
Lower Trip Threshold	V_{T2}	0.235	0.25	0.265	V	V_{THERM} High-to-Low
Lower Trip Point Hysteresis	V_{T2HYS}	—	50	—	mV	
System Test (LDO) Mode						
Input High Voltage Level	V_{IH}	(V_{DD}-0.1)	—	—	V	
THERM Input Sink Current	I_{SINK}	3	6	20	µA	Stand-by or system test mode
Bypass Capacitance	C_{BAT}	1	—	—	µF	I_{OUT} < 250 mA
		4.7	—	—	µF	I_{OUT} > 250 mA

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
Automatic Power Down						
Automatic Power Down Entry Threshold	V_{PD}	—	V_{BAT} + 50 mV	—	V	2.3V ≤ V_{BAT} ≤ V_{REG} V_{DD} Falling
Automatic Power Down Exit Threshold	V_{PDEXIT}	—	V_{BAT} + 150 mV	—	V	2.3V ≤ V_{BAT} ≤ V_{REG} V_{DD} Rising
Timer Enable Input ($\overline{TE}$)						
Input High Voltage Level	V_{IH}	2.0	—	—	V	
Input Low Voltage Level	V_{IL}	—	—	0.6	V	
Input Leakage Current	I_{LK}	—	0.01	1	µA	V_{TE} = 6V
Thermal Shutdown						
Die Temperature	T_{SD}	—	150	—	°C	
Die Temperature Hysteresis	T_{SDHYS}	—	10	—	°C	

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V, T_A=-40°C to 85°C. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Sym	Min	Typ	Max	Units	Conditions
UVLO Start Delay	t_{START}	—	—	5	ms	V_{DD} Low-to-High
Current Regulation						
Transition Time Out of Preconditioning	t_{DELAY}	—	—	1	ms	V_{BAT}<V_{PTH} to V_{BAT}>V_{PTH}
Current Rise Time Out of Preconditioning	t_{RISE}	—	—	1	ms	I_{OUT} Rising to 90% of I_{REG}
Preconditioning Comparator Filter Time	t_{PRECON}	0.4	1.3	3.2	ms	Average V_{BAT} Rise/Fall
Termination Comparator Filter Time	t_{TERM}	0.4	1.3	3.2	ms	Average I_{OUT} Falling
$\overline{Charge}$ Comparator Filter Time	t_{CHARGE}	0.4	1.3	3.2	ms	Average V_{BAT} Falling
Thermistor Comparator Filter Time	t_{THERM}	0.4	1.3	3.2	ms	Average THERM Rise/Fall
Elapsed Timer						
Elapsed Timer Period	$t_{ELAPSED}$	0	0	0	Hours	Timer Disabled
		3.6	4.0	4.4	Hours	
		5.4	6.0	6.6	Hours	
		7.2	8.0	8.8	Hours	
Status Indicators						
Status Output turn-off	t_{OFF}	—	—	200	µs	I_{SINK} = 1 mA to 0 mA
Status Output turn-on	t_{ON}	—	—	200	µs	I_{SINK} = 0 mA to 1 mA

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all limits apply for V_{DD}= [V_{REG}(Typical)+0.3V] to 6V. Typical values are at +25°C, V_{DD}= [V_{REG}(Typical)+1.0V]

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, MSOP-10	θ_{JA}	—	113	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection
Thermal Resistance, DFN-10, 3 mm x 3 mm	θ_{JA}	—	41	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 5.2V, V_{REG} = 4.20V, I_{OUT} = 10 mA and T_A= +25°C, Constant-voltage mode.

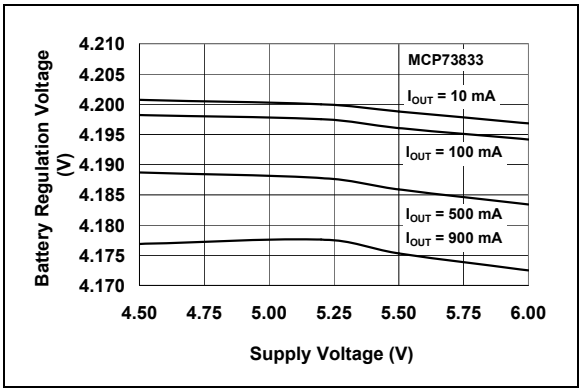


FIGURE 2-1: *Battery Regulation Voltage (V_{BAT}) vs. Supply Voltage (V_{DD}).*

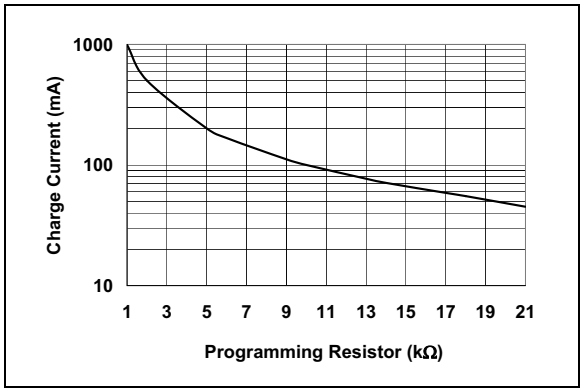


FIGURE 2-4: *Charge Current (I_{OUT}) vs. Programming Resistor (R_{PROG}).*

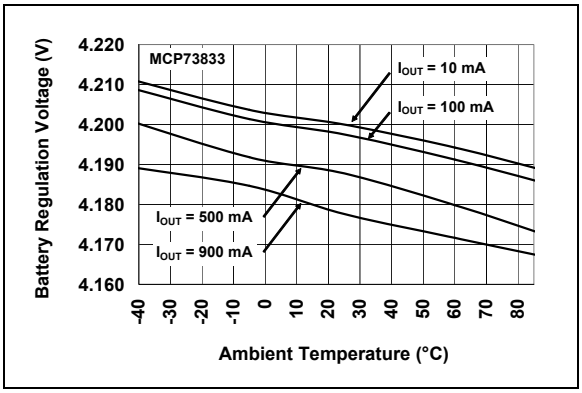


FIGURE 2-2: *Battery Regulation Voltage (V_{BAT}) vs. Ambient Temperature (T_A).*

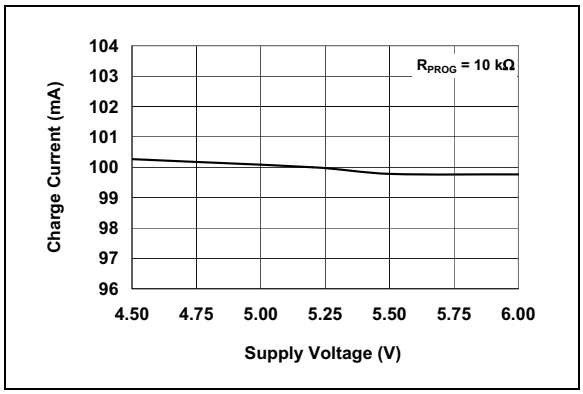


FIGURE 2-5: *Charge Current (I_{OUT}) vs. Supply Voltage (V_{DD}).*

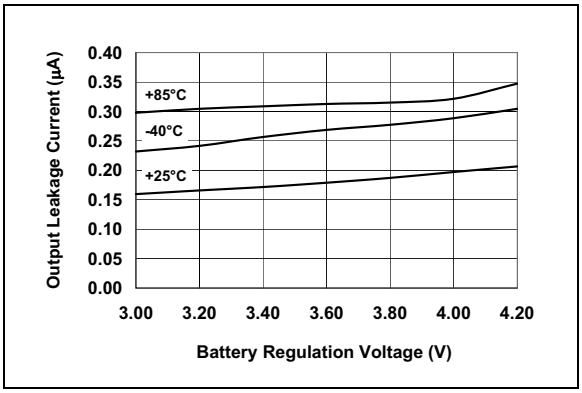


FIGURE 2-3: *Output Leakage Current ($I_{DISCHARGE}$) vs. Battery Regulation Voltage (V_{BAT}).*

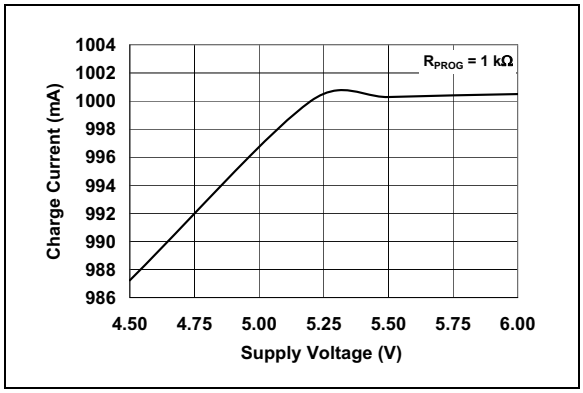


FIGURE 2-6: *Charge Current (I_{OUT}) vs. Supply Voltage (V_{DD}).*

TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, V_{DD} = 5.2V, V_{REG} = 4.20V, I_{OUT} = 10 mA and T_A= +25°C, Constant-voltage mode.

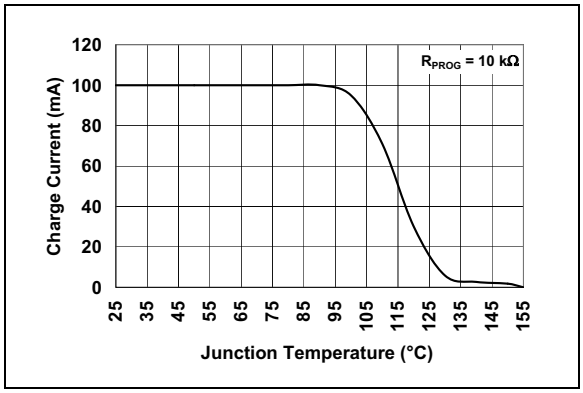


FIGURE 2-7: *Charge Current (I_{OUT}) vs. Junction Temperature (T_J).*

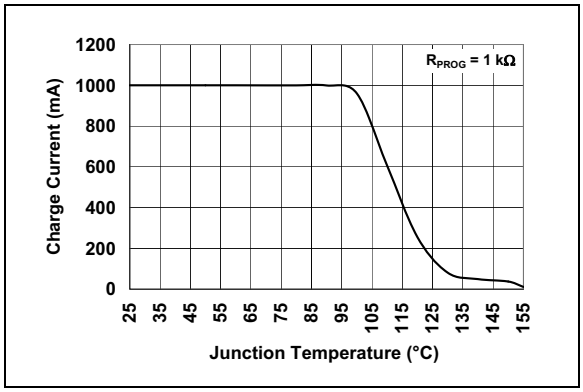


FIGURE 2-8: *Charge Current (I_{OUT}) vs. Junction Temperature (T_J).*

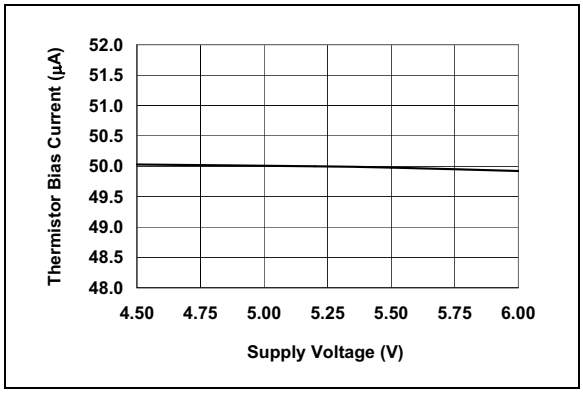


FIGURE 2-9: *Thermistor Bias Current (I_{THRERM}) vs. Supply Voltage (V_{DD}).*

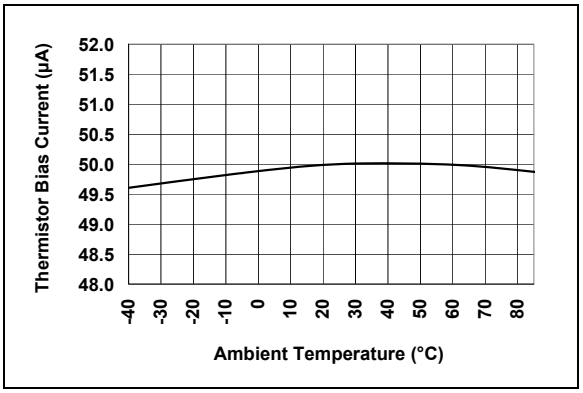


FIGURE 2-10: *Thermistor Bias Current (I_{THRERM}) vs. Ambient Temperature (T_A).*

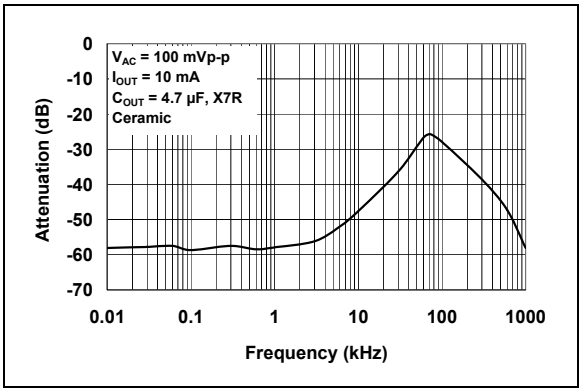


FIGURE 2-11: *Power Supply Ripple Rejection (PSRR).*

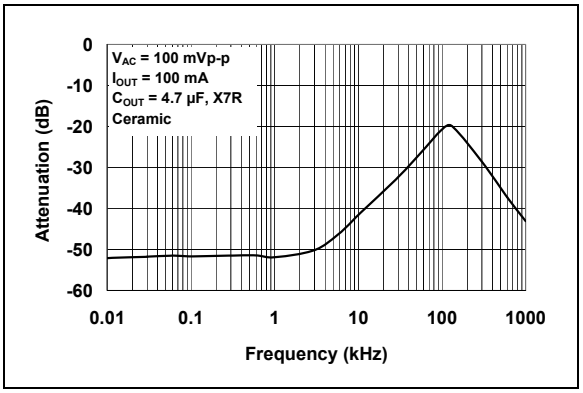


FIGURE 2-12: *Power Supply Ripple Rejection (PSRR).*

TYPICAL PERFORMANCE CURVES (Continued)

Note: Unless otherwise indicated, V_{DD} = 5.2V, V_{REG} = 4.20V, I_{OUT} = 10 mA and T_A= +25°C, Constant-voltage mode.

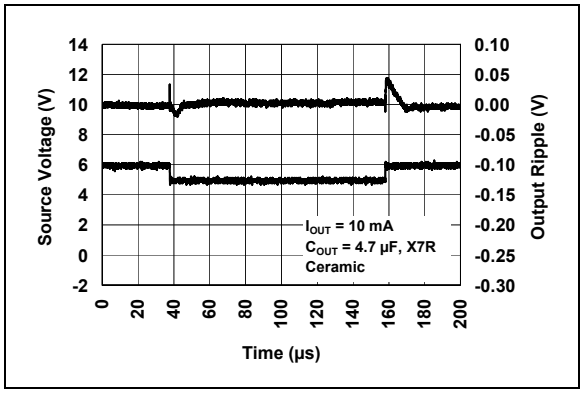


FIGURE 2-13: *Line Transient Response.*

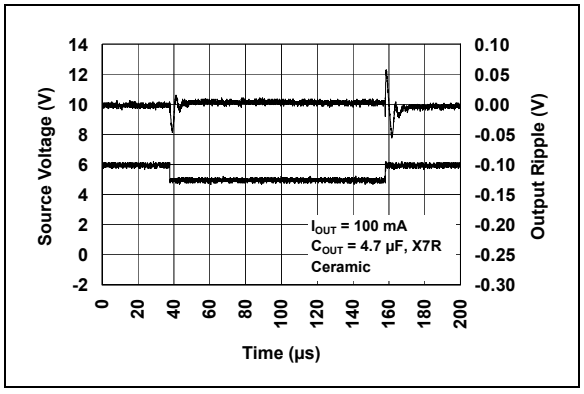


FIGURE 2-14: *Line Transient Response.*

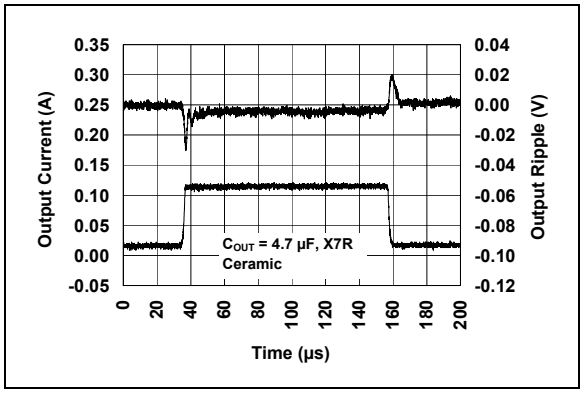


FIGURE 2-15: *Load Transient Response.*

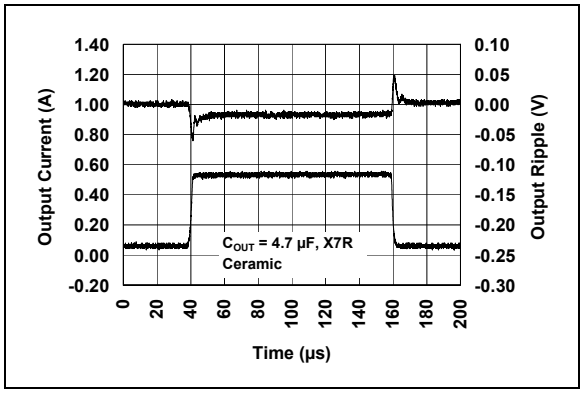


FIGURE 2-16: *Load Transient Response.*

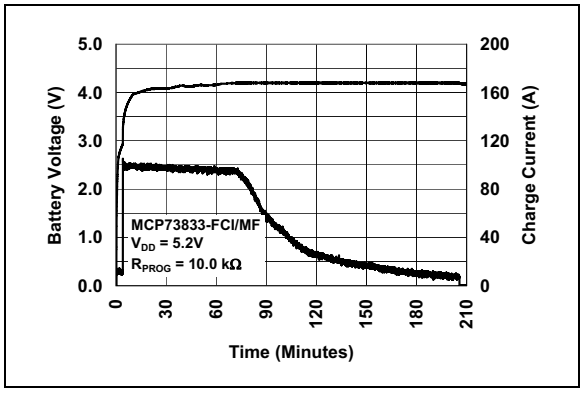


FIGURE 2-17: *Complete Charge Cycle (180 mA Li-Ion Battery).*

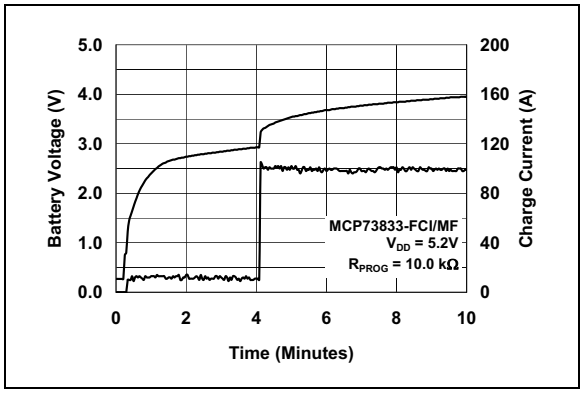


FIGURE 2-18: *Charge Cycle Start - Preconditioning (180 mAh Li-Ion Battery).*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.		Symbol	Function
DFN-10	MSOP-10		
1	1	V_{DD}	Battery Management Input Supply
2	2	V_{DD}	Battery Management Input Supply
3	3	STAT1	Charge Status Output
4	4	STAT2	Charge Status Output
5	5	V_{SS}	Battery Management 0V Reference
6	6	PROG	Current Regulation Set and Charge Control Enable
7	7	$\overline{PG}$, $\overline{TE}$	**MCP73833:** Power Good output, **MCP73834**: Timer Enable input
8	8	THERM	Thermistor input
9	9	V_{BAT}	Battery Charge Control Output
10	10	V_{BAT}	Battery Charge Control Output
11	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

3.1 Battery Management Input Supply (V_{DD})

A supply voltage of [V_{REG} (typical) + 0.3V] to 6V is recommended. Bypass to V_{SS} with a minimum of 1 µF.

3.2 Charge Status Outputs (STAT1, STAT2)

STAT1 and STAT2 are open-drain logic outputs for connection to a LED for charge status indication. Alternatively, a pull-up resistor can be applied for interfacing to a host microcontroller.

3.3 Battery Management 0V Reference (V_{SS})

Connect to negative terminal of battery and input supply.

3.4 Current Regulation Set (PROG)

Preconditioning, fast charge, and termination currents are scaled by placing a resistor from PROG to V_{SS}.

The charge management controller can be disabled by allowing the PROG input to float.

3.5 Power Good Indication ($\overline{PG}$) MCP73833 Only

The power good ($\overline{PG}$) option is a pseudo open-drain output. The $\overline{PG}$ output can sink current, but not source current. However, there is a diode path back to the input, and, as such, the $\overline{PG}$ output should only be pulled up to the input. The $\overline{PG}$ output is low whenever the input to the MCP73833 is above the UVLO threshold and greater than the battery voltage.

3.6 Timer Enable Input ($\overline{TE}$) MCP73834 Only

The timer enable ($\overline{TE}$) input option is used to enable or disable the internal timer. A low signal on this pin enables the internal timer and a high signal disables the internal timer. The $\overline{TE}$ input can be used to disable the timer when the charger is supplying current to charge the battery and power the system load. The $\overline{TE}$ input is compatible with 1.8V logic.

3.7 Thermistor Input (THERM)

An internal 50 µA current source provides the bias for most common 10 kΩ negative-temperature coefficient thermistors (NTC). The MCP73833/4 compares the voltage at the THERM pin to factory set thersholds of 1.20V and 0.25V, typically.

3.8 Battery Charge Control Output (V_{BAT})

Connect to positive terminal of battery. Drain terminal of internal P-channel MOSFET pass transistor. Bypass to V_{SS} with a minimum of 1 µF to ensure loop stability when the battery is disconnected.

3.9 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential.

NOTES:

4.0 FUNCTIONAL DESCRIPTION

The MCP73833/4 is a highly advanced linear charge management controller. Refer to the functional block diagram and Figure 4-1 that depicts the operational flow algorithm from charge initiation to completion and automatic recharge.

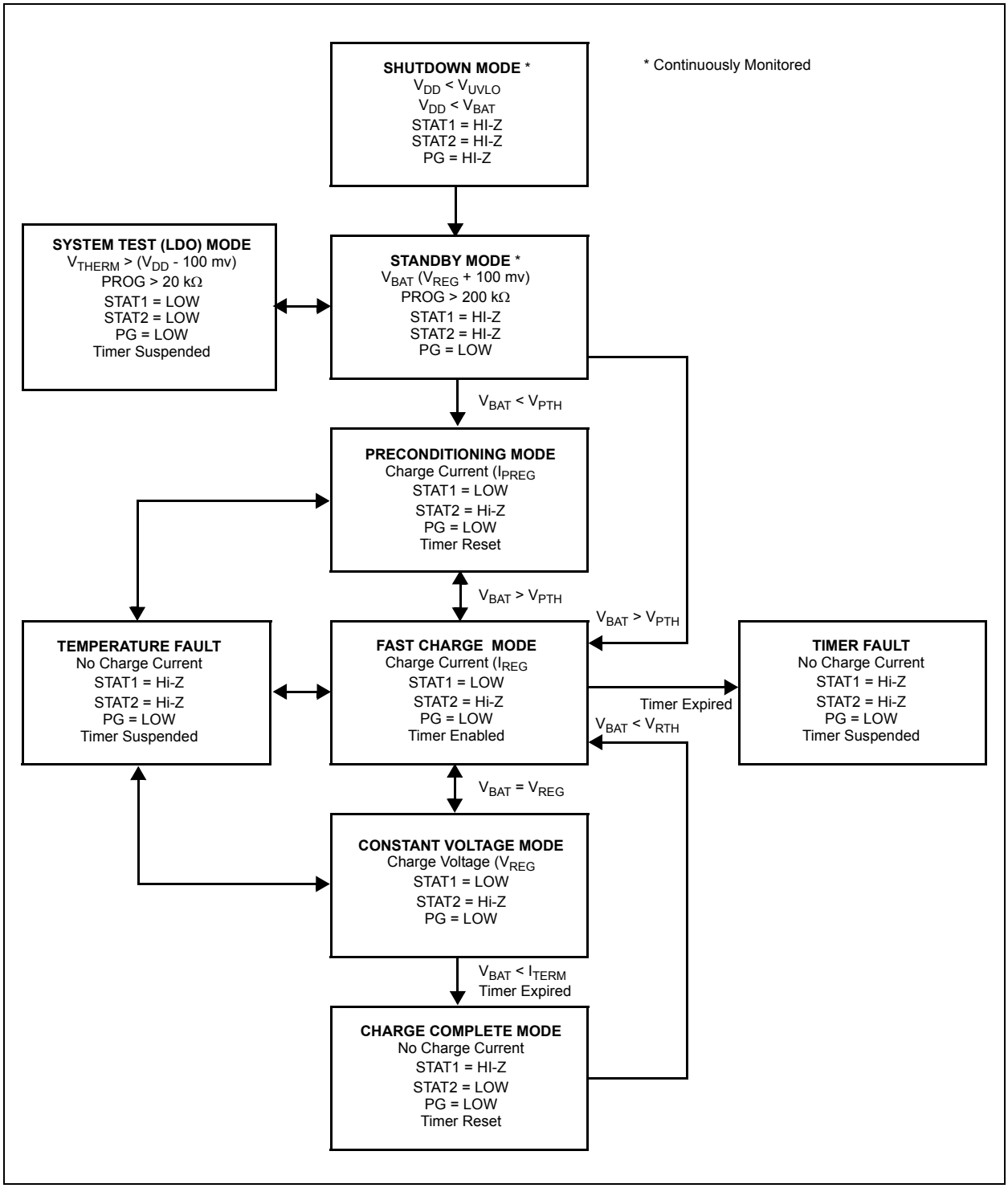


FIGURE 4-1: *Flow Chart.*

4.1 Under Voltage Lockout (UVLO)

An internal under voltage lockout (UVLO) circuit monitors the input voltage and keeps the charger in shutdown mode until the input supply rises above the UVLO threshold. The UVLO circuitry has a built-in hysteresis of 100 mV.

In the event a battery is present when the input power is applied, the input supply must rise +150 mV above the battery voltage before the MCP73833/4 becomes operational.

The UVLO circuit places the device in shutdown mode if the input supply falls to within +50 mV of the battery voltage.

The UVLO circuit is always active. At any time the input supply is below the UVLO threshold or within +50 mV of the voltage at the V_{BAT} pin, the MCP73833/4 is placed in a shutdown mode.

During any UVLO condition, the battery reverse discharge current shall be less than 2 µA.

4.2 Charge Qualification

For a charge cycle to begin, all UVLO conditions must be met and a battery or output load must be present.

A charge current programming resistor must be connected from PROG to V_{SS}. If the PROG pin is open or floating, the MCP73833/4 is disabled and the battery reverse discharge current is less than 2 µA. In this manner, the PROG pin acts as a charge enable and can be used as a manual shutdown.

If the input supply voltage is above the UVLO threshold, but below V_{REG}(Typical)+0.3V, the MCP73833/4 will pulse the STAT1 and PG outputs as the device determines if a battery is present.

4.3 Preconditioning

If the voltage at the V_{BAT} pin is less than the preconditioning threshold, the MCP73833/4 enters a preconditioning or trickle charge mode. The preconditioning threshold is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for preconditioning threshold options.

In this mode, the MCP73833/4 supplies a percentage of the charge current (established with the value of the resistor connected to the PROG pin) to the battery. The percentage or ratio of the current is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for preconditioning current options.

When the voltage at the V_{BAT} pin rises above the pre-conditioning threshold, the MCP73833/4 enters the constant current or fast charge mode.

4.4 Constant Current - Fast Charge Mode

During the constant current mode, the programmed charge current is supplied to the battery or load. The charge current is established using a single resistor from PROG to V_{SS}. The program resistor and the charge current are calculated using Equation 4-1:

EQUATION 4-1:

Where:

$$I_{REG} = \frac{1000V}{R_{PROG}}$$

R_{PROG} = kilo-ohms

I_{REG} = milliampere

Constant current mode is maintained until the voltage at the V_{BAT} pin reaches the regulation voltage, V_{REG}.

When constant current mode is invoked, the internal timer is reset.

4.4.1 TIMER EXPIRED DURING CONSTANT CURRENT - FAST CHARGE MODE

If the internal timer expires before the recharge voltage threshold is reached, a timer fault is indicated and the charge cycle terminates. The MCP73833/4 remains in this condition until the battery is removed, the input power is removed, or the PROG pin is opened. If the battery is removed or the PROG pin is opened, the MCP73833/4 enters the Standby mode where it remains until a battery is reinserted or the PROG pin is reconnected. If the input power is removed, the MCP73833/4 is in Shutdown. When the input power is reapplied, a normal start-up sequence ensues.

4.5 Constant Voltage Mode

When the voltage at the V_{BAT} pin reaches the regulation voltage, V_{REG}, constant voltage regulation begins. The regulation voltage is factory set to 4.20V, 4.35V, 4.40V, or 4.50V with a tolerance of ± 0.75%.

4.6 Charge Termination

The charge cycle is terminated when, during constant voltage mode, the average charge current diminishes below a percentage of the programmed charge current (established with the value of the resistor connected to the PROG pin) or the internal timer has expired. A 1 ms filter time on the termination comparator ensures that transient load conditions do not result in premature charge cycle termination. The percentage or ratio of the current is factory set. The timer period is factory set and can be disabled. Refer to **Section 1.0 "Electrical Characteristics"** for charge termination current ratio and timer period options.

The charge current is latched off and the MCP73833/4 enters a charge complete mode.

4.7 Automatic Recharge

The MCP73833/4 continuously monitors the voltage at the V_{BAT} pin in the charge complete mode. If the voltage drops below the recharge threshold, another charge cycle begins and current is once again supplied to the battery or load. The recharge threshold is factory set. Refer to **Section 1.0 "Electrical Characteristics"** for recharge threshold options.

4.8 Thermal Regulation

The MCP73833/4 limits the charge current based on the die temperature. The thermal regulation optimizes the charge cycle time while maintaining device reliability. Figure 4-2 depicts the thermal regulation for the MCP73833/4.

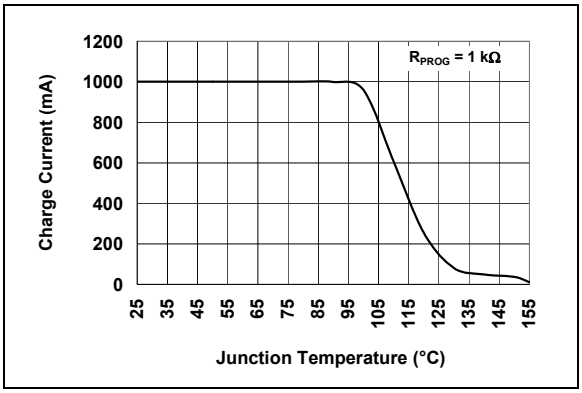


FIGURE 4-2: *Thermal Regulation.*

4.9 Thermal Shutdown

The MCP73833/4 suspends charge if the die temperature exceeds +150°C. Charging will resume when the die temperature has cooled by approximately +10°C. The thermal shutdown is a secondary safety feature in the event that there is a failure within the thermal regulation circuitry.

NOTES:

5.0 DETAILED DESCRIPTION

5.1 Analog Circuitry

5.1.1 BATTERY MANAGEMENT INPUT SUPPLY (V_{DD})

The V_{DD} input is the input supply to the MCP73833/4. The MCP73833/4 automatically enters a Power-down mode if the voltage on the V_{DD} input falls below the UVLO voltage (V_{STOP}). This feature prevents draining the battery pack when the V_{DD} supply is not present.

5.1.2 CURRENT REGULATION SET (PROG)

Fast charge current regulation can be scaled by placing a programming resistor (R_{PROG}) from the PROG input to V_{SS}. The program resistor and the charge current are calculated using the Equation 5-1:

EQUATION 5-1:

$$I_{REG} = \frac{1000V}{R_{PROG}}$$

Where:

R_{PROG} = kilo-ohms

I_{REG} = milliampere

The preconditioning trickle-charge current and the charge termination current are ratiometric to the fast charge current based on the selected device options.

5.1.3 BATTERY CHARGE CONTROL OUTPUT (V_{BAT})

The battery charge control output is the drain terminal of an internal P-channel MOSFET. The MCP73833/4 provides constant current and voltage regulation to the battery pack by controlling this MOSFET in the linear region. The battery charge control output should be connected to the positive terminal of the battery pack.

5.1.4 TEMPERATURE QUALIFICATION (THERM)

The MCP73833/4 continuously monitors battery temperature during a charge cycle by measuring the voltage between the THERM and V_{SS} pins. An internal 50 µA current source provides the bias for most common 10 kΩ negative-temperature coefficient (NTC) or positive-temperature coefficient (PTC) thermistors.The current source is controlled, avoiding measurement sensitivity to fluctuations in the supply voltage (V_{DD}). The MCP73833/4 compares the voltage at the THERM pin to factory set thersholds of 1.20V and 0.25V, typically. Once a volage outside the thresholds is detected during a charge cycle, the MCP73833/4 immediately suspends the charge cycle. The MCP73833/4 suspends charge by turning off the pass transistor and holding the timer value. The charge cycle resumes when the voltage at the THERM pin returns to the normal range.

If temperature monitoring is not required, place a standard 10 kΩ resistor from THERM to V_{SS}.

5.1.4.1 System Test (LDO) Mode

The MCP73833/4 can be placed in a system test mode. In this mode, the MCP73833/4 operates as a low dropout linear regulator (LDO). The output voltage is regulated to the factory set voltage regulation option. The available output current is limitted to the programmed fast charge current. For stability, the V_{BAT} output must be bypassed to V_{SS} with a minimum capacitance of 1 µF for output currents up to 250 mA. A minimum capacitance of 4.7 µF is required for output currents above 250 mA.

The system test mode is entered by driving the THERM input greater than (V_{DD}-100 mV) with no battery connected to the output. In this mode, the MCP73833/4 can be used to power the system without a battery present.

Note 1: I_{THERM} is disabled during shutdown, stand-by, and system test modes.

2: A pull-down current source on the THERM input is active only in stand-by and system test modes.

3: During system test mode, the PROG input sets the available output current limit.

4: System test mode shall be exited by releasing the THERM input or cycling input power.

5.2 Digital Circuitry

5.2.1 STATUS INDICATORS AND POWER GOOD ($\overline{PG}$ - OPTION)

The charge status outputs have two different states: Low (L), and High Impedance (Hi-Z). The charge status outputs can be used to illuminate LEDs. Optionally, the charge status outputs can be used as an interface to a host microcontroller. Table 5-1 summarize the state of the status outputs during a charge cycle.

TABLE 5-1: STATUS OUTPUTS

Charge Cycle State	STAT1	STAT2	PG
Shutdown	Hi-Z	Hi-Z	Hi-Z
Standby	Hi-Z	Hi-Z	L
Charge in Progress	L	Hi-Z	L
Charge Complete (EOC)	Hi-Z	L	L
Temperature Fault	Hi-Z	Hi-Z	L
Timer Fault	Hi-Z	Hi-Z	L
System Test Mode	L	L	L

5.2.2 POWER GOOD ($\overline{PG}$) OPTION

The power good ($\overline{PG}$) option is a pseudo open-drain output. The $\overline{PG}$ output can sink current, but not source current. However, there is a diode path back to the input, and as such, the $\overline{PG}$ output should only be pulled up to the input. The $\overline{PG}$ output is low whenever the input to the MCP73833 is above the UVLO threshold and greater than the battery voltage. If the supply voltage is above the UVLO, but below V_{REG}(Typical)+0.3V, the MCP73833 will pulse the PG output as the device determines if a battery is present.

5.2.3 TIMER ENABLE ($\overline{TE}$) OPTION

The timer enable ($\overline{TE}$) input option is used to enable or disable the internal timer. A low signal on this pin enables the internal timer and a high signal disables the internal timer. The $\overline{TE}$ input can be used to disable the timer when the charger is supplying current to charge the battery and power the system load. The $\overline{TE}$ input is compatible with 1.8V logic.

5.2.4 DEVICE DISABLE (PROG)

The current regulation set input pin (PROG) can be used to terminate a charge at any time during the charge cycle, as well as to initiate a charge cycle or initiate a recharge cycle.

Placing a programming resistor from the PROG input to V_{SS} enables the device. Allowing the PROG input to float or by applying a logic-high input signal, disables the device and terminates a charge cycle. When disabled, the device's supply current is reduced to 100 µA, typically.

6.0 APPLICATIONS

The MCP73833/4 is designed to operate in conjunction with a host microcontroller or in stand-alone applications. The MCP73833/4 provides the preferred charge algorithm for Lithium-Ion and Lithium-Polymer cells Constant-current followed by Constant-voltage. Figure 6-1 depicts a typical stand-alone application circuit, while Figures 6-2 and 6-3 depict the accompanying charge profile.

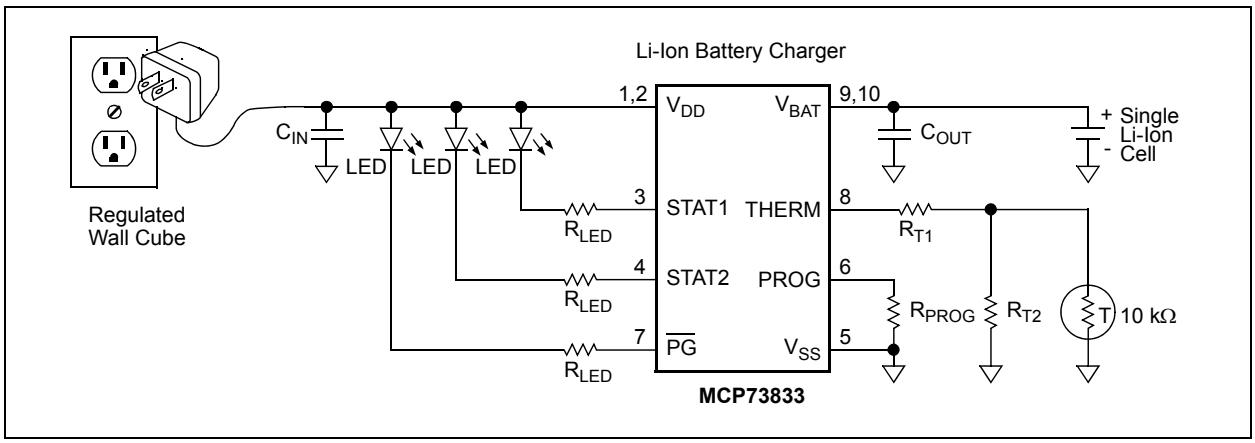


FIGURE 6-1: *Typical Application Circuit.*

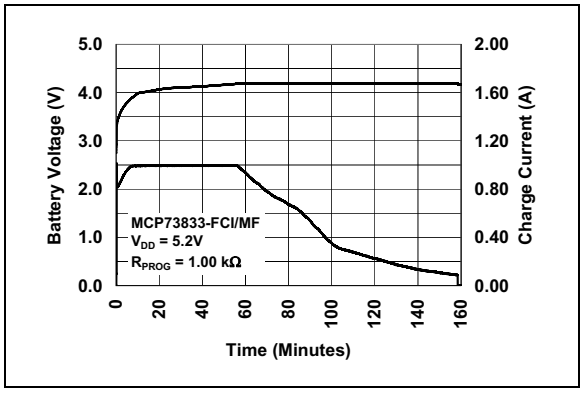


FIGURE 6-2: *Typical Charge Profile with Thermal Regulation (1700 mAh Li-Ion Battery).*

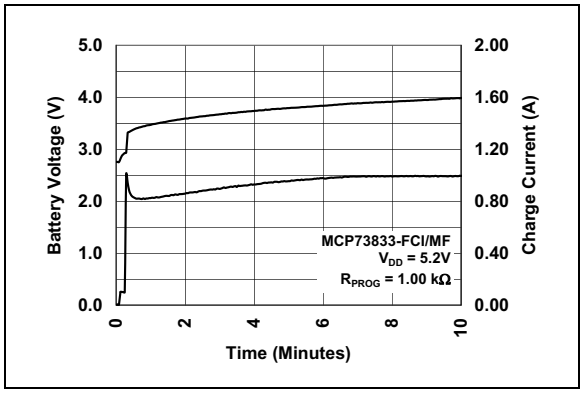


FIGURE 6-3: *Typical Charge Cycle Start with Thermal Regulation (1700 mAh Li-Ion Battery).*

6.1 Application Circuit Design

Due to the low efficiency of linear charging, the most important factors are thermal design and cost, which are a direct function of the input voltage, output current and thermal impedance between the battery charger and the ambient cooling air. The worst-case scenario is when the device has transitioned from the Preconditioning mode to the Constant-current mode. In this situation, the battery charger has to dissipate the maximum power. A trade-off must be made between the charge current, cost and thermal requirements of the charger.

6.1.1 COMPONENT SELECTION

Selection of the external components in Figure 6-1 is crucial to the integrity and reliability of the charging system. The following discussion is intended as a guide for the component selection process.

6.1.1.1 Current Programming Resistor (R_{PROG})

The preferred fast charge current for Lithium-Ion cells is at the 1C rate, with an absolute maximum current at the 2C rate. For example, a 500 mAh battery pack has a preferred fast charge current of 500 mA. Charging at this rate provides the shortest charge cycle times without degradation to the battery pack performance or life.

6.1.1.2 Thermal Considerations

The worst-case power dissipation in the battery charger occurs when the input voltage is at the maximum and the device has transitioned from the Preconditioning mode to the Constant-current mode. In this case, the power dissipation is:

$$PowerDissipation = (V_{DDMAX} - V_{PTHMIN}) \times I_{REGMAX}$$

Where:

V_{DDMAX}	=	the maximum input voltage
I_{REGMAX}	=	the maximum fast charge current
V_{PTHMIN}	=	the minimum transition threshold voltage

Power dissipation with a 5V, ±10% input voltage source is:

$$PowerDissipation = (5.5V - 2.7V) \times 550mA = 1.54W$$

This power dissipation with the battery charger in the MSOP-10 package will cause thermal regulation to be entered as depicted in Figure 6-3. Alternatively, the DFN-10 (3 mm x 3 mm) package could be utilized to reduce charge cycle times.

6.1.1.3 External Capacitors

The MCP73833/4 is stable with or without a battery load. In order to maintain good AC stability in the Constant-voltage mode, a minimum capacitance of 4.7 µF is recommended to bypass the V_{BAT} pin to V_{SS}. This capacitance provides compensation when there is no battery load. In addition, the battery and interconnections appear inductive at high frequencies. These elements are in the control feedback loop during Constant-voltage mode. Therefore, the bypass capacitance may be necessary to compensate for the inductive nature of the battery pack.

Virtually any good quality output filter capacitor can be used, independent of the capacitor's minimum Effective Series Resistance (ESR) value. The actual value of the capacitor (and its associated ESR) depends on the output load current. A 4.7 µF ceramic, tantalum or aluminum electrolytic capacitor at the output is usually sufficient to ensure stability for output currents up to a 500 mA.

6.1.1.4 Reverse-Blocking Protection

The MCP73833/4 provides protection from a faulted or shorted input. Without the protection, a faulted or shorted input would discharge the battery pack through the body diode of the internal pass transistor.

6.1.1.5 Charge Inhibit

The current regulation set input pin (PROG) can be used to terminate a charge at any time during the charge cycle, as well as to initiate a charge cycle or initiate a recharge cycle.

Placing a programming resistor from the PROG input to V_{SS} enables the device. Allowing the PROG input to float or by applying a logic-high input signal, disables the device and terminates a charge cycle. When disabled, the device's supply current is reduced to 100 µA, typically.

6.1.1.6 Temperature Monitoring

The charge temperature window can be set by placing fixed value resistors in series-parallel with a thermistor. The resistance values of R_{T1} and R_{T2} can be calculated with the following equations in order to set the temperature window of interest.

For NTC thermistors:

$$24k\Omega = R_{T1} + \frac{R_{T2} \times R_{COLD}}{R_{T2} + R_{COLD}}$$

$$5k\Omega = R_{T1} + \frac{R_{T2} \times R_{HOT}}{R_{T2} + R_{HOT}}$$

Where:

R_{T1}	=	the fixed series resistance
R_{T2}	=	the fixed parallel resistance
R_{COLD}	=	the thermistor resistance at the lower temperature of interest
R_{HOT}	=	the thermistor resistance at the upper temperature of interest

For example, by utilizing a 10 kΩ at 25C NTC thermistor with a sensitivity index, β, of 3892, the charge temperature range can be set to 0C - 50C by placing a 1.54 kΩ resistor in series (R_{T1}), and a 69.8 kΩ resistor in parallel (R_{T2}) with the thermistor as depicted in Figure 6-1.

6.1.1.7 Charge Status Interface

A status output provides information on the state of charge. The output can be used to illuminate external LEDs or interface to a host microcontroller. Refer to Table 5-1 for a summary of the state of the status output during a charge cycle.

6.2 PCB Layout Issues

For optimum voltage regulation, place the battery pack as close as possible to the device's V_{BAT} and V_{SS} pins, recommended to minimize voltage drops along the high current-carrying PCB traces.

If the PCB layout is used as a heatsink, adding many vias in the heatsink pad can help conduct more heat to the backplane of the PCB, thus reducing the maximum junction temperature. Figures 6-4 and 6-5 depict a typical layout with PCB heatsinking.

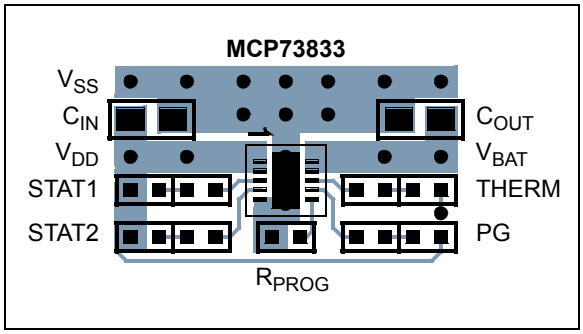


FIGURE 6-4: *Typical Layout (Top).*

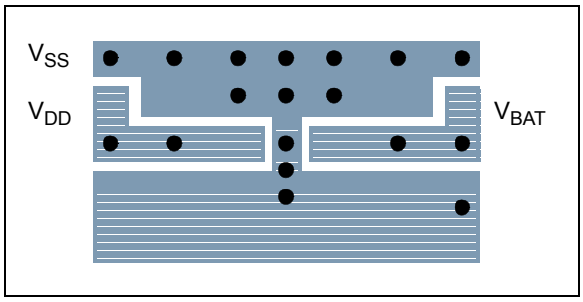


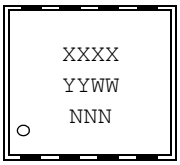
FIGURE 6-5: *Typical Layout (Bottom).*

NOTES:

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

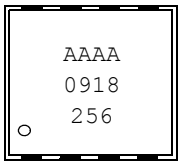
10-Lead DFN (3x3)



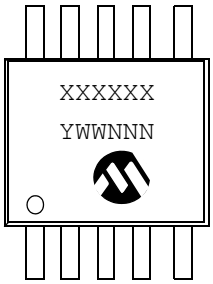
Part Number *	Marking Code	Part Number *	Marking Code
MCP73833-AMI/MF	AAAA		
MCP73833-BZI/MF	AAAB		
MCP73833-FCI/MF	AAAC	MCP73834-FCI/MF	BAAC
MCP73833-GPI/MF	AAAD	MCP73834-GPI/MF	BAAD
MCP73833-NVI/MF	AAAF	MCP73834-NVI/MF	BAAF
MCP73833-6SI/MF	AAAH	MCP73834-6SI/MF	BAAH
MCP73833-CNI/MF	AAAK	MCP73834-CNI/MF	BAAK

* Consult Factory for Alternative Device Options.

Example:



10-Lead MSOP



Part Number *	Marking Code	Part Number *	Marking Code
MCP73833-AMI/UN	833AMI		
MCP73833-BZI/UN	833BZI		
MCP73833-FCI/UN	833FCI	MCP73834-FCI/UN	834FCI
MCP73833-GPI/UN	833GPI	MCP73834-GPI/UN	834GPI
MCP73833-NVI/UN	833NVI	MCP73834-NVI/UN	834NVI
MCP73833-CNI/UN	833CNI	MCP73834-CNI/UN	834CNI

* Consult Factory for Alternative Device Options.

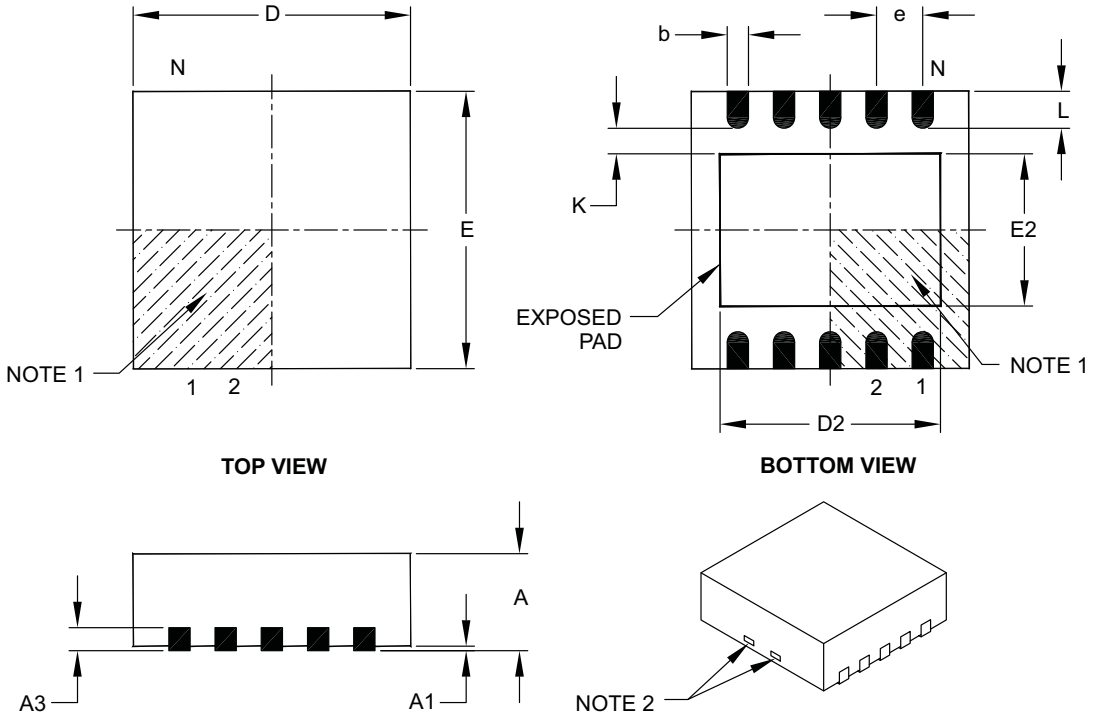
Example:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.35	2.48
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.40	1.58	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

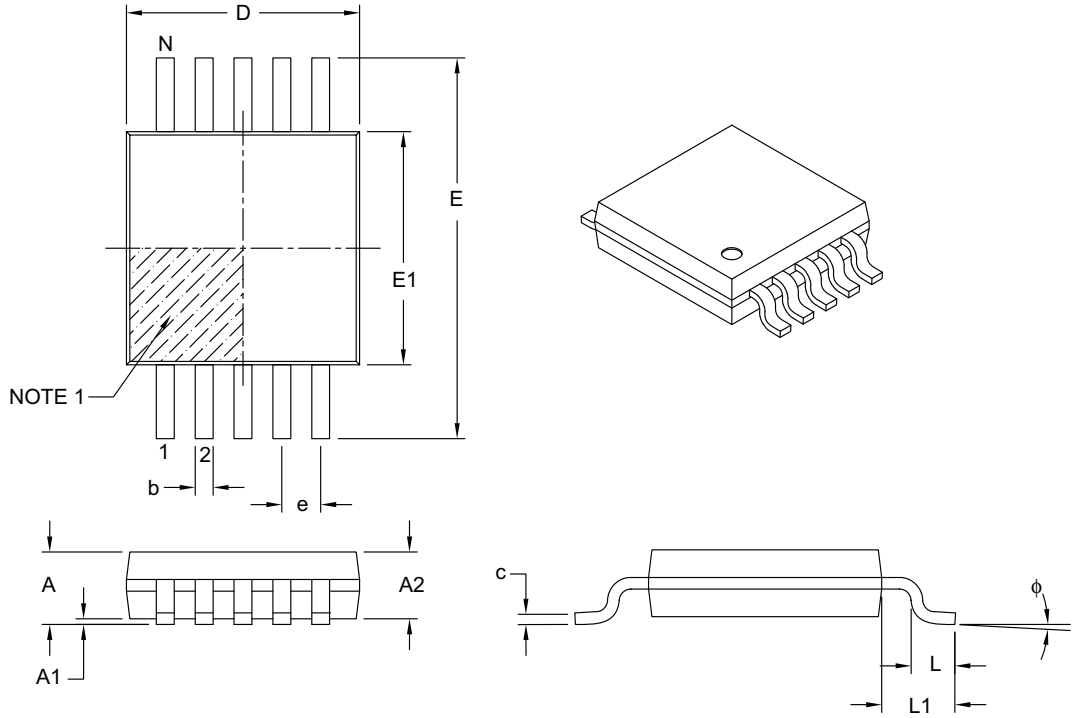
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-063B

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.15	–	0.33

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (May 2009)

The following is the list of modifications:

1. Added the MCP73833-6SI/MF and MCP73834-6SI/MF10-lead DFN packages.
2. Updated DFN pinout.
3. Updated Package Outline Drawings.
4. Updated Appendix A Revision History.

Revision A (September 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X/	XX
Device	Output Options*	Temp.	Package

Device:	MCP73833:	1A Fully Integrated Charger, PG function on pin 7
	MCP73833T:	1A Fully Integrated Charger, PG function on pin 7 (Tape and Reel)
	MCP73834:	1A Fully Integrated Charger, TE function on pin 7
	MCP73834T:	1A Fully Integrated Charger, TE function on pin 7 (Tape and Reel)
Output Options * *	* Refer to table below for different operational options.	
	* * Consult Factory for Alternative Device Options.	
Temperature:	I =	-40°C to +85°C
Package Type:	MF =	Plastic Dual Flat No Lead (DFN) (3x3x0.9 mm Body), 10-lead
	UN =	Plastic Micro Small Outline Package (MSOP), 10-lead

Examples: * *

a) MCP73833-AMI/UN: 10-lead MSOP pkg.
b) MCP73833-BZI/UN: 10-lead MSOP pkg.
c) MCP73833-CNI/MF: 10-lead DFN pkg.
d) MCP73833-FCI/UN: 10-lead MSOP pkg.
e) MCP73833-GPI/UN: 10-lead MSOP pkg.
f) MCP73833-NVI/MF: 10-lead DFN pkg.
g) MCP73833-6SI/MF: 10-lead DFN pkg.

a) MCP73834-CNI/MF: 10-lead DFN pkg.
b) MCP73834-FCI/UN: 10-lead MSOP pkg.
c) MCP73834-GPI/UN: 10-lead MSOP pkg.
d) MCP73834-NVI/MF: 10-lead DFN pkg.
e) MCP73834-6SI/MF: 10-lead DFN pkg.

* * Consult Factory for Alternative Device Options

Part Number	V_{REG}	I_{PREG}/I_{REG}	V_{PTH}/V_{REG}	I_{TERM}/I_{REG}	V_{RTH}/V_{REG}	Timer Period
MCP73833-AMI/MF	4.20V	10%	71.5%	7.5%	96.5%	0 hours
MCP73833-BZI/MF	4.20V	100%	N/A	7.5%	96.5%	0 hours
MCP73833-CNI/MF	4.20V	10%	71.5%	20%	94%	4 hours
MCP73833-FCI/MF	4.20V	10%	71.5%	7.5%	96.5%	6 hours
MCP73833-GPI/MF	4.20V	100%	N/A	7.5%	96.5%	6 hours
MCP73833-NVI/MF	4.35V	10%	71.5%	7.5%	96.5%	6 hours
MCP73833-6SI/MF	4.50V	10%	71.5%	7.5%	96.5%	6 hours
MCP73833-AMI/UN	4.20V	10%	71.5%	7.5%	96.5%	0 hours
MCP73833-FCI/UN	4.20V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-BZI/MF	4.20V	100%	N/A	7.5%	96.5%	0 hours
MCP73834-CNI/MF	4.20V	10%	71.5%	20%	94%	4 hours
MCP73834-FCI/MF	4.20V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-NVI/MF	4.35V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-6SI/MF	4.50V	10%	71.5%	7.5%	96.5%	6 hours
MCP73834-FCI/UN	4.20V	10%	71.5%	7.5%	96.5%	6 hours

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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