# Dual EIA-423/EIA-232D **Line Driver**

The MC3488A dual is single-ended line driver has been designed to satisfy the requirements of EIA standards EIA-423 and EIA-232D, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. It is suitable for use where signal wave shaping is desired and the output load resistance is greater than 450  $\Omega$ . Output slew rates are adjustable from 1.0 µs to 100 µs by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility.

#### **Features**

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for V<sub>EE</sub> Supply
- Second Source µA9636A
- Pb-Free Packages are Available



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#### **MARKING DIAGRAMS**



SOIC-8 **D SUFFIX CASE 751** 





PDIP-8 P1 SUFFIX **CASE 626** 



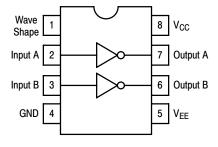
= Assembly Location

L, WL = Wafer Lot Y, YY = Year W, WW = Work Week

■ or G = Pb-Free Package

(Note: Microdot may be in either location)

# **PIN CONNECTIONS**



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

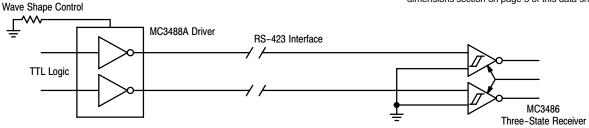


Figure 1. Simplified Application

#### MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Power Supply Voltages		V <sub>CC</sub> V <sub>EE</sub>	+ 15 – 15	V
Output Current	Source Sink	I <sub>O+</sub> I <sub>O-</sub>	+ 150 – 150	mA
Operating Ambient Temperature		T <sub>A</sub>	0 to + 70	°C
Junction Temperature Range		TJ	150	°C
Storage Temperature Range		T <sub>stg</sub>	- 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### **RECOMMENDED OPERATING CONDITIONS**

Characteristic	Symbol	Min	Тур	Max	Unit
Power Supply Voltages	V <sub>CC</sub> V <sub>EE</sub>	10.8 - 13.2	12 – 12	13.2 - 10.8	V
Operating Temperature Range	T <sub>A</sub>	0	25	70	°C
Wave Shaping Resistor	R <sub>WS</sub>	10	_	1000	kΩ

#### TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply over recommended operating conditions)

Characteristic	Symbol	Min	Тур	Max	Unit
Input Voltage – Low Logic State	V <sub>IL</sub>	_	-	0.8	V
Input Voltage – High Logic State	V <sub>IH</sub>	2.0	-	_	V
Input Current – Low Logic State (V <sub>IL</sub> = 0.4 V)	I <sub>IL</sub>	- 80	-	-	μΑ
Input Current – High Logic State (V <sub>IH</sub> = 2.4 V) (V <sub>IH</sub> = 5.5 V)	I <sub>IH1</sub> I <sub>IH2</sub>	_ _	_ _	10 100	μΑ
Input Clamp Diode Voltage (I <sub>IK</sub> = - 15 mA)	V <sub>IK</sub>	- 1.5	-	_	V
Output Voltage – Low Logic State $(R_L = \infty)$ , EIA–423 $(R_L = 3.0 \text{ k}\Omega)$ , EIA–232D $(R_L = 450 \Omega)$ , EIA–423	V <sub>OL</sub>	- 6.0 - 6.0 - 6.0	- - -	- 5.0 - 5.0 - 4.0	V
Output Voltage – High Logic State $(R_L = \infty)$ , EIA–423 $(R_L = 3.0 \text{ k}\Omega)$ , EIA–232D $(R_L = 450 \Omega)$ , EIA–423	V <sub>OH</sub>	5.0 5.0 4.0	- - -	6.0 6.0 6.0	V
Output Resistance ( $R_L \ge 450 \Omega$ )	R <sub>O</sub>	_	25	50	Ω
Output Short-Circuit Current (Note 2) $  (V_{in} = V_{out} = 0 \text{ V}) $ $  (V_{in} = V_{IH(Min)}, V_{out} = 0 \text{ V}) $	I <sub>OSH</sub> I <sub>OSL</sub>	- 150 + 15	_ _	- 15 + 150	mA
Output Leakage Current (Note 3) ( $V_{CC} = V_{EE} = 0 \text{ V}, -6.0 \text{ V} \leq V_0 \leq 6.0 \text{ V}$ )	I <sub>ox</sub>	- 100	-	100	μΑ
Power Supply Currents (R <sub>W</sub> = 100 k $\Omega$ , R <sub>L</sub> = $\infty$ , V <sub>IL</sub> $\leq$ V <sub>in</sub> $\leq$ V <sub>IH</sub> )	I <sub>CC</sub> I <sub>EE</sub>	- - 18	- -	+ 18 -	mA

One output shorted at a time.
 No V<sub>EE</sub> diode required.

<sup>1.</sup> Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

**TRANSITION TIMES** (Unless otherwise noted,  $C_L$  = 30 pF, f = 1.0 kHz,  $V_{CC}$  = -  $V_{EE}$  = 12.0 V  $\pm$  10%,  $T_A$  = 25°C,  $R_L$  = 450  $\Omega$ . Transition times measured 10% to 90% and 90% to 10%)

Characteristic		Symbol	Min	Тур	Max	Unit
Transition Time, Low-to-High State Output	$(R_W = 10 \text{ k}\Omega)$ $(R_W = 100 \text{ k}\Omega)$ $(R_W = 500 \text{ k}\Omega)$ $(R_W = 1000 \text{ k}\Omega)$	t⊤LH	0.8 8.0 40 80		1.4 14 70 140	μs
Transition Time, High-to-Low State Output	$(R_W = 10 \text{ k}\Omega)$ $(R_W = 100 \text{ k}\Omega)$ $(R_W = 500 \text{ k}\Omega)$ $(R_W = 1000 \text{ k}\Omega)$	t <sub>THL</sub>	0.8 8.0 40 80		1.4 14 70 140	μs

#### **ORDERING INFORMATION**

Device	Operating Temperature Range	Package	Shipping <sup>†</sup>
MC3488AD		SOIC-8	98 Units / Rail
MC3488ADG		SOIC-8 (Pb-Free)	98 Units / Rail
MC3488ADR2		SOIC-8	1000 / Tape & Reel
MC3488ADR2G	T <sub>A</sub> = 0 to +70°C	SOIC-8 (Pb-Free)	1000 / Tape & Reel
MC3488AP1		PDIP-8	50 Units / Rail
MC3488AP1G		PDIP-8 (Pb-Free)	50 Units / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

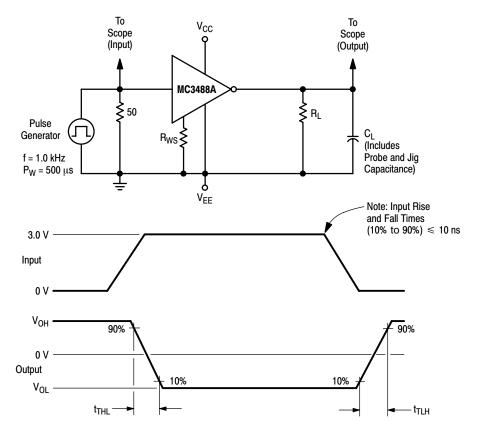


Figure 2. Test Circuit and Waveforms for Transition Times

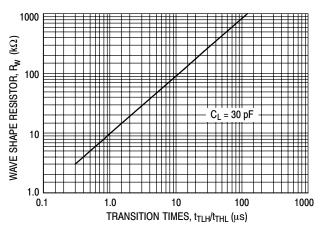


Figure 3. Output Transition Times versus Wave Shape Resistor Value

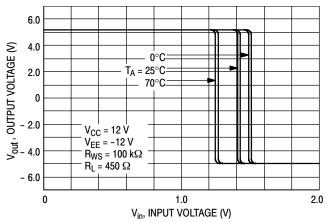
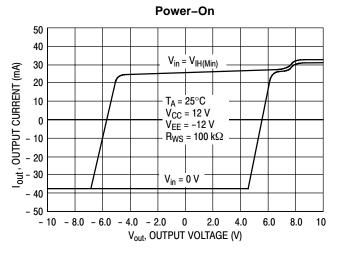


Figure 4. Input/Output Characteristics versus Temperature



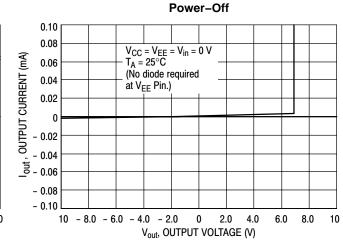


Figure 5. Output Current versus Output Voltage

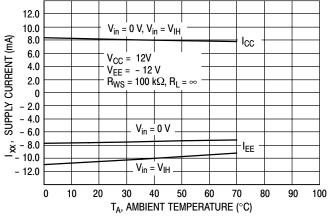


Figure 6. Supply Current versus Temperature

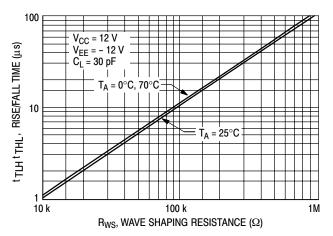


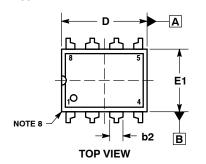
Figure 7. Rise/Fall Time versus RWS

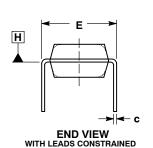


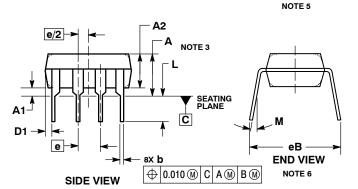
PDIP-8 CASE 626-05 ISSUE P

**DATE 22 APR 2015** 









STYLE 1: PIN 1. AC IN 2. DC + IN 3. DC - IN 4. AC IN 5. GROUND 6. OUTPUT 7. AUXILIARY 8. V<sub>CC</sub>

#### NOTES

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
  DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
- AGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
  DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
- DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
- 6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE
- DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
- 8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α		0.210		5.33
A1	0.015		0.38	
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060	TYP	1.52 TYP	
С	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005		0.13	
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
е	0.100	BSC	BSC 2.54 BS	
eВ		0.430		10.92
L	0.115	0.150	2.92	3.81
М		10°		10°

# **GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

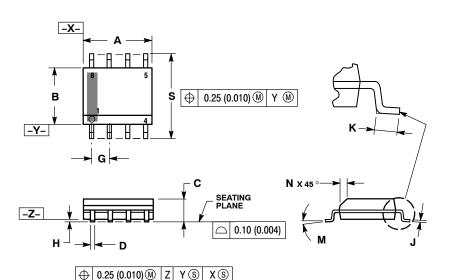
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SOIC-8 NB CASE 751-07 **ISSUE AK** 

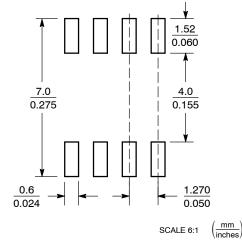
**DATE 16 FEB 2011** 



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

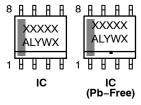
	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.80	5.00	0.189	0.197
В	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27	1.27 BSC		0 BSC
Н	0.10	0.25	0.004	0.010
7	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

#### **SOLDERING FOOTPRINT\***



<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

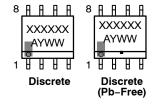
#### **GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code = Assembly Location = Wafer Lot

= Year = Work Week

= Pb-Free Package



XXXXXX = Specific Device Code = Assembly Location Α

= Year ww = Work Week

= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

#### **STYLES ON PAGE 2**

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### SOIC-8 NB CASE 751-07 ISSUE AK

### **DATE 16 FEB 2011**

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11:  PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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