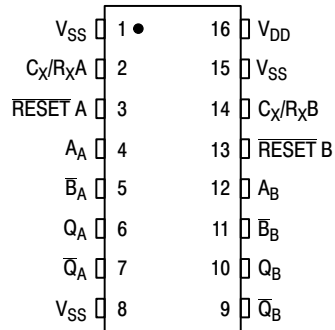
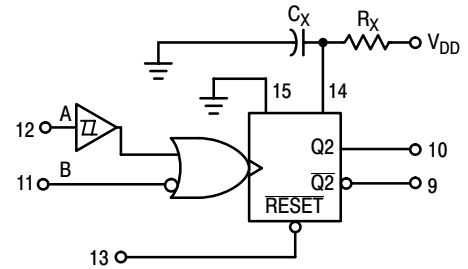
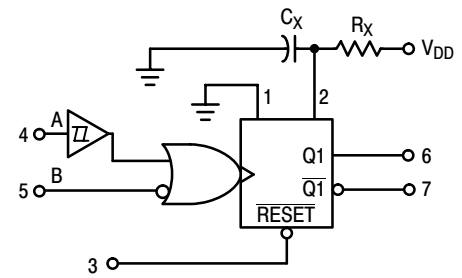


MC14538B

PIN ASSIGNMENT

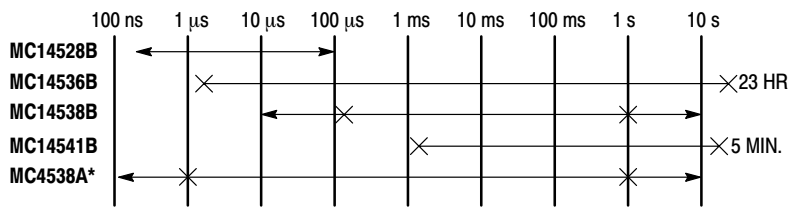


BLOCK DIAGRAM



R_X AND C_X ARE EXTERNAL COMPONENTS.
V_{DD} = PIN 16
V_{SS} = PIN 8, PIN 1, PIN 15

ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2 - 6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ← →
RECOMMENDED PULSE WIDTH RANGE × ×

ORDERING INFORMATION

Device	Package	Shipping [†]
MC14538BCP	PDIP-16	500 Units / Rail
MC14538BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14538BD	SOIC-16	48 Units / Rail
MC14538BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14538BDR2	SOIC-16	2500 Units / Tape & Reel
MC14538BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14538BDW	SOIC-16 WB	47 Units / Rail
MC14538BDWR2	SOIC-16 WB	1000 Units / Tape & Reel
MC14538BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel
MC14538BDTR2	TSSOP-16*	2500 Units / Tape & Reel
MC14538BF	SOEIAJ-16	50 Units / Rail
MC14538BFG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC14538BFEL	SOEIAJ-16	2000 Units / Tape & Reel
MC14538BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC14538B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	"1" Level V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	– 3.0	–	– 2.4	– 4.2	–	– 1.7	–	mAdc
		5.0	– 0.64	–	– 0.51	– 0.88	–	– 0.36	–	
		10	– 1.6	–	– 1.3	– 2.25	–	– 0.9	–	
		15	– 4.2	–	– 3.4	– 8.8	–	– 2.4	–	
	Sink I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current, Pin 2 or 14	I _{in}	15	–	±0.05	–	±0.00001	±0.05	–	±0.5	μAdc
Input Current, Other Inputs	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance, Pin 2 or 14	C _{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) Q = Low, $\bar{Q}$ = High	I _{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current, Active State (Both) (Per Package) Q = High, $\bar{Q}$ = Low	I _{DD}	5.0	–	2.0	–	0.04	0.20	–	2.0	mAdc
		10	–	2.0	–	0.08	0.45	–	2.0	
		15	–	2.0	–	0.13	0.70	–	2.0	
Total Supply Current at an external load capacitance (C _L) and at external timing network (R _X , C _X) (Note 3)	I _T	5.0 10	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8.0 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ where: I _T in μA (one monostable switching only), C _X in μF, C _L in pF, R _X in k ohms, and f in Hz is the input frequency.							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

MC14538B

SWITCHING CHARACTERISTICS (Note 4) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ (Note 5)	Max	
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 255 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$ Reset to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$	t_{PLH}, t_{PHL}	5.0	–	300	600	ns
		10	–	150	300	
		15	–	100	220	
		5.0	–	250	500	ns
		10	–	125	250	
		15	–	95	190	
Input Rise and Fall Times Reset B Input A Input	t_r, t_f	5	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
		5	–	300	1.0	ms
		10	–	1.2	0.1	
		15	–	0.4	0.05	
		5	No Limit			–
		10				
		15				
Input Pulse Width A, B, or Reset	t_{WH}, t_{WL}	5.0	170	85	–	ns
		10	90	45	–	
		15	80	40	–	
Retrigger Time	t_{rr}	5.0	0	–	–	ns
		10	0	–	–	
		15	0	–	–	
Output Pulse Width — Q or $\bar{Q}$ Refer to Figures 8 and 9 $C_X = 0.002 \mu\text{F}$, $R_X = 100 \text{ k}\Omega$ $C_X = 0.1 \mu\text{F}$, $R_X = 100 \text{ k}\Omega$ $C_X = 10 \mu\text{F}$, $R_X = 100 \text{ k}\Omega$	T	5.0	198	210	230	μs
		10	200	212	232	
		15	202	214	234	
		5.0	9.3	9.86	10.5	ms
		10	9.4	10	10.6	
		15	9.5	10.14	10.7	
		5.0	0.91	0.965	1.03	s
		10	0.92	0.98	1.04	
		15	0.93	0.99	1.06	
		5.0	–	± 1.0	± 5.0	%
		10	–	± 1.0	± 5.0	
		15	–	± 1.0	± 5.0	

4. The formulas given are for the typical characteristics only at 25°C .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	(Note 6)	$\text{k}\Omega$
External Timing Capacitance	C_X	–	0	–	No Limit (Note 7)	μF

6. The maximum usable resistance R_X is a function of the leakage of the capacitor C_X , leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for $R_X > 1 \text{ M}\Omega$.

7. If $C_X > 15 \mu\text{F}$, use discharge protection diode per Fig. 11.

MC14538B

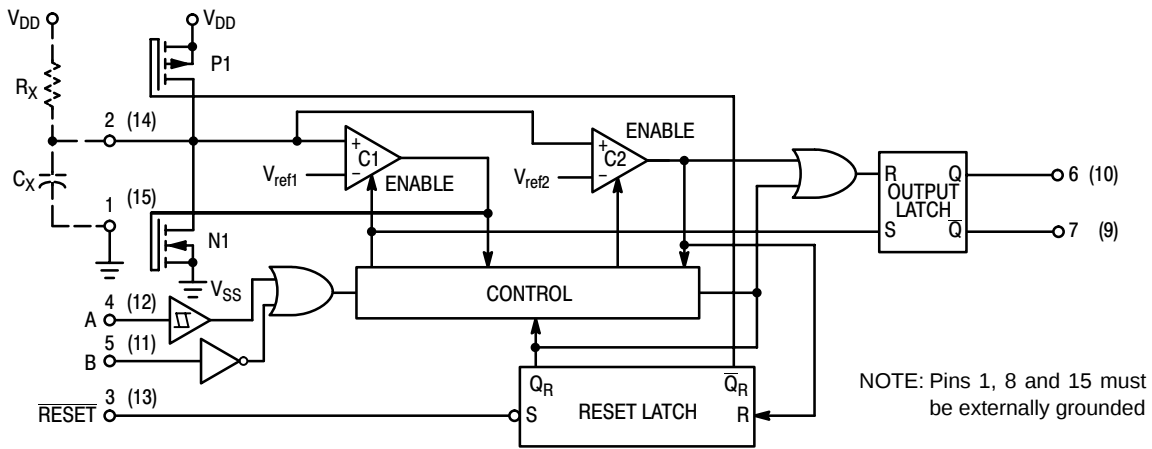


Figure 1. Logic Diagram
(1/2 of Device Shown)

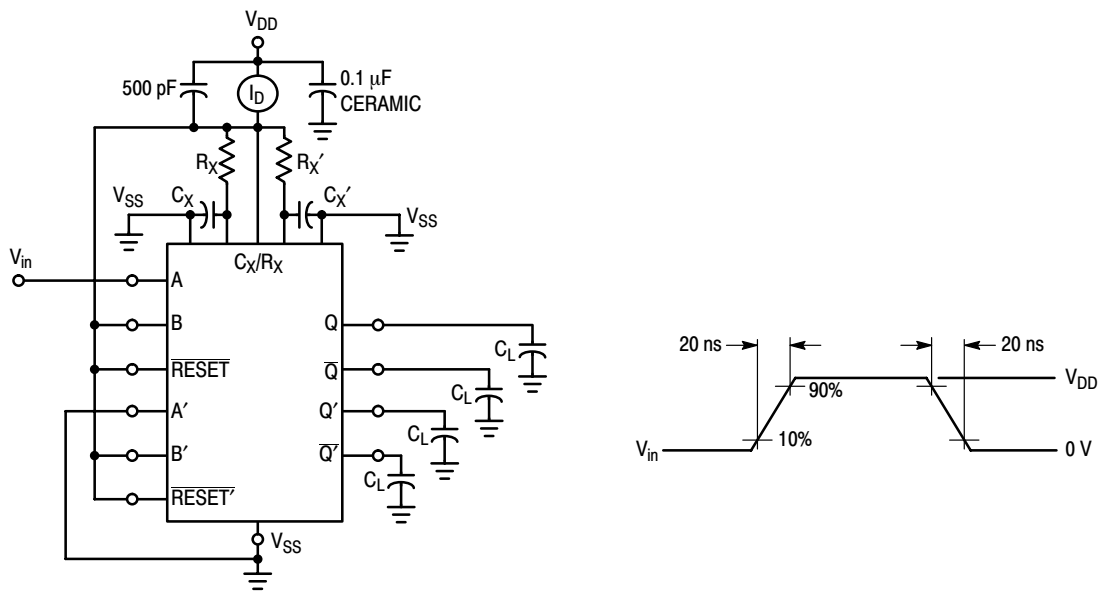
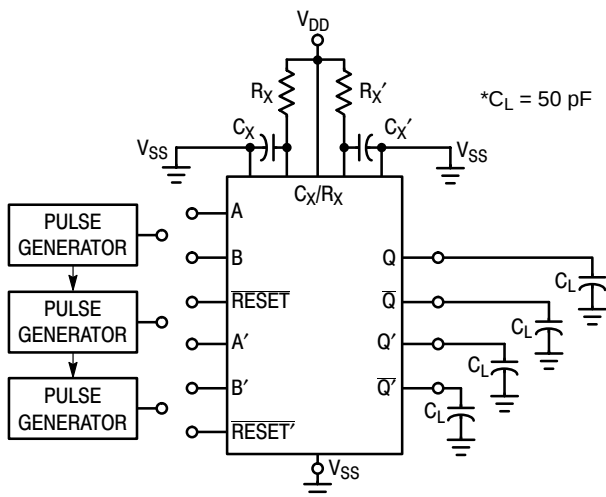


Figure 2. Power Dissipation Test Circuit and Waveforms



INPUT CONNECTIONS

Characteristics	Reset	A	B
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} , T , t_{WH} , t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} , T , t_{WH} , t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH} , t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.
NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.

PG1 =

PG2 =

PG3 =

Figure 3. Switching Test Circuit

MC14538B

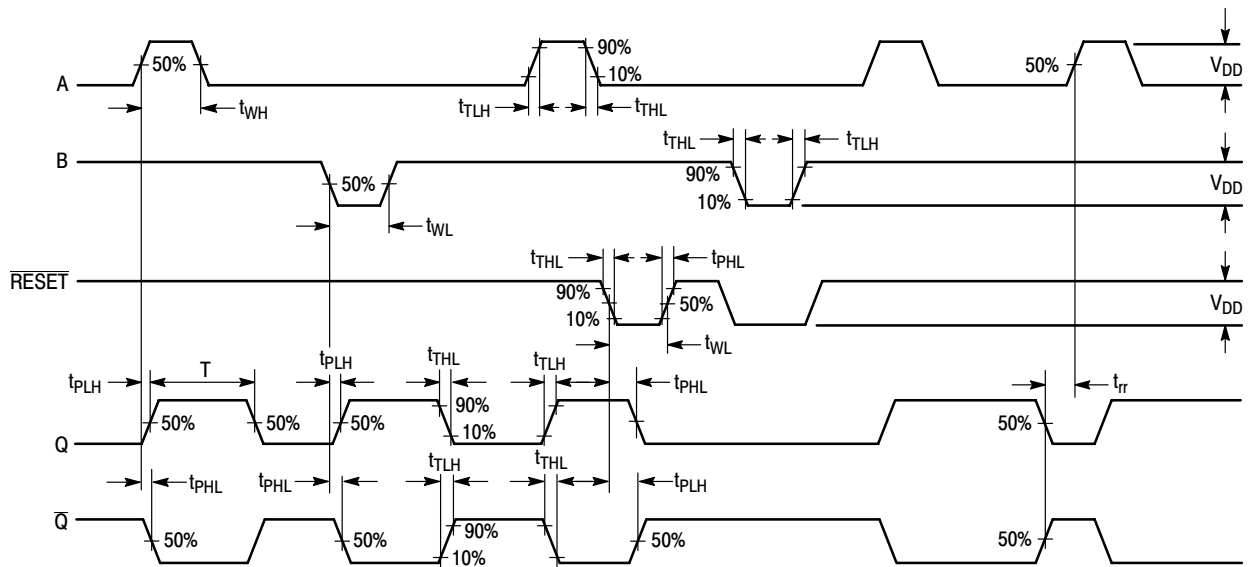


Figure 4. Switching Test Waveforms

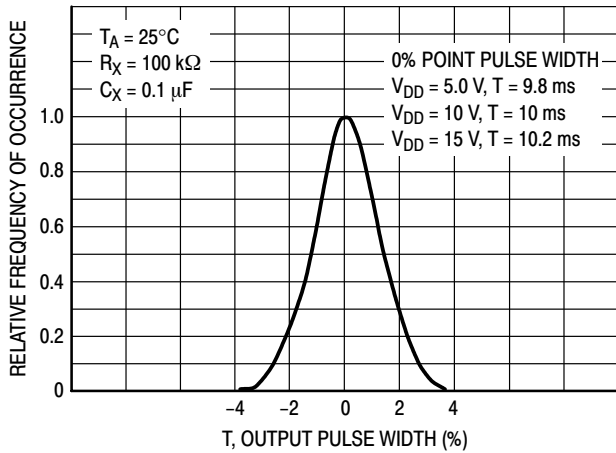


Figure 5. Typical Normalized Distribution of Units for Output Pulse Width

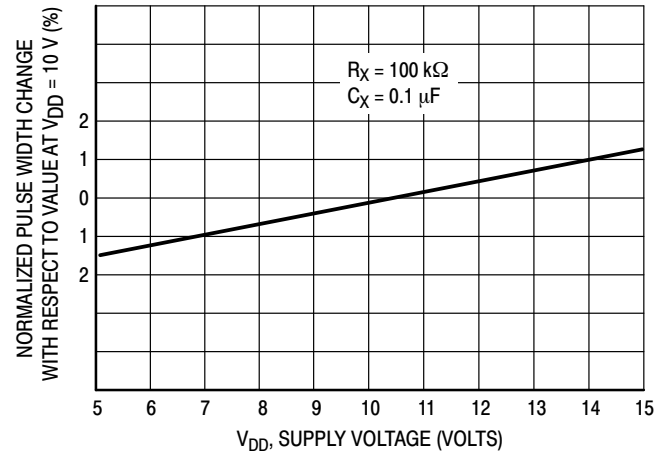


Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

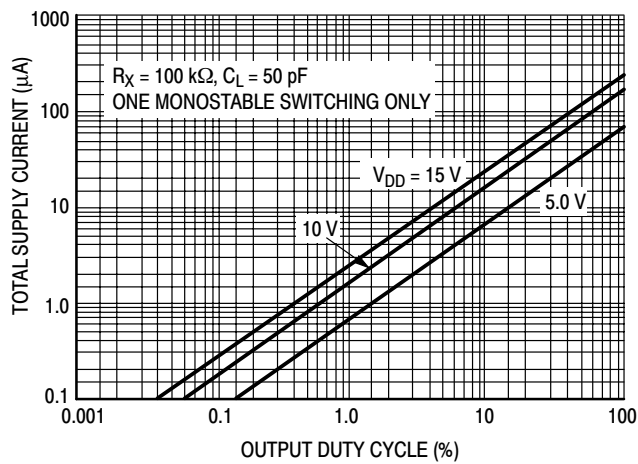


Figure 7. Typical Total Supply Current versus Output Duty Cycle

FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\bar{Q}$
H		H		
H	L			
H		L	Not Triggered	Not Triggered
H	H		Not Triggered	Not Triggered
H	L, H,	H	Not Triggered	Not Triggered
H	L	L, H,	Not Triggered	Not Triggered
L	X	X	L	H
	X	X	Not Triggered	Not Triggered

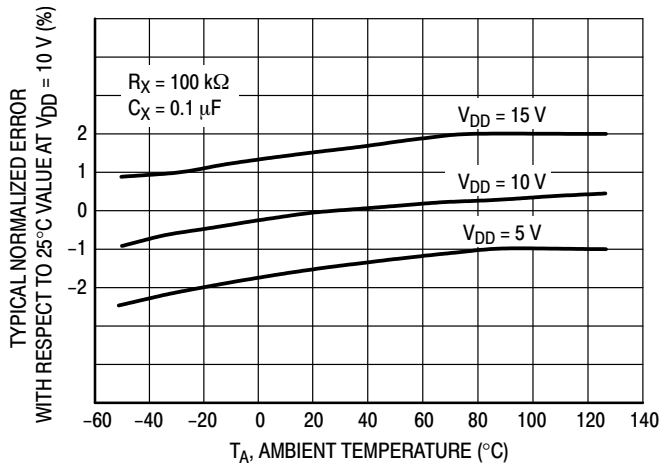


Figure 8. Typical Error of Pulse Width Equation versus Temperature

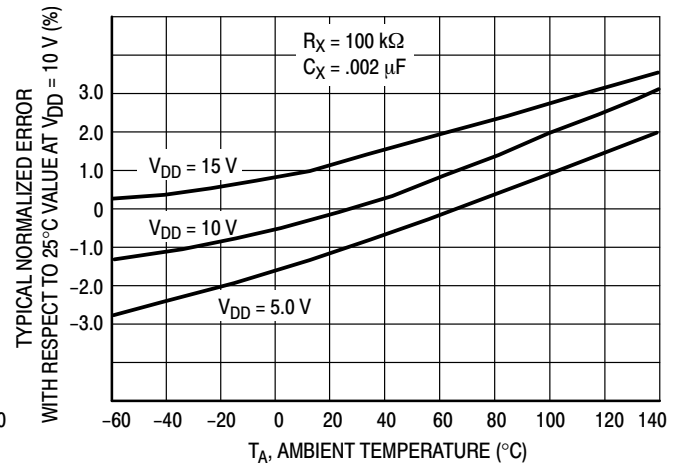


Figure 9. Typical Error of Pulse Width Equation versus Temperature

THEORY OF OPERATION

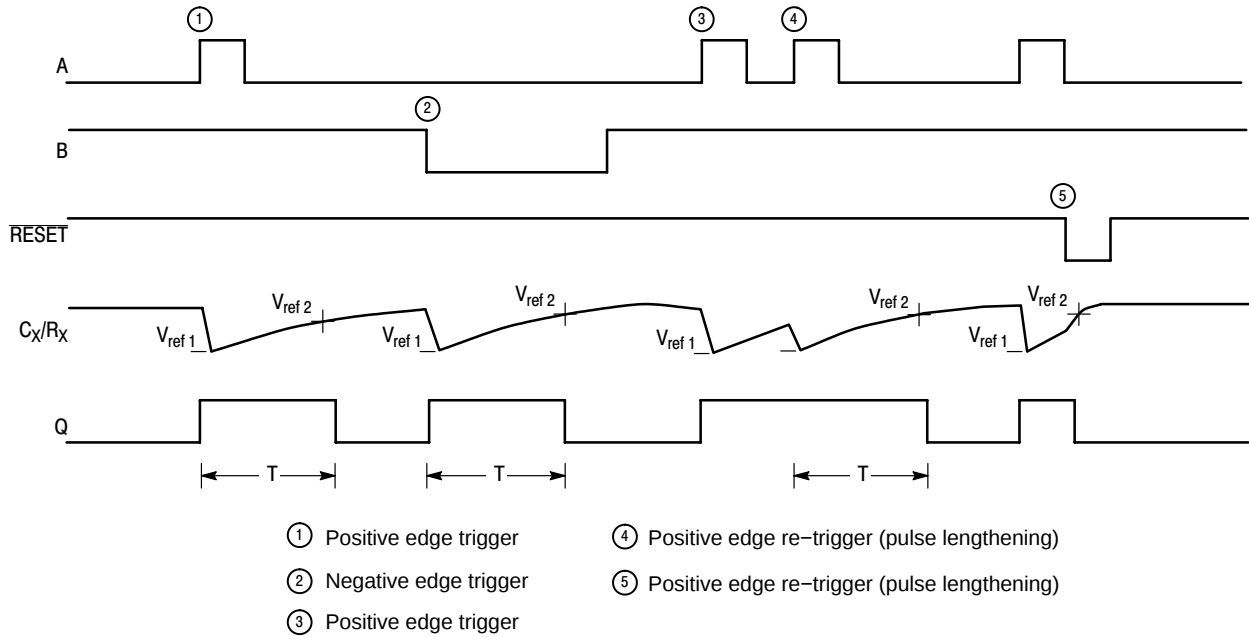


Figure 10. Timing Operation

TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD} . When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and $\overline{\text{Reset}}$ are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until $V_{\text{ref}1}$ is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X , toward V_{DD} . When the voltage across C_X equals $V_{\text{ref}2}$, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state, C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are “off” with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X , R_X , or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{\text{ref}1}$, but has not yet reached $V_{\text{ref}2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at C_X/R_X will again drop to $V_{\text{ref}1}$ before progressing along the RC charging curve toward V_{DD} . The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse

on $\overline{\text{Reset}}$ sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 ⑤. When the voltage on the capacitor reaches $V_{\text{ref}2}$, the reset latch will clear, and will then be ready to accept another pulse. If the $\overline{\text{Reset}}$ input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the $\overline{\text{Reset}}$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER-DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than $(V_{DD}) \cdot (C)/(10 \text{ mA})$. For example, if $V_{DD} = 10 \text{ V}$ and $C_X = 10 \mu\text{F}$, the V_{DD} supply should discharge no faster than $(10 \text{ V}) \times (10 \mu\text{F})/(10 \text{ mA}) = 10 \text{ ms}$. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, D_X , connected as shown in Fig. 11.

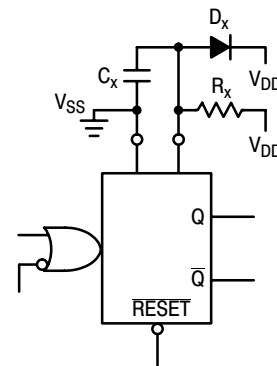


Figure 11. Use of a Diode to Limit Power Down Current Surge

TYPICAL APPLICATIONS

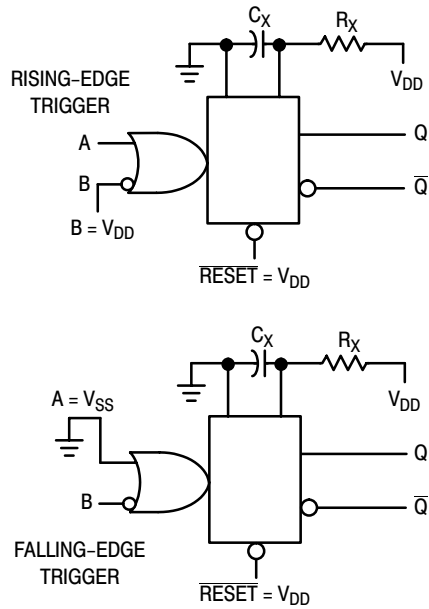


Figure 12. Retriggerable Monostables Circuitry

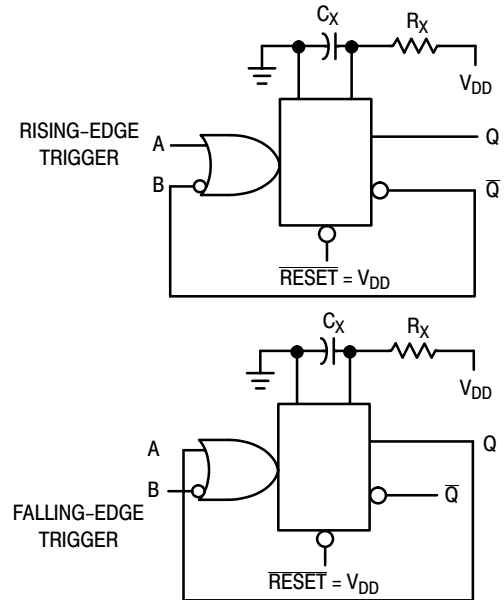


Figure 13. Non-Retriggerable Monostables Circuitry

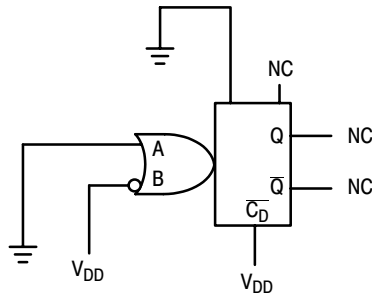
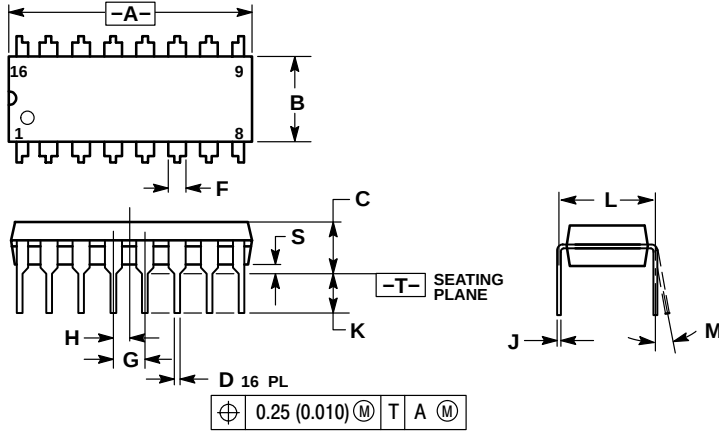


Figure 14. Connection of Unused Sections

MC14538B

PACKAGE DIMENSIONS

PDIP-16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE T

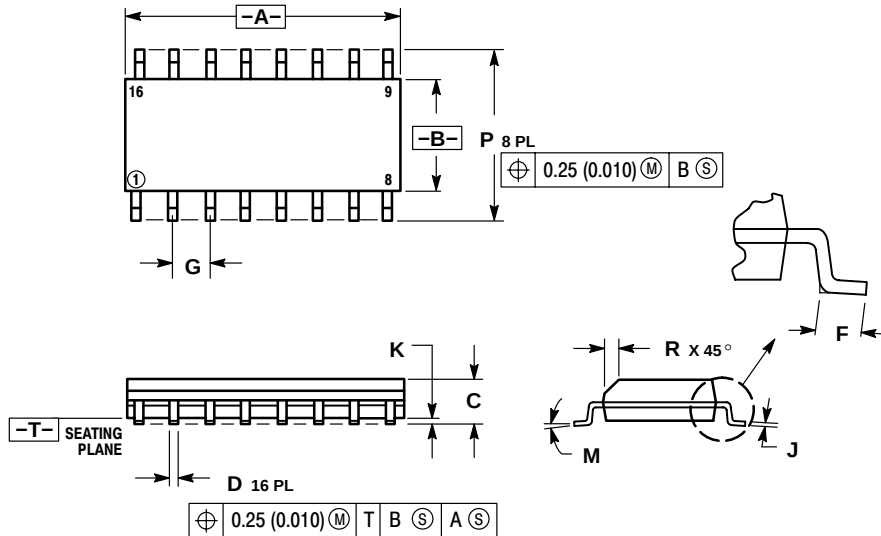


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



NOTES:

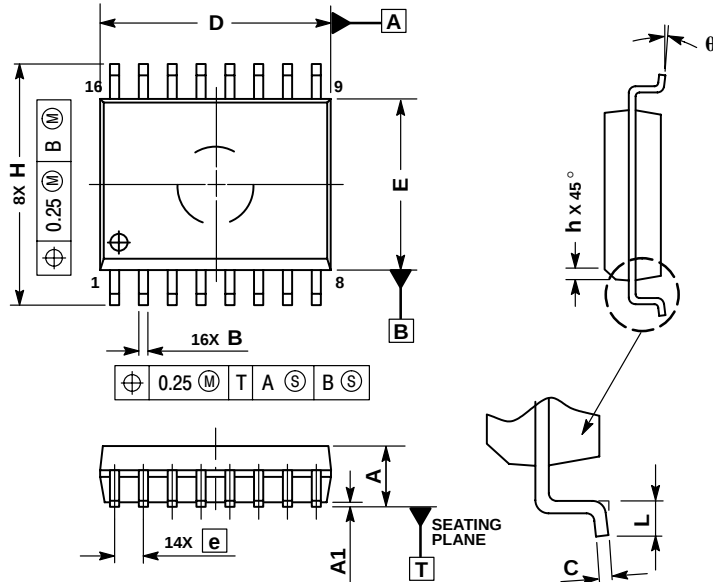
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MC14538B

PACKAGE DIMENSIONS

SOIC-16 WB
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G-03
ISSUE C

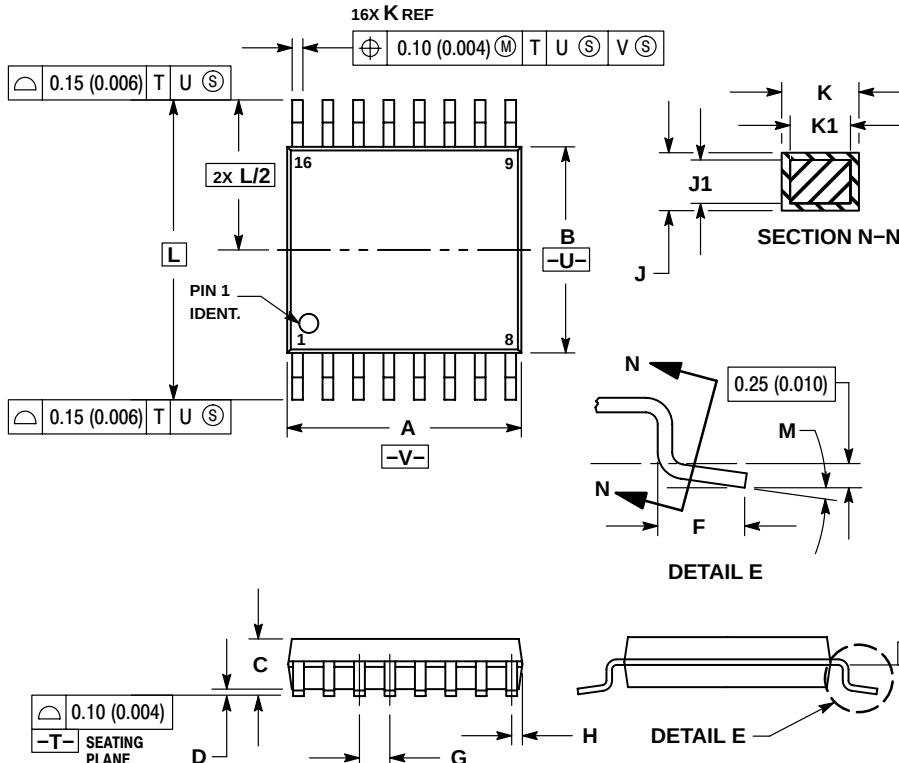


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

TSSOP-16
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F-01
ISSUE A



NOTES:

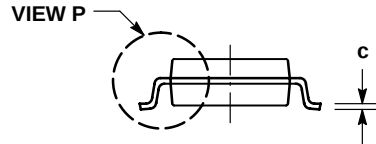
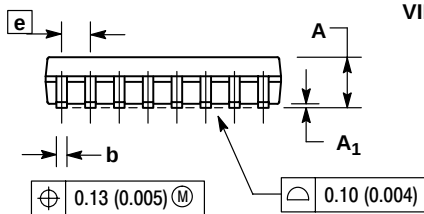
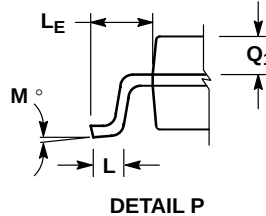
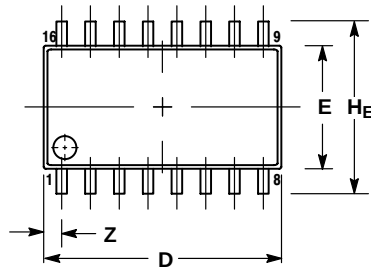
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

		MILLIMETERS		INCHES	
DIM		MIN	MAX	MIN	MAX
A		4.90	5.10	0.193	0.200
B		4.30	4.50	0.169	0.177
C		---	1.20	---	0.047
D		0.05	0.15	0.002	0.006
F		0.50	0.75	0.020	0.030
G		0.65	BSC	0.026	BSC
H		0.18	0.28	0.007	0.011
J		0.09	0.20	0.004	0.008
J1		0.09	0.16	0.004	0.006
K		0.19	0.30	0.007	0.012
K1		0.19	0.25	0.007	0.010
L		6.40	BSC	0.252	BSC
M		0°	8°	0°	8°

MC14538B

PACKAGE DIMENSIONS

SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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