Absolute Maximum Ratings

V_{DD}, $\overline{MUTE}$, SET to GND .....-0.3V to +6V
INL, INR to GND .....(V_{DD} - 6V) to (V_{DD} + 0.3V)
Continuous Current In/Out of V_{DD} 30mA
Continuous Current In/Out of $\overline{MUTE}$ 30mA
Continuous Current In/Out of SET 30mA
Continuous Current In/Out of INL, INR and GND 390mA
Continuous Power Dissipation (T_A = +70°C)
6-Bump UCSP (derate 3.9mW/°C above +70°C).....308.3mW
6-Pin µDFN (derate 4.5mW/°C above +70°C) 357.8mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Temperature (soldering)
Reflow.....+235°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

UCSP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ...259.50°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... N/A

µDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ...223.60°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....122°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 3.0V, V_{GND} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

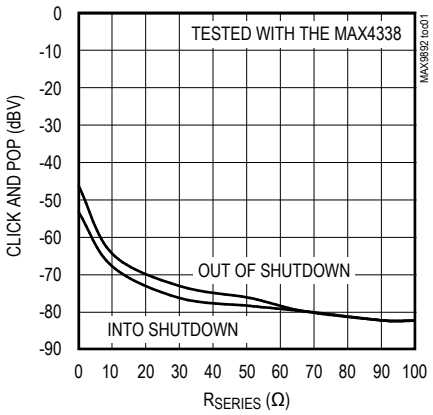
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by R_{ON} test	1.7		5.5	V
Recommended Supply Voltage Range	V_{DD}	(Note 3)	1.7		3.6	V
Supply Current	I_{DD}	V_{DD} = 5.5V, T_A = +25°C (Note 4)		0.6	1	µA
Input Voltage Range	V_{IN}	Guaranteed by input leakage current test	V_{DD} - 5.5V		V_{DD}	V
Turn-On Time (Figure 1)	t_{ON}	Measured from $\overline{MUTE}$ = GND and input voltage settled to 90% of its final value		130		ns
Turn-Off Time (Figure 1)	t_{OFF}	C_{SET} = 500pF	4	10	17	ms
		C_{SET} = 50pF		1		
		C_{SET} = 50nF		1000		
Turn-On Time Resistor	R_{SET}	C_{SET} = 500pF	350	800	1300	kΩ
Switch On-Resistance	R_{ON}	V_{DD} = 3.0V		0.3		Ω
		V_{DD} = 1.7V			2	
		V_{DD} = 5.5V			1	
Click-and-Pop Reduction		R_{SERIES} = 30Ω, R_{LOAD} = 16Ω		35		dB
Input Leakage Current	I_{IN}	T_A = +25°C, V_{IN} = V_{DD} - 5.5V, V_{DD} = 1.7V			±1	µA
		T_A = +25°C, V_{IN} = V_{DD}, V_{DD} = 5.5V			±1	
$\overline{MUTE}$ Leakage Current	$I_{\overline{MUTE}}$	V_{DD} = 5.5V, $V_{\overline{MUTE}}$ = 0 or 5.5V, T_A = +25°C			±1	µA
$\overline{MUTE}$ Input-Voltage High	V_{IH}		1.5			V
$\overline{MUTE}$ Input-Voltage Low	V_{IL}				0.4	V

Note 2: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Operating within the recommended supply voltage range ensures that negative audio signals are not limited by the device. Supply voltages above the recommended supply voltage range may limit the headphone amplifier's maximum output voltage.
Note 4: Supply current is measured when switches are off.

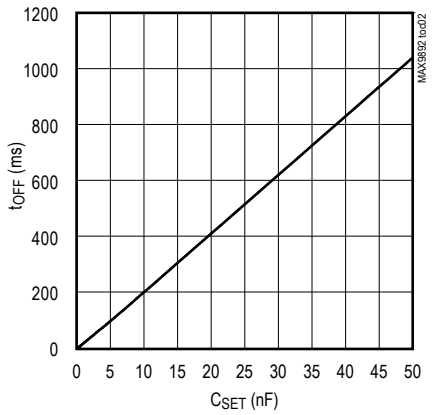
Typical Operating Characteristics

(V_{DD} = 3.0V, V_{GND} = 0, T_A = +25°C, unless otherwise noted.)

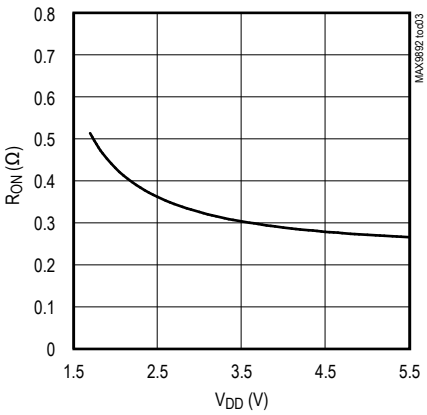
CLICK AND POP vs. R_{SERIES}



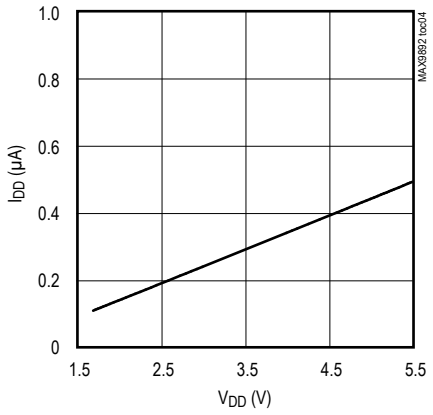
t_{OFF} vs. C_{SET}



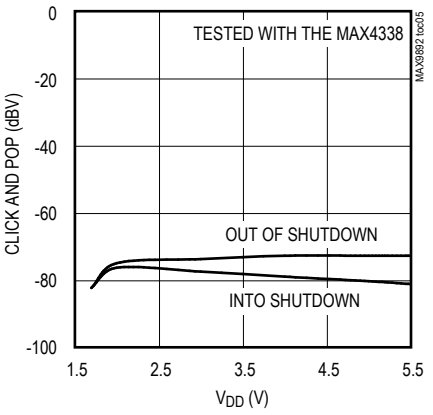
R_{ON} vs. SUPPLY VOLTAGE



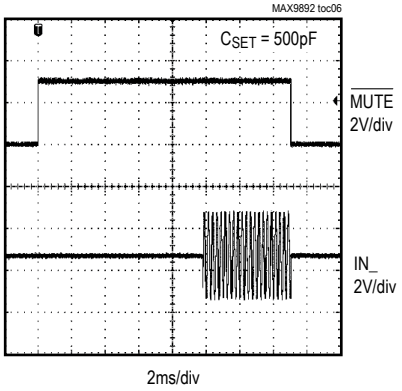
SUPPLY CURRENT vs. SUPPLY VOLTAGE



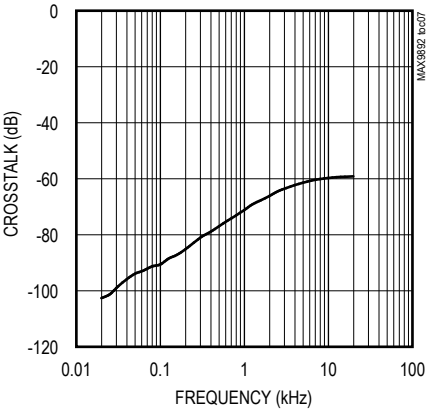
CLICK AND POP vs. V_{DD}



SWITCH TURN-OFF/ON TIME



CROSSTALK vs. FREQUENCY



Pin Description

UCSP BUMP	µDFN PIN	NAME	FUNCTION
A1	1	INL	Left-Channel Input. Connect INL in between the output coupling capacitor and the headphone jack.
A2	2	GND	Ground
A3	3	INR	Right-Channel Input. Connect INR in between the output coupling capacitor and the headphone jack.
B1	6	$\overline{MUTE}$	Active-Low Enable
B2	5	V_{DD}	Power Supply
B3	4	SET	Turn-Off Time Set. Connect an external capacitor in between SET and GND to set the switch open delay; see the *Setting the Turn-Off Time* section for more information.

Timing Diagram

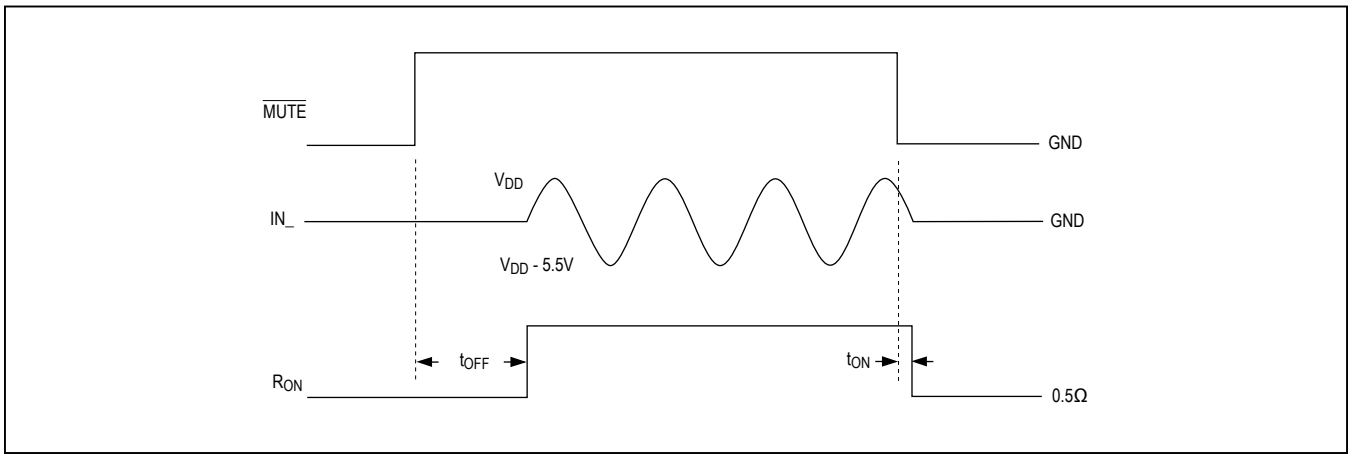


Figure 1. Turn-On/Off Time

Detailed Description

The MAX9892 is the second-generation click-and-pop eliminator designed to be used with conventional headphone amplifiers. The MAX9892 works by adding a low-impedance current path from the headphone side of the DC-blocking capacitor to ground. Drive $\overline{MUTE}$ low when turning off the amplifier, and high when enabling the amplifier. A short turn-on time allows the switches in the MAX9892 to close before the DC-blocking capacitors have significantly discharged, eliminating clicks and pops at amplifier turn-off. An adjustable turn-off time allows the delay to be set to mask all clicks and pops during amplifier turn-on.

Setting the Turn-Off Time

The MAX9892 features a SET input that allows the turn-off time to be adjusted from 1ms to 1000ms to match the click-and-pop profile of the amplifier startup. The value of an external capacitor sets the switch open delay, as shown in the following equation:

$$t_{ON}\ (ms) = 0.02 \times C_{SET}\ (pF)$$

When the headphone amplifier is enabled, the MAX9892 automatically waits the set delay time before opening the analog switches. This allows amplifier turn-on click and pop to be eliminated.

Applications Information

Setting the Supply Voltage

The MAX9892 operates from 1.7V to 3.6V supply voltage. The inputs, INL and INR, accept voltage swings from V_{DD} to V_{DD} - 5.5V. The audio signal applied to a headphone is ground biased, meaning that the signal swings just as much negative as positive. Since the MAX9892 input voltage is limited to V_{DD} - 5.5V on the negative side, the voltage on V_{DD} must be set properly to pass the audio signal when the switch is open (Figure 2).

A voltage-divider can be used to scale down an available supply voltage as shown in Figure 3. The voltage-divider allows the creation of a supply voltage for the MAX9892 that is low enough to allow the negative portion of the audio signal to pass. When using large resistances for the voltage-divider, the supply current affects what resistors to use. Select R_2 between 10kΩ to 1MΩ for a given supply voltage. Use the following equation to calculate the R_1:

$$R_1 = \frac{(V_{AMP} - V_{DD})}{I_2 + I_{DD}}$$

where V_{AMP} is the supply voltage of the amplifier, and I_2 is the current through R_2. For a signal of ±2V in reference to GND, the MAX9892 supply can be set from 2V to 3.5V.

Selecting Series Resistors

A series resistor (R_{SERIES}), as shown in the *Typical Operating Circuit*, is necessary to achieve optimal click-and-pop reduction. See the Click and Pop vs. R_{SERIES} graph in the *Typical Operating Characteristics* for details on how much click-and-pop reduction to expect for a given series resistor.

Layout Considerations

Bypass V_{DD} to GND with a 0.1µF capacitor. The 0.1µF bypass capacitor should be positioned as close as possible to V_{DD}. Minimize trace length from GND to solid system ground plane to ensure optimum performance.

Refer to the MAX9892 Evaluation Kit for a proven PCB layout.

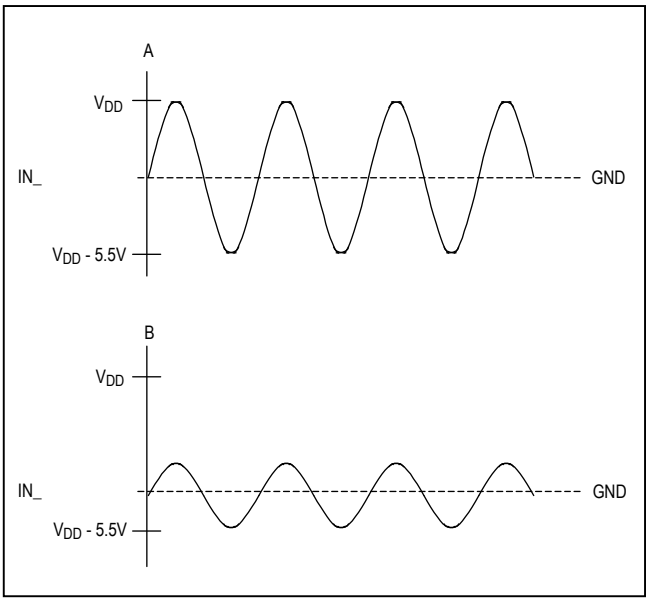


Figure 2. Proper Supply Selected for a Given Input Signal.
A: Supply Voltage with a Large Signal;
B: Supply Voltage with a Small Signal

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape-carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Understanding the Basics of the Wafer-Level Chip-Scale Package (WL-CSP)* at www.maximintegrated.com/ucsp. See Figure 4 for the recommended MAX9892 PCB footprint.

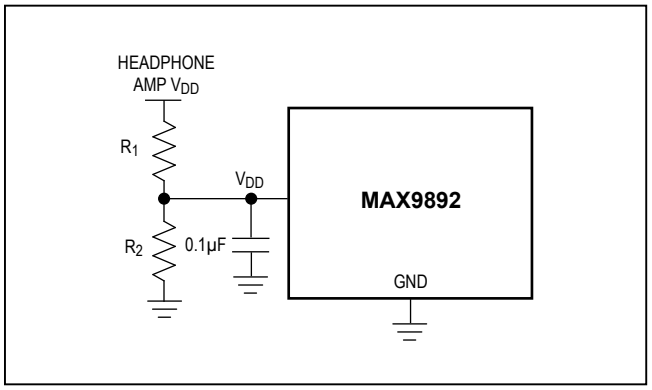


Figure 3. Scaling Down the Supply Voltage with a Voltage Divider

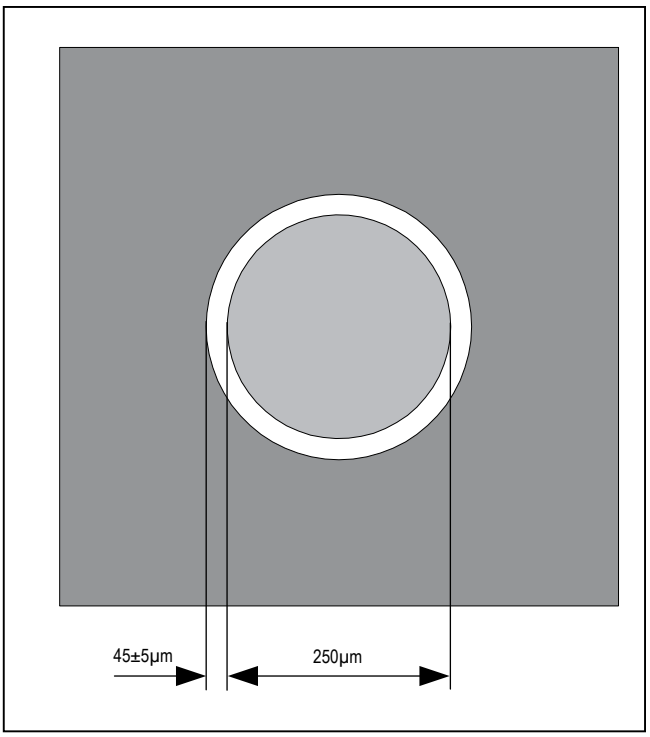


Figure 4. PCB Footprint Recommendation Diagram

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 UCSP	R61A1+1	21-0228
6 µDFN	L622-1	21-0164

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/08	Initial release	—
1	12/16	Added *Package Thermal Characteristics* section and updated *Electrical Characteristics* table	1, 2

