Low-Cost, Ultra-Small, Single/Dual/Quad Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS}) ....-0.3V to +6V
Voltage Inputs (IN+, IN- to V_{SS}). ....-0.3V to (V_{DD} + 0.3V)
Differential Input Voltage (IN+ to IN-) ....+6.6V
Output Short-Circuit
Duration ....2s to Either V_{DD} or V_{SS}
Current into Any Pin 20mA
Continuous Power Dissipation (T_A = +70°C) ....
5-Pin SC70 (derate 3.1mW/°C above +70°C)...............247mW
5-Pin SOT23 (derate 7.1mW/°C above +70°C).............571mW
6-Pin SC70 (derate 3.1mW/°C above +70°C)...............245mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C).............696mW
8-Pin SOT23 (derate 9.1mW/°C above +70°C).............727mW
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
8-Pin SO (derate 5.88mW/°C above +70°C).................471mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
14-Pin SO (derate 8.33mW/°C above +70°C)...............667mW
Operating Temperature Range
Automotive Application....................-40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = 0, V_{CM} = 0, $V_{\overline{SHDN}}$ = +5V (Note 1), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{DD}	Guaranteed by PSRR test	2.5		5.5	V
Supply Current per Comparator	I_{DD}			35	55	µA
Supply Current in Shutdown		$V_{\overline{SHDN}}$ = 0 (Note 1)		0.05	1	µA
Shutdown Input Bias Current		$V_{\overline{SHDN}}$ = 0 to V_{DD} (Note 1)		0.1	2.5	µA
Shutdown Logic High		(Note 1)	0.7 × V_{DD}			V
Shutdown Logic Low		(Note 1)			0.3 × V_{DD}	V
Input Offset Voltage	V_{OS}	(Note 3)		±1	±5	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}			±1		µV/°C
Hysteresis		(Note 4)		4		mV
Input Bias Current	I_{BIAS}			8	80	nA
Input Offset Current	I_{OS}			±2	±60	nA
Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test	V_{SS}		V_{DD} - 1.1	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \le V_{CM} \le$ (V_{DD} - 1.1V), V_{DD} = +5.5V	72	100		dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = +2.5V to +5.5V	72	100		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} = 0, $V_{\overline{SHDN}}$ = +5V (Note 1), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

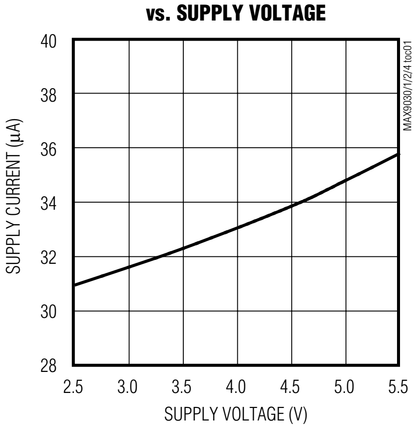
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage-Swing	V_{OL}, V_{OH}	V_{OH} = V_{DD} - V_{OUT}, (V_{IN+} - V_{IN-}) ≥ 20mV	I_{SOURCE} = 10µA		2		mV
			I_{SOURCE} = 4mA		165	400	
		V_{OL} = V_{OUT} - V_{SS}, (V_{IN-} - V_{IN+}) ≥ 20mV	I_{SINK} = 10µA		2		
			I_{SINK} = 4mA		165	400	
Output Short-Circuit Current	I_{SC}				45		mA
Shutdown Mode Output Leakage		$V_{\overline{SHDN}}$ ≤ (0.3 × V_{DD}), V_{OUT} = 0 to V_{DD} (Note 1)			±0.01	±3.5	µA
Propagation Delay	t_{PD+}, t_{PD-}	R_L = 10kΩ, C_L = 15pF (Note 5)	V_{OD} = 10mV		228		ns
			V_{OD} = 100mV		188		
Rise/Fall-Time	t_R, t_F	V_{DD} = +5V, R_L = 10kΩ, C_L = 15pF (Note 6)			20		ns
Shutdown Delay Time ON/OFF		(Note 1)			40		ns
Shutdown Delay Time OFF/ON		(Note 1)			400		ns
Power-On Time		R_L = 10kΩ, C_L = 15pF			200		ns
Maximum Capacitive Load	C_L	No sustained oscillations			150		pF

Note 1: MAX9030 only.
Note 2: All devices are production tested at +25°C. All temperature limits are guaranteed by design.
Note 3: Comparator Input Offset is defined as the center of the hysteresis zone.
Note 4: Hysteresis is defined as the difference of the trip points required to change comparator output states.
Note 5: V_{OD} is the overdrive that is beyond the offset and hysteresis-determined trip points.
Note 6: Rise and fall times are measured between 10% and 90% at OUT.

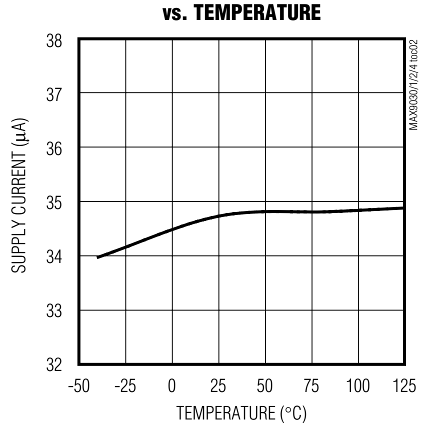
Typical Operating Characteristics

(V_{DD} = +5V, V_{SS} = 0, V_{CM} = 0, R_L = 10kΩ, C_L = 15pF, V_{OD}= 100mV, T_A = +25°C, unless otherwise noted.)

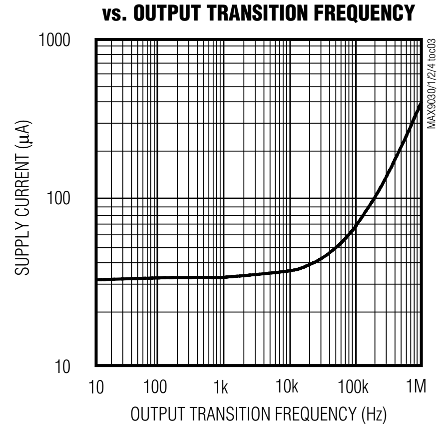
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. OUTPUT TRANSITION FREQUENCY

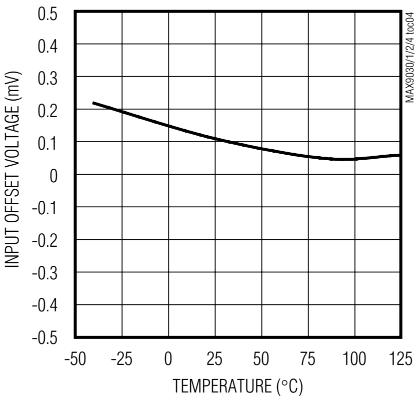


Low-Cost, Ultra-Small, Single/Dual/Quad Single-Supply Comparators

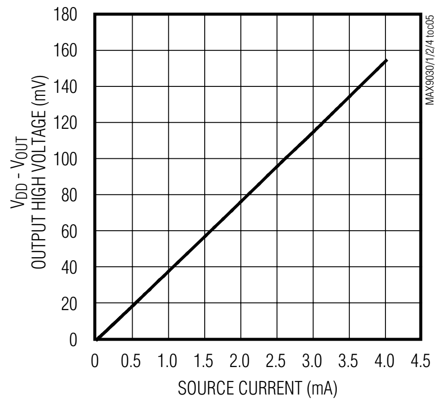
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} = 0, R_L = 10kΩ, C_L = 15pF, V_{OD} = 100mV, T_A = +25°C, unless otherwise noted.)

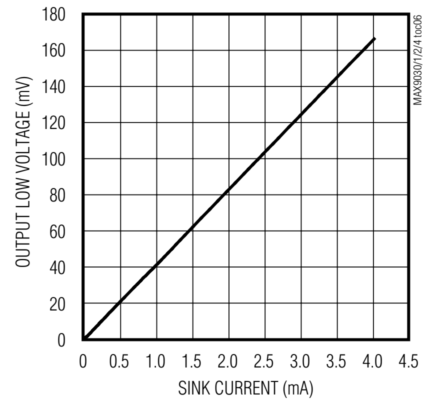
INPUT OFFSET VOLTAGE vs. TEMPERATURE



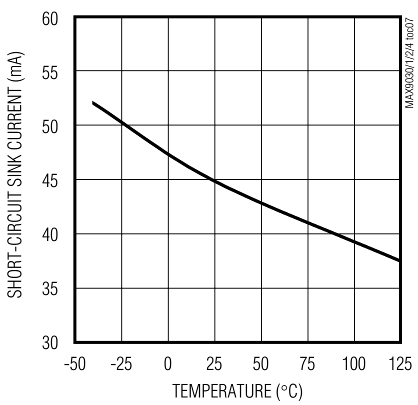
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



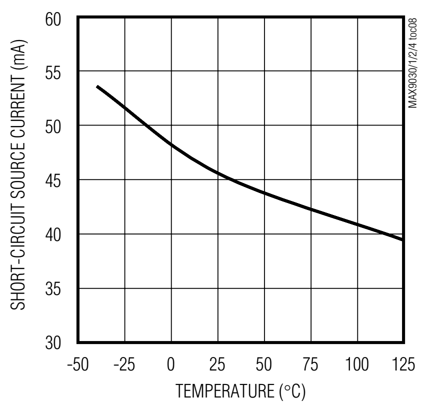
OUTPUT LOW VOLTAGE vs. SINK CURRENT



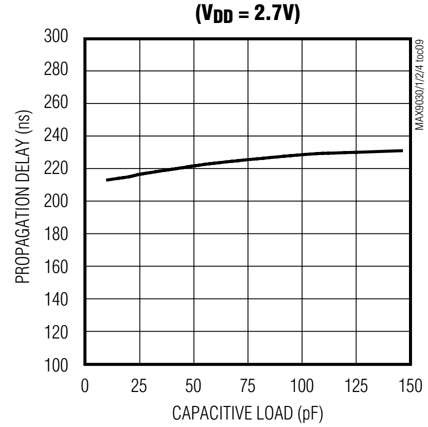
OUTPUT SHORT-CIRCUIT (SINK) CURRENT vs. TEMPERATURE



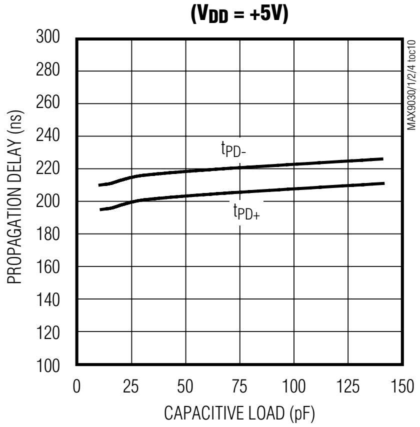
OUTPUT SHORT-CIRCUIT (SOURCE) CURRENT vs. TEMPERATURE



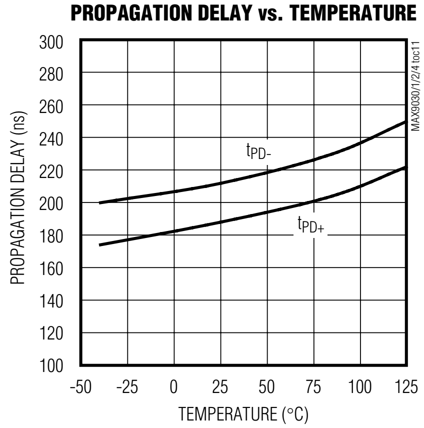
PROPAGATION DELAY vs. CAPACITIVE LOAD (V_{DD} = 2.7V)



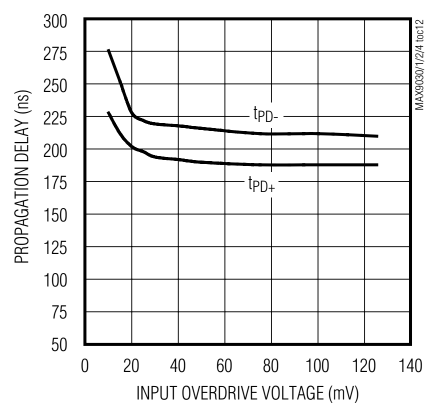
PROPAGATION DELAY vs. CAPACITIVE LOAD (V_{DD} = +5V)



PROPAGATION DELAY vs. TEMPERATURE



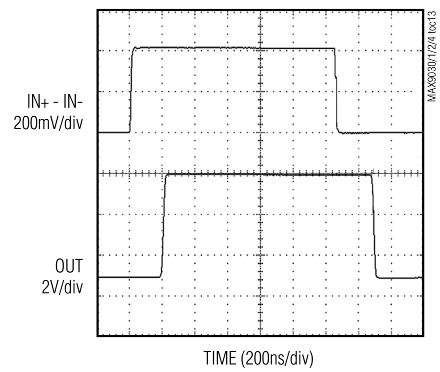
PROPAGATION DELAY vs. INPUT OVERDRIVE VOLTAGE



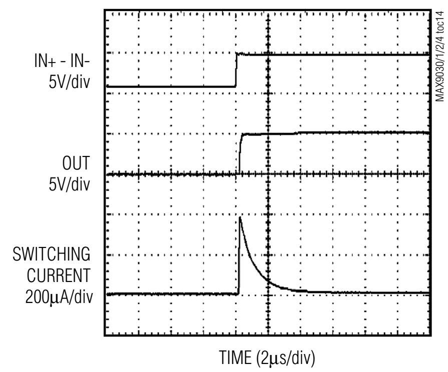
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0, V_{CM} = 0, R_L = 10kΩ, C_L = 15pF, V_{OD} = 100mV, T_A = +25°C, unless otherwise noted.)

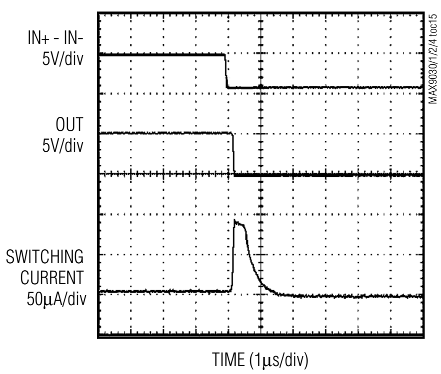
PROPAGATION DELAY



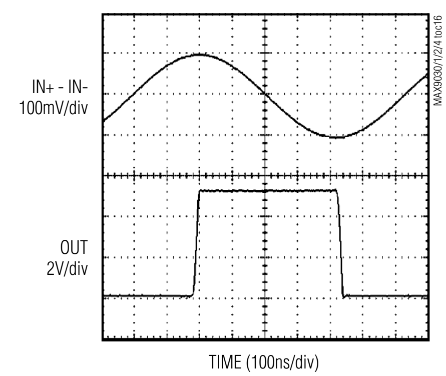
OUTPUT SWITCHING CURRENT, RISING



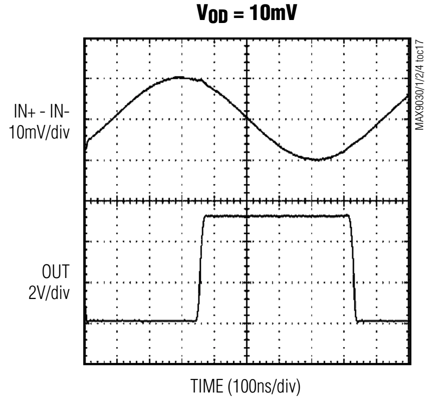
OUTPUT SWITCHING CURRENT, FALLING



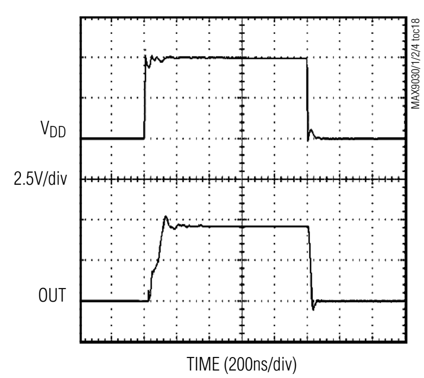
SINUSOID 1MHz RESPONSE AT 1.25MHz V_{OD} = 100mV



SINUSOID 1MHz RESPONSE AT 1.25MHz V_{OD} = 10mV



POWER-UP DELAY



Low-Cost, Ultra-Small, Single/Dual/Quad Single-Supply Comparators

Pin Description

PIN				NAME	FUNCTION
MAX9030	MAX9031	MAX9032	MAX9034		
1	1	—	—	IN+	Comparator Noninverting Input
2	2	4	11	V_{SS}	Negative Supply Voltage. Bypass with a 0.1µF capacitor.
3	3	—	—	IN-	Comparator Inverting Input
4	4	—	—	OUT	Comparator Output
5	—	—	—	$\overline{SHDN}$	Shutdown
6	5	8	4	V_{DD}	Positive Supply Voltage. Bypass with a 0.1µF capacitor.
—	—	1	1	OUTA	Comparator A Output
—	—	2	2	INA-	Comparator A Inverting Input
—	—	3	3	INA+	Comparator A Noninverting Input
—	—	5	5	INB+	Comparator B Noninverting Input
—	—	6	6	INB-	Comparator B Inverting Input
—	—	7	7	OUTB	Comparator B Output
—	—	—	8	OUTC	Comparator C Output
—	—	—	9	INC-	Comparator C Inverting Input
—	—	—	10	INC+	Comparator C Noninverting Input
—	—	—	12	IND+	Comparator D Noninverting Input
—	—	—	13	IND-	Comparator D Inverting Input
—	—	—	14	OUTD	Comparator D Output

Detailed Description

The MAX9030/MAX9031/MAX9032/MAX9034 are single/dual/quad low-cost comparators. They have an operating supply voltage from +2.5V to +5.5V when operating from a single supply and from ±1.25V to ±2.75V when operating from dual power supplies, and consume only 35µA. Their common-mode input voltage range extends from the negative supply to within 1.1V of the positive supply. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

Shutdown Mode

The MAX9030 comparator comes with a power-saving shutdown mode. When in shutdown, the supply current drops from a typical 35µA to 0.05µA, and the outputs become high impedance. $\overline{SHDN}$ has a high input impedance and typically draws 0.1µA when connected to V_{SS} or V_{DD}. A maximum logic low voltage of 0.3V × V_{DD} applied to $\overline{SHDN}$ places the device in the shutdown mode. A minimum logic high voltage of 0.7V × V_{DD} applied to $\overline{SHDN}$ will enable normal operation. To disable shutdown, connect $\overline{SHDN}$ to V_{DD}.

Applications Information

Adding Hysteresis

Hysteresis extends the comparator's noise margin by increasing the upper threshold and decreasing the lower threshold. A voltage-divider from the output of the comparator sets the trip voltage. Therefore, the trip voltage is related to the output voltage.

These comparators have 4mV internal hysteresis. Additional hysteresis can be generated with two resistors using positive feedback (Figure 1). Use the following procedure to calculate resistor values:

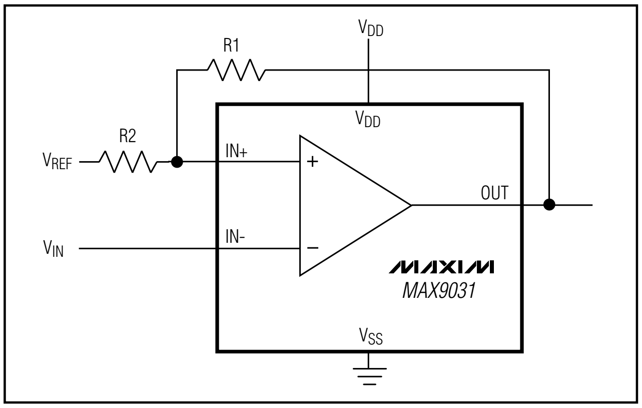


Figure 1. Additional Hysteresis

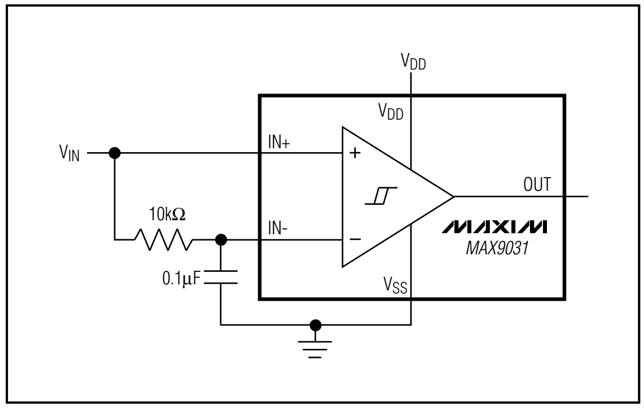


Figure 2. Time Averaging of the Input Signal for Data Recovery

1) Find the trip points of the comparator using these formulas:

$$V_{TH} = V_{REF} + [((V_{DD} - V_{REF})R2) / (R1 + R2)$$
$$V_{TL} = V_{REF}(1 - (R2 / (R1 + R2))]$$

where V_{TH} is the threshold voltage at which the comparator switches its output from high to low as V_{IN} rises above the trip point. V_{TL} is the threshold voltage at which the comparator switches its output from low to high as V_{IN} drops below the trip point.

2) The hysteresis band will be:

$$V_{HYS} = V_{TH} - V_{TL} = V_{DD}(R2 / (R1 + R2))$$

3) In this example, let V_{DD} = +5V and V_{REF} = +2.5V.

$$V_{TH} = 2.5V + 2.5(R2 / (R1 + R2))V$$

and

$$V_{TL} = 2.5[1 - (R2 / (R1 + R2))]$$

4) Select R2. In this example, we will choose 1kΩ.

5) Select V_{HYS}. In this example, we will choose 50mV.

6) Solve for R1.

$$V_{HYS} = V_{DD}(R2 / (R1 + R2))$$
$$0.050V = 5(1000\Omega/(R1 + 1000\Omega))\ V$$

where R1 ≈ 100kΩ, V_{TH} = 2.525V, and V_{TL} = 2.475V.

The above-described design procedure assumes rail-to-rail output swing. If the output is significantly loaded, the results should be corrected.

Board Layout and Bypassing

Use 100nF bypass as a starting point. Minimize signal trace lengths to reduce stray capacitance. Minimize the capacitive coupling between IN- and OUT. For slow-moving input signals (rise-time > 1ms), use a 1nF capacitor between IN+ and IN-.

Biasing for Data Recovery

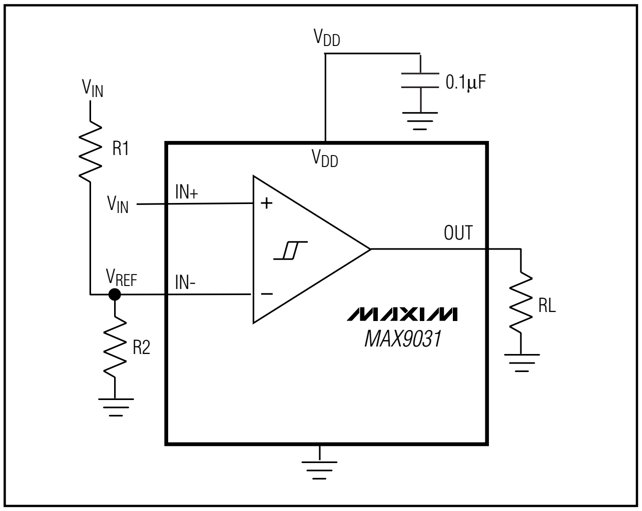
Digital data is often embedded into a bandwidth and amplitude-limited analog path. Recovering the data can be difficult. Figure 2 compares the input signal to a time-averaged version of itself. This self-biases the threshold to the average input voltage for optimal noise margin. Even severe phase distortion is eliminated from the digital output signal. Be sure to choose R1 and C1 so that:

$$f_{CAR} >> 1 / (2\pi R1C1)$$

where f_{CAR} is the fundamental carrier frequency of the digital data stream.

Low-Cost, Ultra-Small, Single/Dual/Quad Single-Supply Comparators

Typical Application Circuit

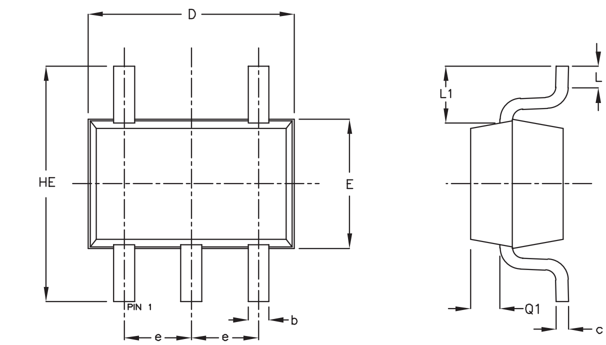


Chip Information

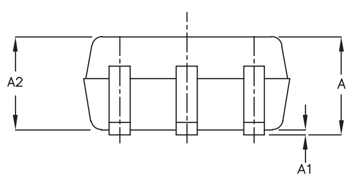
TRANSISTOR COUNT/MAX9030/MAX9031: 123
TRANSISTOR COUNT/MAX9032: 184
TRANSISTOR COUNT/MAX9034: 368

Package Information

SC70, 5L.EPS



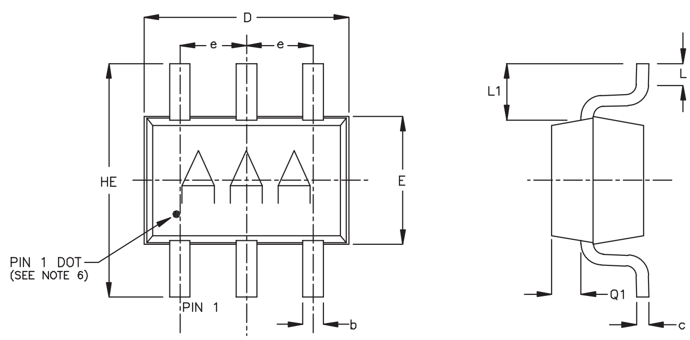
SYMBOL	MIN	MAX
e	0.65 BSC	
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425 TYP.	



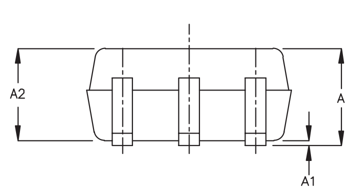
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
5. COPLANARITY 4 MILS. MAX.

MAXIM PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SC70, 5L
APPROVAL | DOCUMENT CONTROL NO. 21-0076 | REV B | 1/1

SC70, 6L.EPS



SYMBOL	MIN	MAX
e	0.65 BSC	
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425 TYP.	

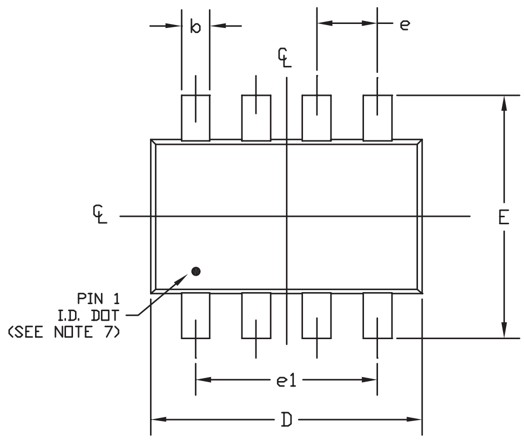


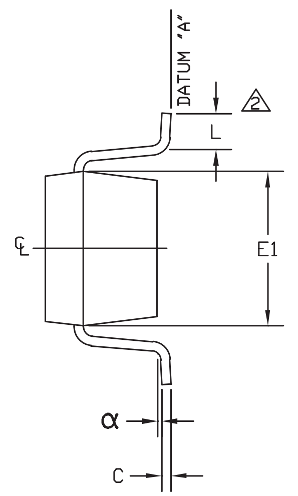
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT

MAXIM PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SC70, 6L
APPROVAL | DOCUMENT CONTROL NO. 21-0077 | REV B | 1/1

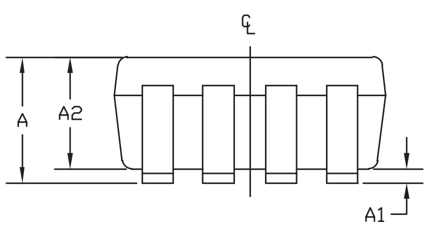
Package Information (continued)

SOT23, 8L.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



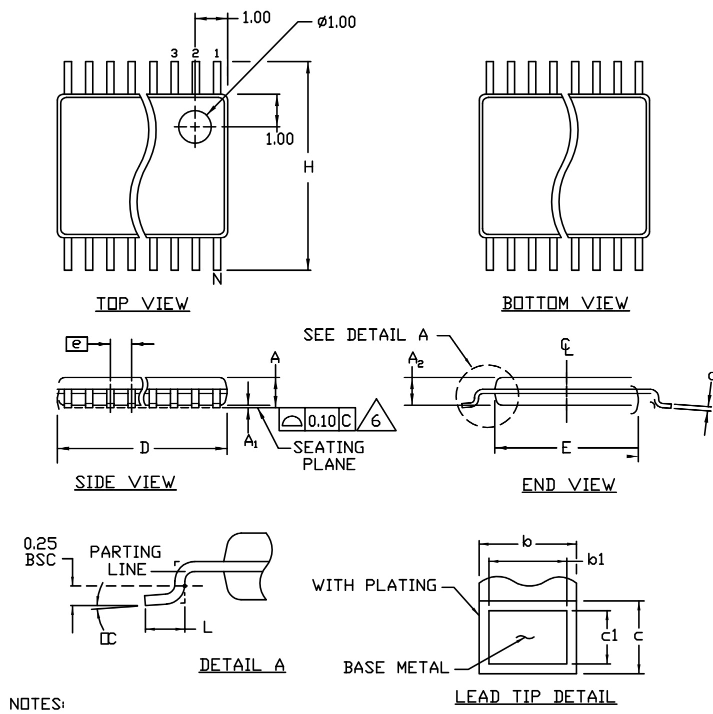
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. (2) FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.

MAXIM
PROPRIETARY INFORMATION

TITLE:			
PACKAGE OUTLINE, SOT 23, 8L			
APPROVAL	DOCUMENT CONTROL NO. 21-0078	REV B	1/1

Package Information (continued)

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC MO-153	N		VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AD	20	D	6.40	6.60	.252	.260
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS- AB, AC, AD, AE, AF
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	D	1/1

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