Smallest, Most Reliable, 12V, Infiniband-Compliant Hot-Swap Controller

ABSOLUTE MAXIMUM RATINGS

IN, POK to RET .....-0.3V to +16V
GATE to RET .....-0.3V to (V_{IN} + 7V)
OUT, ISET, CTIM to RET .....-0.3V to (V_{IN} + 0.3V)
EN, LPEN, OVP to RET .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMax (derate 5.6 mW/°C above +70°C).....444.4 mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{EN} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VB BULK SUPPLY CONTROL					
IN Supply Voltage Range		10	12	14	V
ISET Current Source		18.5	20	21.5	µA
Current-Limit Offset Voltage	V_{ISET} - V_{IN}	-4	0	+4	mV
OUT Input Current	V_{OUT} = 12V		6	12	µA
Severe Overcurrent Threshold	With respect to current regulation threshold		150		mV
25W OUT Current Regulation	R_{ISET} = 3.09kΩ ±1%, R_{SENSE} = 20mΩ ±1%	2.6	3.1	3.6	A
50W OUT Current Regulation	R_{ISET} = 3.09kΩ ±1%, R_{SENSE} = 10mΩ ±1%	5.2	6.2	7.2	A
GATE PARAMETERS					
Gate Response Time to Severe Overcurrent	V_{RSENSE} ≥ (150mV + current regulation threshold + 50mV) until V_{GATE} begins to slew low (Note 1)		100		ns
Gate Response Time to Overcurrent	V_{RSENSE} ≥ current regulation threshold + 50mV until V_{GATE} begins to slew low (Note 1)		600		ns
Gate Turn-On Current		8.4	10	11.6	µA
Gate Pulldown Current	Overcurrent, V_{RSENSE} ≥ (current regulation threshold + 100mV) (Note 1)		2.7		mA
	Severe overcurrent		350		
Gate High Voltage		V_{IN} + 4	V_{IN} + 5		V
IN PARAMETERS					
Quiescent Supply Current			1.5	3	mA
IN UVLO Threshold	Hysteresis = 300mV	7.5	8.4	9.0	V
POK Undervoltage Threshold	Measured at OUT, rising edge, hysteresis = 300mV	9.2	9.6	10.0	V
POK Delay	V_{POK} rising	100	220	350	µs
POK Output Voltage	V_{OUT} < 9.2V, I_{POK} = 1.6mA		0.1	0.25	V
POK Leakage Current	V_{OUT} > 10V, V_{POK} = 14V		0.1	1	µA
EN Rising Threshold	Hysteresis = 120mV	1.3	1.65	2.0	V
EN Pullup Voltage	EN unconnected	4.5	5.5		V
EN Pullup Current		12	20	28	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, V_{EN} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LPEN Rising Threshold	Hysteresis = 120mV	1.3	1.65	2.0	V
LPEN Pullup Voltage	LPEN unconnected	4.5	5.5		V
LPEN Pullup Current		12	20	28	µA
OVP Threshold Voltage	Hysteresis = 10mV, V_{OVP} rising	1.96	2.00	2.04	V
OVP Fault Timeout			1.5		ms
CTIM PARAMETERS					
CTIM Charging Current	V_{CTIM} < 1.5V	16	20	24	µA
CTIM Fault Pullup Current	V_{CTIM} = 6V	6	8	12	mA
Current-Limit Timeout Threshold Voltage		1.5	1.8	2.1	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{EN} = 0, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VB BULK SUPPLY CONTROL					
IN Supply Voltage Range		10		14	V
ISET Current Source	Current regulation threshold = I_{SET} x R_{ISET}	18		22	µA
Current-Limit Offset Voltage	V_{ISET} - V_{IN}	-4		+4	mV
OUT Input Current	V_{OUT} = 12V			12	µA
25W OUT Current Regulation	R_{ISET} = 3.09kΩ ±1%, R_{SENSE} = 20mΩ ±1%	2.5		3.7	A
50W OUT Current Regulation	R_{ISET} = 3.09kΩ ±1%, R_{SENSE} = 10mΩ ±1%	5.0		7.4	A
GATE PARAMETERS					
Gate Turn-On Current		8		12	µA
Gate High Voltage		V_{IN} + 4			V
IN PARAMETERS					
Quiescent Supply Current				3	mA
IN UVLO Threshold	Hysteresis = 300mV	7.5		9.0	V
POK Undervoltage Threshold	Measured at OUT, rising edge, hysteresis = 300mV	9.0		10.2	V
POK Delay	V_{POK} rising	100		350	µs
POK Output Voltage	V_{OUT} < 9.2V, I_{POK} = 1.6mA			0.25	V
POK Leakage Current	V_{OUT} > 10V, V_{POK} = 14V			1	µA
EN Rising Threshold	Hysteresis = 120mV	1.3		2.0	V
EN Pullup Voltage	EN unconnected	4.5			V
EN Pullup Current		12		28	µA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, V_{EN} = 0, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

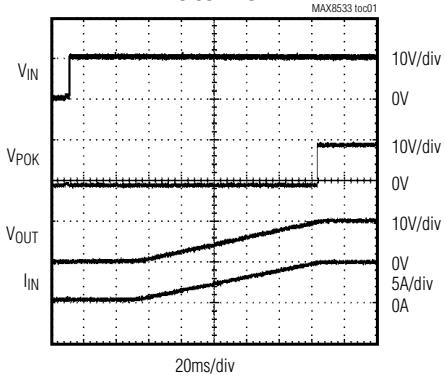
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LPEN Rising Threshold	Hysteresis = 120mV	1.3		2.0	V
LPEN Pullup Voltage	LPEN unconnected	4.5			V
LPEN Pullup Current		12		28	µA
OVP Threshold Voltage	Hysteresis = 10mV, V_{OVP} rising	1.96		2.04	V
CTIM PARAMETERS					
CTIM Charging Current	V_{CTIM} < 1.5V	15		25	µA
CTIM Fault Pullup Current	V_{CTIM} = 6V	6		12	mA
Current-Limit Timeout Threshold Voltage		1.4		2.2	V

Note 1: The current regulation threshold is set by R3 (Figure 2). It is equal to 20µA x R3.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

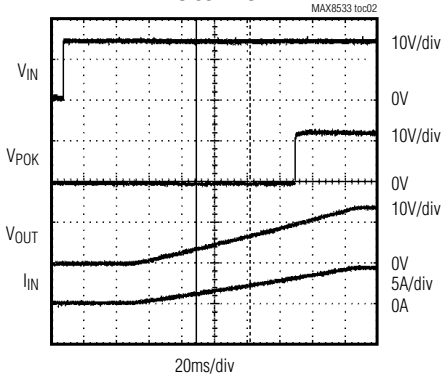
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

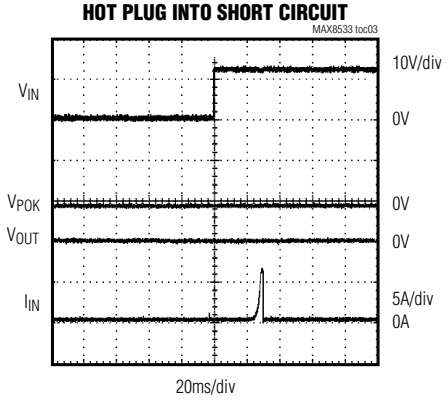
HOT PLUG WITH 10V INPUT INTO 50W LOAD



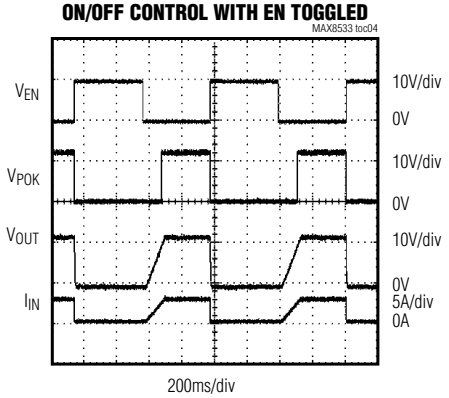
HOT PLUG WITH 14V INPUT INTO 65W LOAD



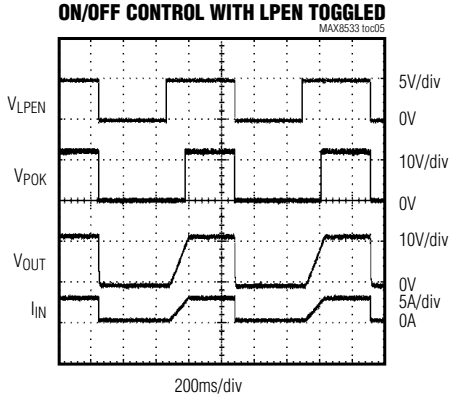
HOT PLUG INTO SHORT CIRCUIT



ON/OFF CONTROL WITH EN TOGGLED



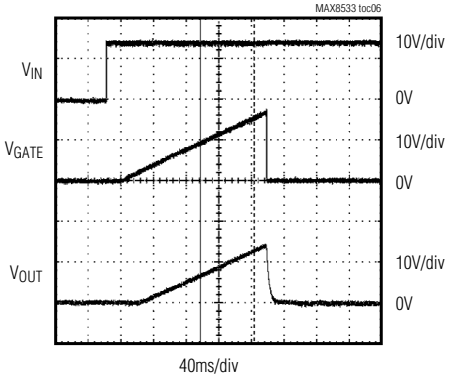
ON/OFF CONTROL WITH LPEN TOGGLED



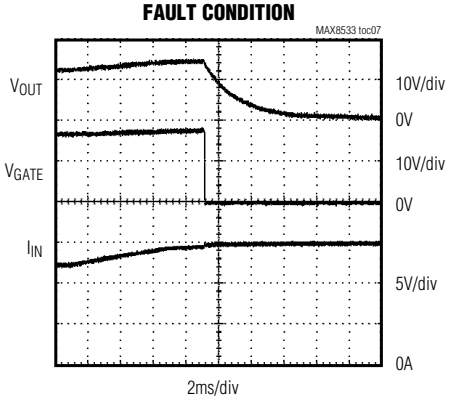
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

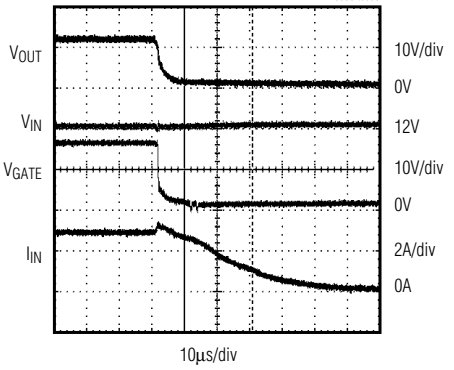
HOT PLUG INTO INPUT OVERVOLTAGE CONDITION



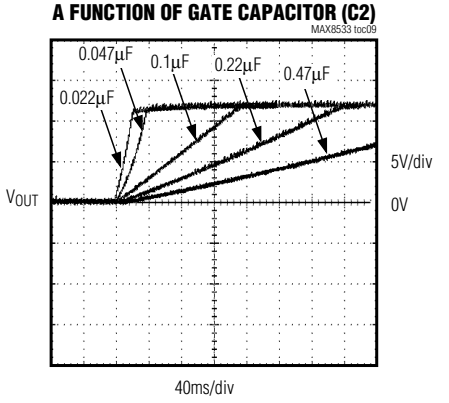
INPUT OVERVOLTAGE PROTECTION FAULT CONDITION



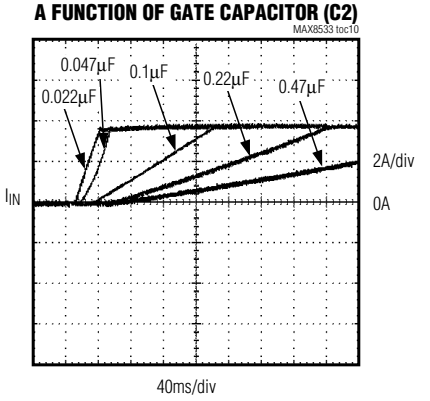
SHORT-CIRCUIT CURRENT PROTECTION



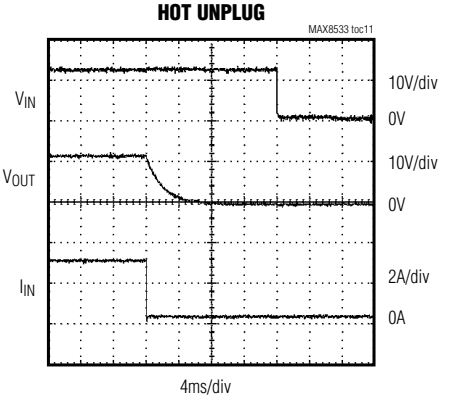
OUTPUT-VOLTAGE RISE TIME AS A FUNCTION OF GATE CAPACITOR (C2)



INPUT-CURRENT RISE TIME AS A FUNCTION OF GATE CAPACITOR (C2)



HOT UNPLUG



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Pin Description

PIN	NAME	FUNCTION
1	ISET	Current-Limit Threshold Programming Input. Connect to the low side of the current-limit threshold programming resistor.
2	IN	Bulk Power Supply. Connect to the input power supply and positive terminal of the current-sense resistor.
3	GATE	External MOSFET-Gate-Drive Output. Connect to the gate of the external N-channel MOSFET. A series resistor and capacitor connected from GATE to RET sets the turn-on ramp rate. At turn-on, this capacitor is charged to V_{IN} + 5V (typ) by an internal current source. GATE is pulled to RET when EN is high and/or LPEN is low. GATE is pulled to RET during a fault condition.
4	CTIM	Current Regulation Time Programming Input. Connect a capacitor from CTIM to RET. The capacitance at CTIM determines the time delay between an overcurrent event and chip output shutdown (current-limit timeout). CTIM is pulled low, resetting the fault latch when either EN is high or LPEN is low.
5	RET	Bulk Power Ground
6	OVP	Overvoltage Protection Input. Connect to common point of a resistor-divider from OUT to RET. GATE pulls low when V_{OVP} exceeds the 2V threshold for at least 1.5ms and the IC is latched off.
7	OUT	Output Voltage. Connect to the output of the circuit.
8	POK	Power-Good Output. POK is an open-drain output that becomes high impedance when V_{OUT} reaches 9.6V. Pull POK up to the supply rail using an external pullup resistor. POK is pulled to RET until the MAX8533 is enabled.
9	LPEN	Local Power-Enable Input. LPEN is a positive-assertion enable input to turn on the IC. Pull LPEN low to disable the output. LPEN has an internal pullup to 5V.
10	EN	Chip-Enable Input. EN is an active-low input that enables the IC.

Detailed Description

The MAX8533 is a single-port, 12V, IB-compliant versatile hot-swap controller IC designed for applications where a line card is inserted into a live backplane. The MAX8533 can be implemented in both IB Class I (non-isolated) and Class II (isolated) power-topology applications. Normally, when a line card is plugged into a live backplane, the low impedance of the card's discharged filter capacitors can momentarily collapse the input supply voltage. The MAX8533 is designed to reside on the line card and to provide inrush current-limiting and short-circuit protection. This is achieved using an external N-channel MOSFET, current-sense resistor, and current-limit set resistor, along with two on-chip comparators (Figure 1).

UVLO and Startup

The MAX8533 has an undervoltage lockout protection circuit. The circuit is disabled when V_{IN} is below 8.4V (typ). The gate of the MOSFET, CTIM, LPEN, and POK is pulled to RET until V_{IN} exceeds the UVLO threshold.

Once V_{IN} exceeds the UVLO threshold and LPEN and EN are enabled, the capacitor on the gate of the external MOSFET is charged and the MOSFET turns on. The charging of this capacitor provides soft-start to prevent high inrush currents.

On/Off Control

The MAX8533 is enabled/disabled using LPEN and EN. Drive EN low and LPEN high to enable the device. LPEN can also be left unconnected as it is internally connected to 5V. Drive LPEN low or EN high to disable the output. Table 1 is the truth table for these inputs.

Table 1. Truth Table

EN	LPEN	OUTPUT
0	0	OFF
0	1	ON
1	0	OFF
1	1	OFF

Zero is a logic-low input, 1 is a logic-high input or unconnected input.

Startup Into Load

The MAX8533 is intended to be used in a circuit where no load is applied until the POK signal is enabled. In an application where the load is applied during the output-voltage ramp up, the $R_{DS(ON)}$ of the MOSFET is higher and the power dissipated by the MOSFET is larger. Repeated, rapid hot-swaps into a load can create sufficient heat to exceed the power-dissipation limits of the package causing failure of the MOSFET.

Applications Information

Setting the Turn-On Ramp Rate

The MOSFET turn-on ramp rate is determined by the capacitor (C2) at GATE (Figure 2). An internal 10µA current source charges C2 to bring GATE high. The soft-start rate is determined as follows:

$$t_{SS} = C2 \times (V_{IN} + 5)/(10 \times 10^{-6})$$

t_{SS} may be longer than expected in the application depending on the gate capacitance of the external MOSFET. The necessary gate voltage is provided by an on-board charge pump that boosts the voltage at GATE to (V_{IN} + 5V).

External Power MOSFET Selection

Select the N-channel MOSFET according to the application's current requirements. Table 2 lists some recommended components. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimal voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ can cause high output ripple if the board has pulsing loads, or trigger an external

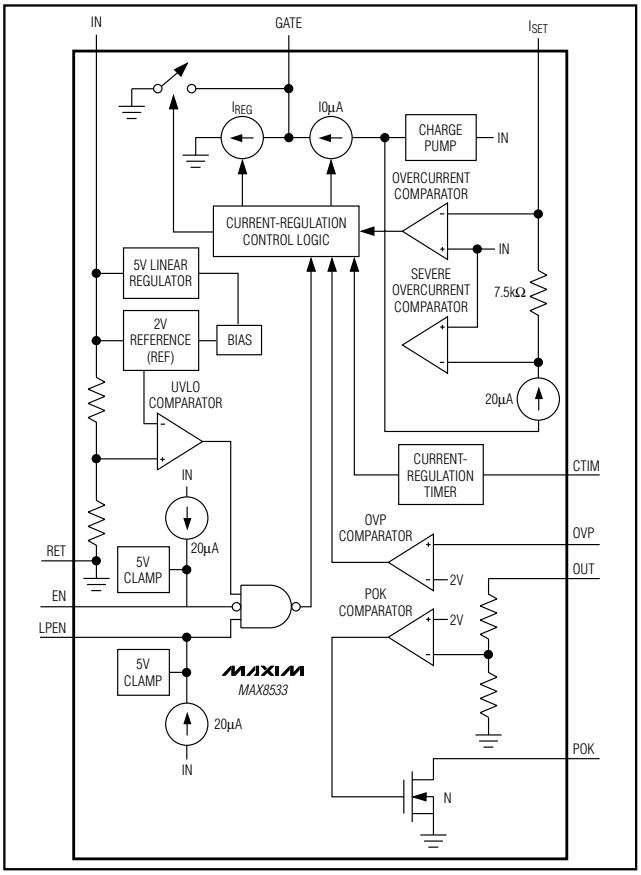


Figure 1. MAX8533 Functional Diagram

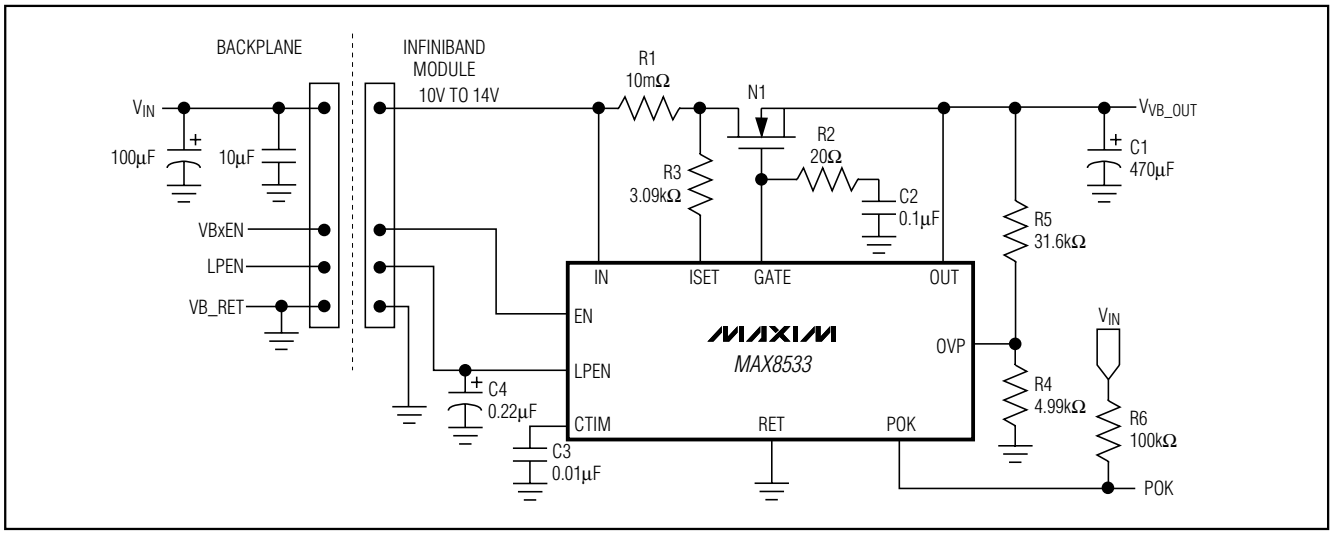


Figure 2. Typical 50W Applications Circuit

Smallest, Most Reliable, 12V, Infiniband-Compliant Hot-Swap Controller

Table 2. External Component List for 50W Output

REF DESIGNATOR	DESCRIPTION	MANUFACTURER PART NO.
C1	470µF, 25V aluminum electrolytic capacitor	Sanyo 25MV470HC
C2	0.1µF ±10%, 25V X5R ceramic capacitor	Taiyo Yuden TMK107BJ104KA
C3	0.01µF ±20% X7R ceramic capacitor	Kemet C0606C103M4RAC
C4	0.22µF ±10%, 25V X5R ceramic capacitor	TDK C1608X5R1A224K
R1*	10mΩ ±1%, 0.5W current-sense resistor	Dale LRF1206-01-R010-F
R2	20Ω ±5% resistor	Panasonic
R3	3.09kΩ ±1% resistor	Panasonic
R4	4.99kΩ ±1% resistor	Panasonic
R5	31.6kΩ ±1% resistor	Panasonic
N1	N-channel MOSFET, 30V, 6mΩ	Siliconix Si4842DY

**Use a 20mΩ ±1%, 0.25W current-sense resistor for 25W applications.*

undervoltage reset monitor at full load. The maximum gate voltage (V_{GS}) rating must be at least ±20V. Low MOSFET gate capacitance is not necessary for the inrush current limiting because it is achieved by limiting the GATE dV/dt. However, higher gate capacitance increases the turn-off time of the MOSFET under fault conditions.

Current-Limit and Overload Protection

The MAX8533 features a dual overcurrent protection circuit that turns off the MOSFET in overcurrent situations. When an overload event is sensed, the IC limits the current to a level set by ISET. Continuous overload for a period set by the user (t_{CTIM}) latches off the MOSFET. The severe overcurrent protection immediately shuts down the external MOSFET and latches it off.

R3 sets the current-limit threshold voltage. This voltage is generated from an internal 20µA source driven through R3. Therefore:

$$V_{ILIM} = R3 \times 20\mu A$$

The current-sense signal is sensed across resistor R1. With no load, the voltage at ISET is the input voltage plus V_{ILIM}. As the load current increases, the voltage drop across R1 increases and reduces the voltage at ISET. Once V_{ISET} is lower than V_{IN}, the overcurrent comparator (Figure 1) is tripped and the MAX8533 enters current regulation mode. During current regulation mode, the gate voltage of the MOSFET is decreased to limit the current to the output. The maximum time period for the current regulation mode is set by the external capacitor at CTIM (C3). This feature allows transient currents that exceed the current limit to pass without shutting down the circuit. The current regulation time period is determined as:

$$t_{IREG} = C3 \times (1.8V/20\mu A)$$

If t_{IREG} expires and the overcurrent condition still exists, the MOSFET is latched off.

The severe overcurrent comparator (Figure 1) trips if the drop across the current-sense resistor (R1) is 150mV higher than the current-limit threshold (V_{IN} exceeds V_{ISET} by 150mV). During a severe overcurrent event, the gate of the external MOSFET is pulled down with a 350mA current source and latched immediately.

Toggle EN, LPEN, or input power to clear the latched fault condition.

Overvoltage Protection

The MAX8533 has an adjustable overvoltage protection feature that latches the IC off in case of an overvoltage event. An external resistor-divider (R4 and R5, Figure 2) from OUT to RET with OVP connected to the center, sets the overvoltage threshold. Use 4.99kΩ for R4. R5 is determined using the following equation:

$$R5 = 4.99 \times 10^3 \times ((V_{OVT} / V_{OVP}) - 1)$$

V_{OVT} is the desired overvoltage threshold and V_{OVP} is 2V (typ). OVP latches off the MAX8533 if an overvoltage condition exists for 1.5ms. Toggle EN, LPEN, or input power to clear the latched fault condition.

Fault Reset

Overcurrent, severe overcurrent, and overvoltage conditions result in the MAX8533 entering a latched fault condition. Toggle LPEN, EN, or input power to reset the latched fault condition and return to normal operation.

Power-Good Output (POK)

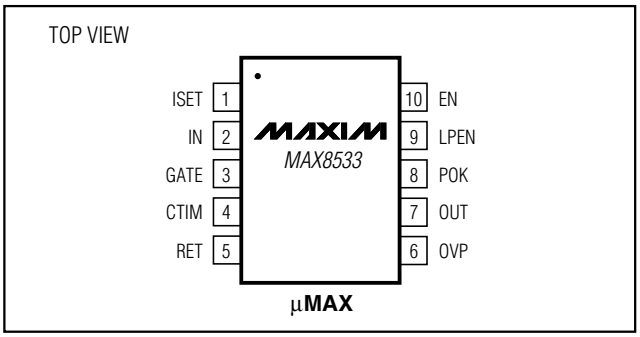
POK is an open-drain output used to enable the on-board DC-to-DC converter. The POK output turns high impedance when the output rail reaches 9.6V. POK must be pulled up to the user's logic level using a pullup resistor.

PC Board Layout Guidelines

To take advantage of the switch response time to an output fault condition, keep all traces as short as possible and maximize the high-current trace width to reduce the effect of undesirable parasitic inductance. The MOSFET dissipates a fair amount of heat due to the high currents involved, especially during an overcurrent condition. In order to dissipate the heat generated by the MOSFET, make the power traces very wide with a large amount of copper area. A more efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board.

Minimize the current-sense resistor trace length (<10mm), and ensure accurate current sensing with Kelvin connections. Place capacitor CTIM as close as possible to the IC. The traces from the current-sense resistor to IN and ISET should be as short as possible for accurate current sensing. Place the MAX8533 circuit as close as possible to the backplane connector. A sample PC board layout is available in the MAX8533 Evaluation Kit.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 2541

PROCESS: BiCMOS

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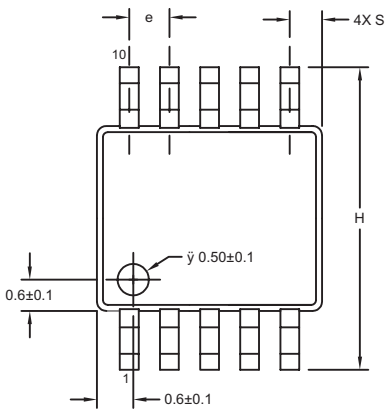
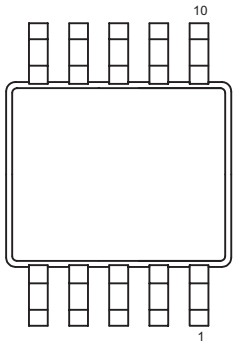
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

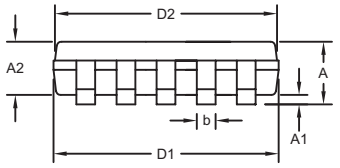


TOP VIEW

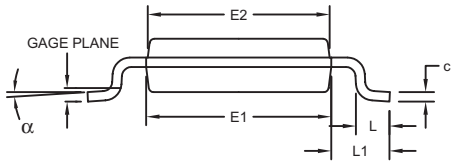


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1