

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)

V_{CC}-0.3V to 6.0V

All Other Inputs (Note 1)-0.3V to ($V_{CC} + 0.3$ V)

Input Current

V_{CC}20mA

GND20mA

Output Current (all outputs).....20mA

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

Plastic DIP (derate 9.09mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....727mW

SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....471mW

μ MAX (derate 4.10mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)330mW

CERDIP (derate 8.00mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....640mW

Operating Temperature Ranges

MAX70_C_, MAX813LC_ 0°C to $+70^\circ\text{C}$

MAX70_E_, MAX813LE_ -40°C to $+85^\circ\text{C}$

MAX70_MJA..... -55°C to $+125^\circ\text{C}$

Storage Temperature Range..... -65°C to $+160^\circ\text{C}$

Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

Soldering Temperature (reflow)

Lead(Pb)-free..... $+260^\circ\text{C}$

Containing Lead(Pb)..... $+240^\circ\text{C}$

Note 1: The input-voltage limits on PFI and $\overline{\text{MR}}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{CC} = 4.75\text{V}$ to 5.5V for MAX705/MAX707/MAX813L, $V_{CC} = 4.5\text{V}$ to 5.5V for MAX706/MAX708, $T_A = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range	V _{CC}	MAX70_C	1.0		5.5	V	
		MAX813LC	1.1		5.5		
		MAX70_E/M, MAX813LE/M	1.2		5.5		
Supply Current	I _{SUPPLY}	MAX705C, MAX706C, MAX813LC		150	350	μA	
		MAX705E/M, MAX706E/M, MAX813LE/M		150	500		
		MAX707C, MAX708C		50	350		
		MAX707E/M, MAX708E/M		50	500		
Reset Threshold (Note 2)	V _{RT}	MAX705, MAX707, MAX813L	4.50	4.65	4.75	V	
		MAX706, MAX708	4.25	4.40	4.50		
Reset Threshold Hysteresis (Note 2)				40		mV	
Reset Pulse Width (Note 2)	t _{RS}		140	200	280	ms	
$\overline{\text{RESET}}$ Output Voltage		I _{SOURCE} = 800μA	V _{CC} - 1.5			V	
		I _{SINK} = 3.2mA	0.4				
		MAX70_C, V _{CC} = 1V, I _{SINK} = 50μA	0.3				
		MAX70_E/M, V _{CC} = 1.2V, I _{SINK} = 100μA	0.3				
RESET Output Voltage		MAX707, MAX708, I _{SOURCE} = 800μA		V _{CC} - 1.5		V	
		MAX707, MAX708, I _{SINK} = 1.2mA		0.4			
		MAX813LC, I _{SOURCE} = 4μA, V _{CC} = 1.1V		0.8			
		MAX813LE/M, I _{SOURCE} = 4μA, V _{CC} = 1.2V		0.9			
		MAX813L	I _{SOURCE} = 800μA		V _{CC} - 1.5		
			I _{SINK} = 3.2mA		0.4		

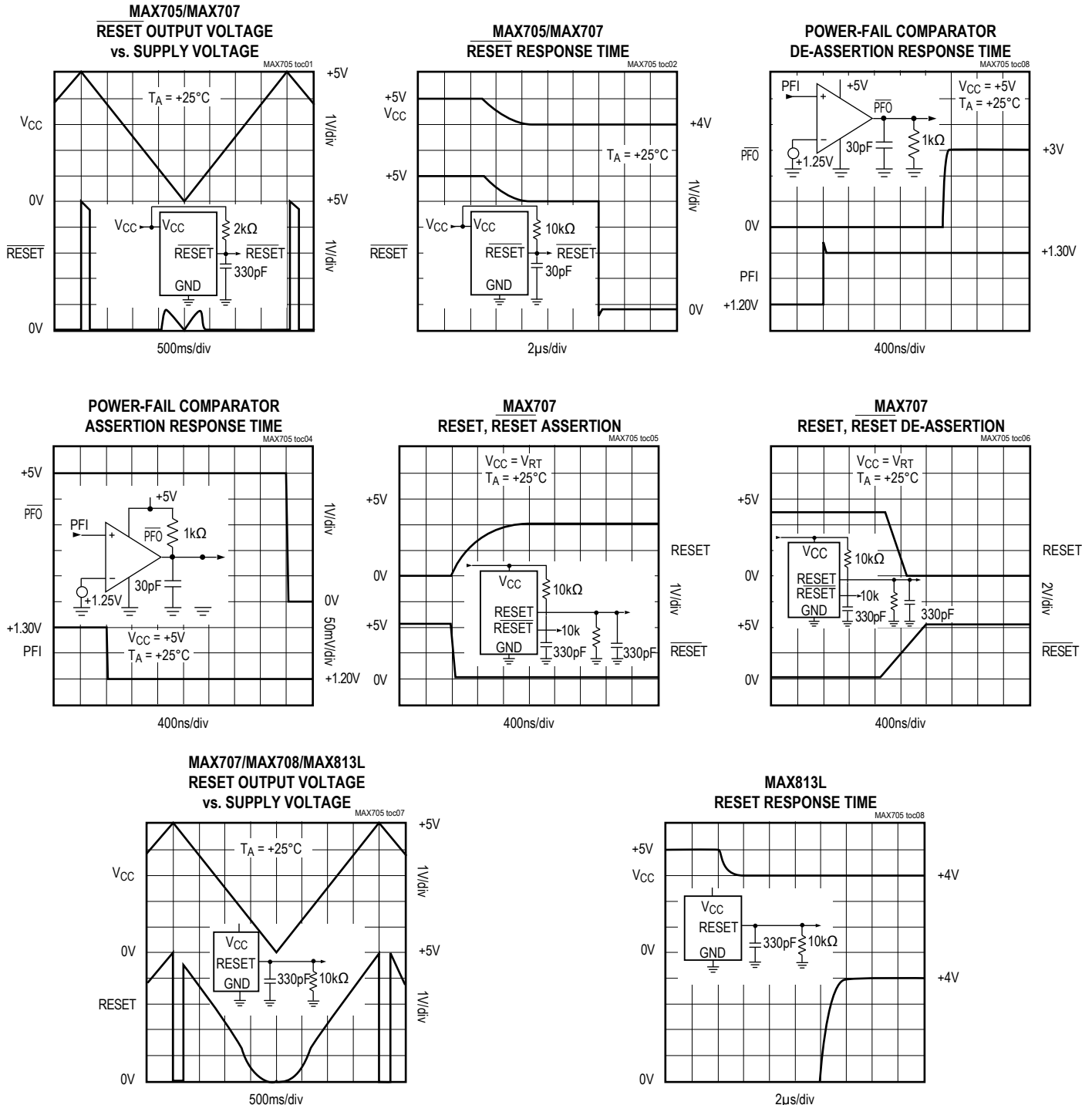
Electrical Characteristics (continued)

(V_{CC} = 4.75V to 5.5V for MAX705/MAX707/MAX813L, V_{CC} = 4.5V to 5.5V for MAX706/MAX708, T_A = T_{MIN} to T_{MAX} , unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Watchdog Timeout Period		t _{WD}	MAX705, MAX706, MAX813L	1.00	1.60	2.25	s
WDI Pulse Width		t _{WP}	V _{IL} = 0.4V, V _{IH} = (V _{CC}) (0.8)	50			ns
WDI Input Threshold	Low		MAX705, MAX706, MAX813L, V _{CC} = 5V	0.8			V
	High			3.5			
WDI Input Current			MAX705, MAX706, MAX813L, V _{CC} = 5V	50	150	μA	
			MAX705, MAX706, MAX813L, WDI = 0V	-150	-50		
$\overline{WDO}$ Output Voltage			MAX705, MAX706, MAX813L, I _{SOURCE} = 800μA	V _{CC} - 1.5		V	
			MAX705, MAX706, MAX813L, I _{SINK} = 1.2mA	0.4			
$\overline{MR}$ Pull-Up Current			$\overline{MR}$ = 0V	100	250	600	μA
$\overline{MR}$ Pulse Width		t _{MR}		150			ns
$\overline{MR}$ Input Threshold	Low			0.8			V
	High			2.0			
$\overline{MR}$ to Reset Out Delay (Note 2)		t _{MD}		250			ns
PFI Input Threshold			V _{CC} = 5V	1.20	1.25	1.30	V
PFI Input Current				-25.00	+0.01	+25.00	nA
$\overline{PFO}$ Output Voltage			I _{SOURCE} = 800μA	V _{CC} - 1.5		V	
			I _{SINK} = 3.2mA	0.4			

Note 2: Applies to both $\overline{RESET}$ in the MAX705–MAX708 and $RESET$ in the MAX707/MAX708/MAX813L.

Typical Operating Characteristics



Pin Description

PIN						NAME	FUNCTION
MAX705/MAX706		MAX707/MAX708		MAX813L			
DIP/SO	μMAX	DIP/SO	μMAX	DIP/SO	μMAX		
1	3	1	3	1	3	MR	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250μA pullup current. It can be driven from a TTL or CMOS logic line, as well as shorted to ground with a switch.
2	4	2	4	2	4	VCC	+5V Supply Input
3	5	3	5	3	5	GND	0V Ground Reference for all signals
4	6	4	6	4	6	PFI	Power-Fail Voltage-Monitor Input. When PFI is less than 1.25V, PFO goes low. Connect PFI to GND or VCC when not used.
5	7	5	7	5	7	PFO	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise PFO stays high.
6	8	—	—	6	8	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (Figure 1). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three stated, or WDI sees a rising or falling edge.
—	—	6	—	—	—	N.C.	No Connect
7	1	7	1	—	—	RESET	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever VCC is below the reset threshold (4.65V in the MAX705 and 4.40V in the MAX706). It remains low for 200ms after VCC rises above the reset threshold or MR goes from low to high (Figure 3). A watchdog timeout will not trigger RESET unless WDO is connected to MR.
8	2	—	—	8	2	WDO	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. WDO also goes low during low-line conditions. Whenever VCC is below the reset threshold, WDO stays low; however, unlike RESET, WDO does not have a minimum pulse width. As soon as VCC rises above the reset threshold, WDO goes high with no delay.
—	—	8	2	7	1	RESET	Active-High RESET Output is the inverse of RESET. Whenever RESET is high, RESET is low, and vice versa (Figure 2). The MAX813L has a RESET output only.

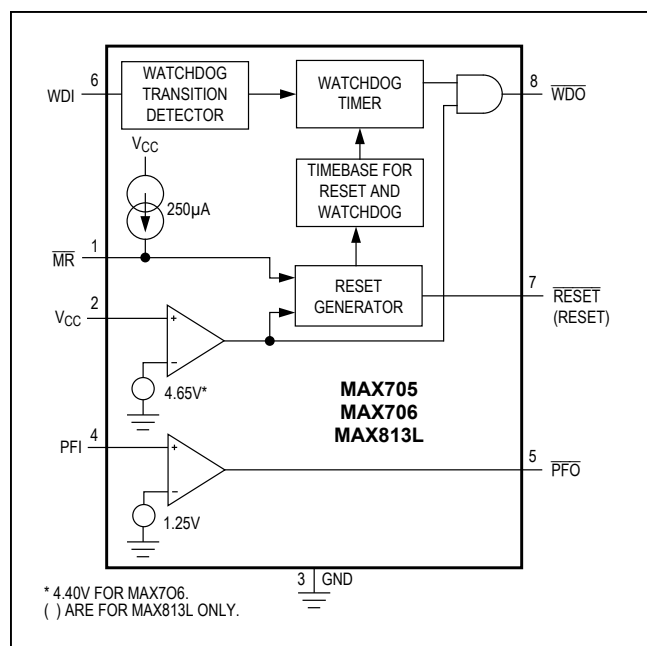


Figure 1. MAX705/MAX706/MAX813L Block Diagram

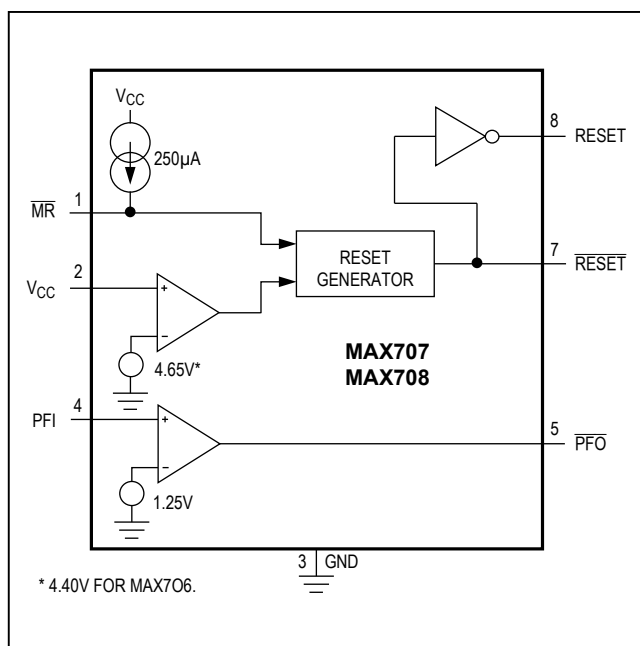


Figure 2. MAX707/MAX708 Block Diagram

Detailed Description

Reset Output

A microprocessor's (μ P's) reset input starts the μ P in a known state. Whenever the μ P is in an unknown state, it should be held in reset. The MAX705–MAX708/MAX813L assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after about 200ms. $\overline{RESET}$ pulses low whenever V_{CC} dips below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The MAX707/MAX708/MAX813L active-high $RESET$ output is simply the complement of the $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.1V. Some μ Ps, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The MAX705/MAX706/MAX813L watchdog circuit monitors the μ P's activity. If the μ P does not toggle the watchdog input (WDI) within 1.6sec and WDI is not three

stated, $\overline{WDO}$ goes low. As long as $\overline{RESET}$ is asserted or the WDI input is three stated, the watchdog timer stays cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer starts counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ is not connected to the nonmaskable interrupt input (NMI) of a μ P. When V_{CC} drops below the reset threshold, $\overline{WDO}$ goes low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI interrupt.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

The MAX705/MAX706 have a watchdog timer and a $\overline{RESET}$ output. The MAX707/MAX708 have both active-high and active-low reset outputs. The MAX813L has both an active-high reset output and a watchdog timer.

Manual Reset

The manual-reset input ($\overline{MR}$) allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS-logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in the MAX705/ MAX706/ MAX813L. Simply connect $\overline{WDO}$ to $\overline{MR}$.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

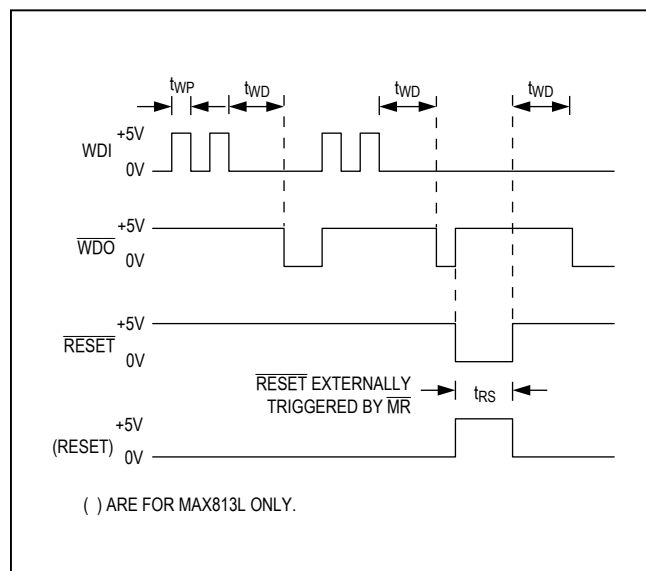


Figure 3. MAX705/MAX706/MAX813L Watchdog Timing

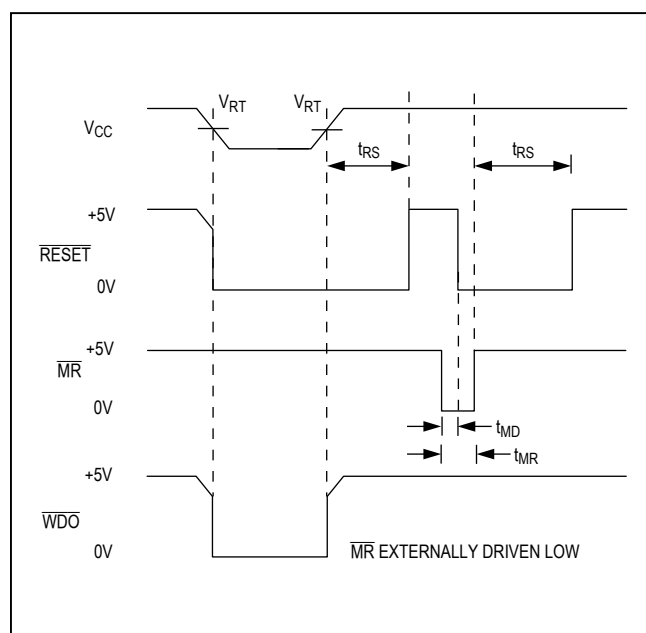


Figure 4. MAX705/MAX706 $\overline{\text{RESET}}$, MR, and $\overline{\text{WDO}}$ Timing with WDI Three Stated. The MAX707/MAX708/MAX813L $\overline{\text{RESET}}$ output is the inverse of $\overline{\text{RESET}}$ shown.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see *Typical Operating Circuit*). Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use $\overline{\text{PFO}}$ to interrupt the μ P so it can prepare for an orderly power-down.

Applications Information

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to $V_{CC} = 0V$

When V_{CC} falls below 1V, the MAX705–MAX708 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pulldown resistor is added to the $\overline{\text{RESET}}$ pin, as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding $\overline{\text{RESET}}$ low. Resistor value (R1) is not critical. It should be about 100k Ω , large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage-divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{\text{PFO}}$. A capacitor between PFI and GND reduces the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{\text{RESET}}$ can be asserted on other voltages in addition to the +5V V_{CC} line. Connect $\overline{\text{PFO}}$ to MR to initiate a $\overline{\text{RESET}}$ pulse when PFI drops below 1.25V. Figure 6 shows the MAX705–MAX708 configured to assert $\overline{\text{RESET}}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{\text{PFO}}$ is high. By adding the resistors and transistor as shown, a high $\overline{\text{PFO}}$ triggers a reset. As long as $\overline{\text{PFO}}$ remains high, the MAX705–MAX708/MAX813L keep reset asserted ($\overline{\text{RESET}}$ = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

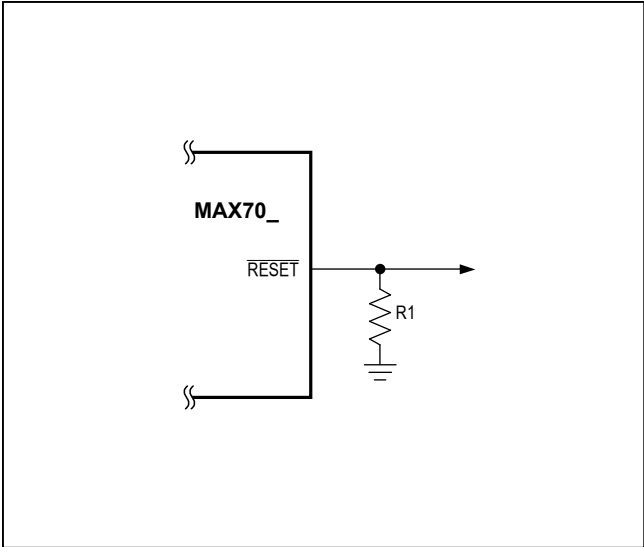


Figure 5. RESET Valid to Ground Circuit

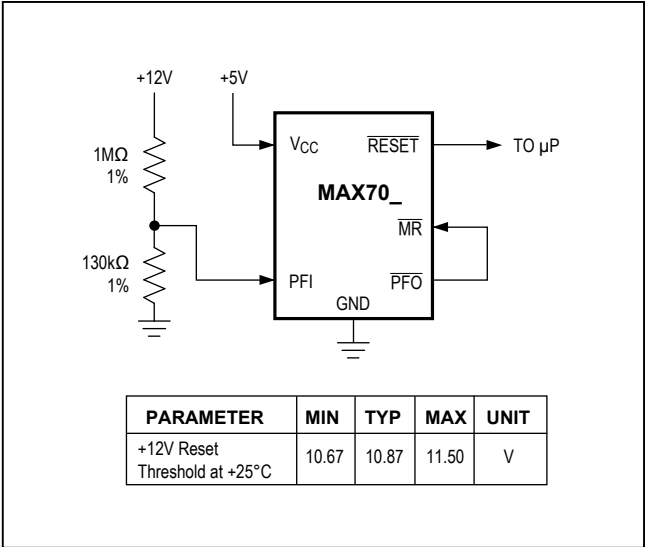


Figure 6. Monitoring Both +5V and +12V

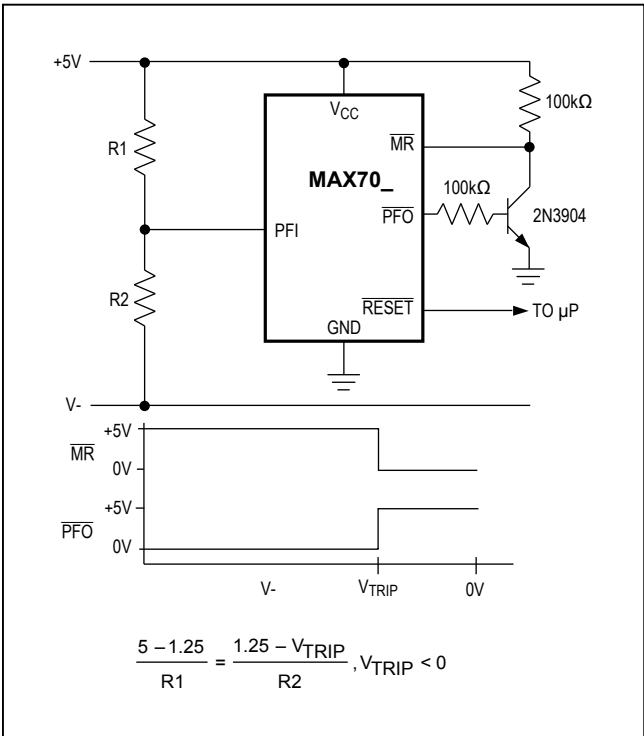


Figure 7. Monitoring a Negative Voltage

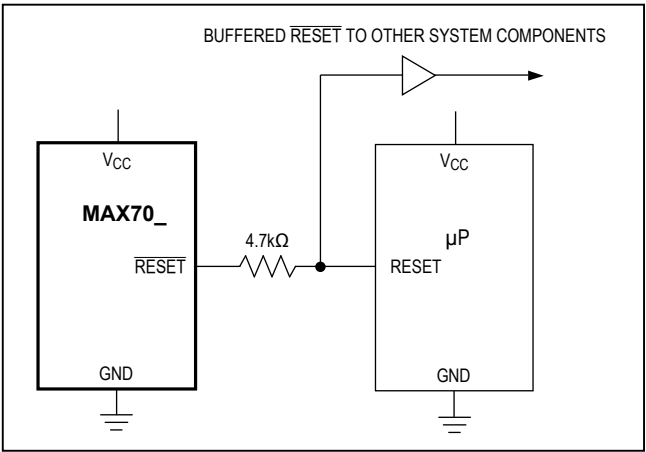


Figure 8. Interfacing to μ Ps with Bidirectional Reset Pins

Interfacing to μ Ps with Bidirectional Reset Pins

μ Ps with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX705–MAX708 RESET output. If, for example, the RESET output is driven high and the μ P wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7k Ω resistor between the RESET output and the μ P reset I/O, as in Figure 8. Buffer the RESET output to other system components.

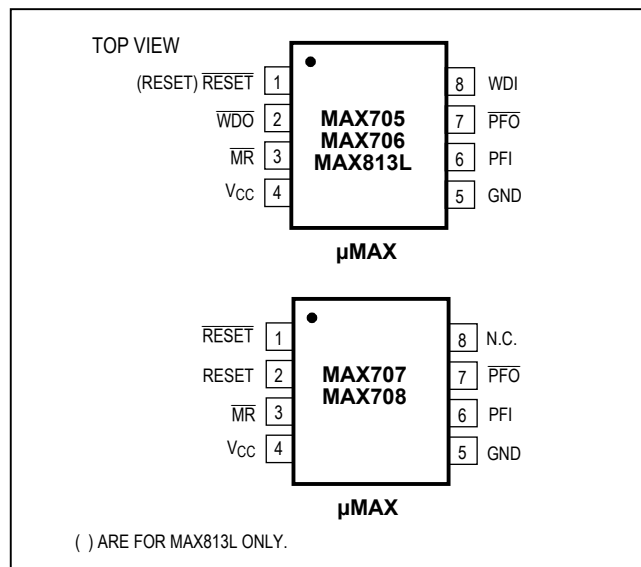
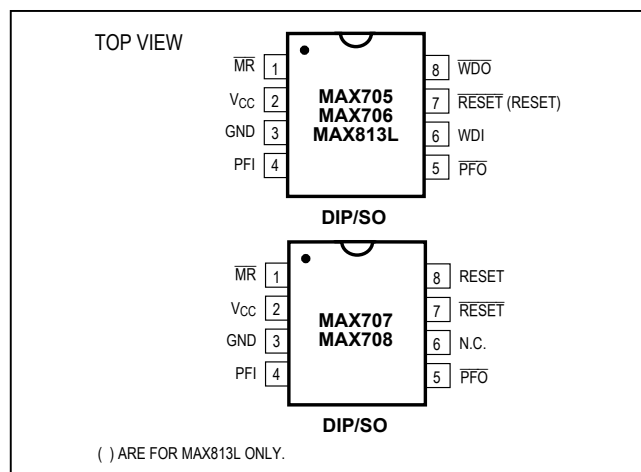
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX705EPA	-40°C to +85°C	8 Plastic DIP
MAX705ESA	-40°C to +85°C	8 SO
MAX705EUA	-40°C to +85°C	8 μ MAX
MAX705MJA	-55°C to +125°C	8 Cerdip**
MAX706CPA	0°C to +70°C	8 Plastic DIP
MAX706CSA	0°C to +70°C	8 SO
MAX706CUA	0°C to +70°C	8 μ MAX
MAX706C/D	0°C to +70°C	Dice*
MAX706EPA	-40°C to +85°C	8 Plastic DIP
MAX706ESA	-40°C to +85°C	8 SO
MAX706EUA	-40°C to +85°C	8 μ MAX
MAX706MJA	-55°C to +125°C	8 Cerdip**
MAX707CPA	0°C to +70°C	8 Plastic DIP
MAX707CSA	0°C to +70°C	8 SO
MAX707CUA	0°C to +70°C	8 μ MAX
MAX707C/D	0°C to +70°C	Dice*
MAX707EPA	-40°C to +85°C	8 Plastic DIP
MAX707ESA	-40°C to +85°C	8 SO
MAX707EUA	-40°C to +85°C	8 μ MAX
MAX707MJA	-55°C to +125°C	8 Cerdip**
MAX708CPA	0°C to +70°C	8 Plastic DIP
MAX708CSA	0°C to +70°C	8 SO
MAX708CUA	0°C to +70°C	8 μ MAX
MAX708C/D	0°C to +70°C	Dice*
MAX708EPA	-40°C to +85°C	8 Plastic DIP
MAX708ESA	-40°C to +85°C	8 SO
MAX708EUA	-40°C to +85°C	8 μ MAX
MAX708MJA	-55°C to +125°C	8 Cerdip**
MAX813LCPA	0°C to +70°C	8 Plastic DIP
MAX813LCSA	0°C to +70°C	8 SO
MAX813LCUA	0°C to +70°C	8 μ MAX
MAX813LC/D	0°C to +70°C	Dice*
MAX813LEPA	-40°C to +85°C	8 Plastic DIP
MAX813LESA	-40°C to +85°C	8 SO
MAX813LEUA	-40°C to +85°C	8 μ MAX
MAX813LMJA	-55°C to +125°C	8 Cerdip**

*Dice are specified at $T_A = +25^\circ\text{C}$.

**Contact factory for availability and processing to MIL-STD-883. Devices in PDIP, SO and μ MAX packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead-free not available for Cerdip package.

Pin Configurations



MAX705–MAX708/MAX813L

MAX705–MAX708/MAX813L
Low-Cost, μ P Supervisory Circuits

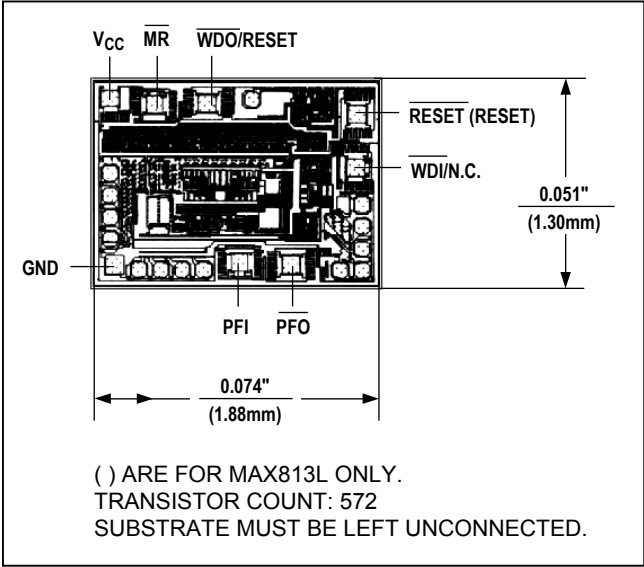
Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	<u>RESET</u> Valid to $V_{CC} = 1V$	Nominal Watchdog Timeout Period (sec), if Available	Separate Watchdog Output	Backup-Battery Switch	V_{CC} -to- V_{OUT} On Resistance Max (Ω)	BATT - to- V_{OUT} On Resistance Max (Ω)	<u>CE</u> Write Protect	Power-Fail Comparator	Manual-Reset Input	Low-Line Output	Battery-On Output	Supply Operating Mode mA max (typ)	Supply Backup Mode μA max (typ)	Pins	Price† 1000-up (\$)
MAX1232	4.37/4.62	250	✓	✓	✓	0.15/0.6/1.2		✓	10	400		✓	✓			0.2(0.05)		8	1.71
MAX690A/692A	4.65/4.40	140	✓		✓	1.6		✓	6	400		✓				0.35(0.2)	5(0.05)	8	3.26
MAX690R/S/T	2.63/2.93/3.08	140	✓		✓	1.6		✓	1.2	25	✓/10ns	✓			✓	0.1(0.035)	5(0.04)	16	3.61
MAX691A/693A	4.65/4.40	140/adj.	✓	✓	✓	1.6/adj.	✓	✓										16	††
MAX1691	The MAX1691 is a module with the MAX691A and a 125mAh lithium battery																		
MAX696	Adj.	35/adj.	✓	✓	✓	1.6/adj.	✓	✓				✓			✓			16	3.55
MAX697	Adj.	35/adj.	✓	✓	✓	1.6/adj.	✓	✓			✓	✓						16	3.58
MAX700	4.65/adj.	200	✓	✓									✓			0.2(0.1)		8	2.17
MAX703/704	4.65/4.40	140	✓		✓			✓	10	400		✓				0.35(0.2)	5(0.05)	8	1.38*
MAX704R/S/T	2.63/2.93/3.08	140	✓		✓	1.6	✓	✓	6	400		✓	✓			0.5(0.4)	1(0.4)	8	2.93
MAX705/706	4.65/4.40	140	✓		✓	1.6	✓	✓				✓	✓			0.35(0.2)		8	1.02*
MAX706P	2.63	140		✓	✓	1.6	✓	✓				✓	✓			0.35(0.2)		8	1.71
MAX706R/S/T	2.63/2.93/3.08	140	✓		✓							✓	✓			0.35(0.2)		8	1.71
MAX707/708	4.65/4.40	140	✓	✓	✓							✓	✓			0.35(0.2)		8	0.88*
MAX708R/S/T	2.63/2.93/3.08	140	✓	✓	✓							✓	✓			0.35(0.2)		8	1.63
MAX791	4.65	140	✓	✓	✓	1	✓	✓	1.2	25	✓/10ns	✓	✓	✓	✓	0.15(0.06)	5(0.04)	16	3.90
MAX802L/M/R/S/T	4.60/4.40/ 2.63/2.93/3.08	140	✓	✓	✓	1	✓	✓			✓/10ns	✓				0.15(0.07)		16	3.42
MAX793R/S/U/T	2.63/2.93/3.07/3.08	140	✓	✓	✓	1.6	✓	✓	TBD	TBD	✓	✓				TBD	TBD	16	††
MAX794	Adj.	140	✓	✓	✓	1.6	✓	✓	TBD	TBD	✓	✓				TBD	TBD	8	††
MAX795R/S/U/T	2.63/2.93/3.07/3.08	140	✓		✓			✓	TBD	TBD	✓					TBD	TBD	16	††
MAX800L/M	4.60/4.40	140	✓	✓	✓	1.6/adj.	✓	✓	1.2	25	✓/10ns	✓/±2%			✓	0.1(0.035)	5(0.04)	8	3.88
MAX801L/N/M	4.68/4.58/4.43	140	✓/±1.5%		✓	1.6		✓	TBD	TBD						TBD	TBD	8	††
MAX802L/M/R/S/T	4.60/4.40/ 2.63/2.93/3.08	140	✓		✓	1.6		✓	10	400		✓/±2%				0.35(0.2)	5(0.05)	8	3.59
MAX804R/S/T	2.63/2.93/3.08	140		✓	✓	1.6		✓	6	400		✓/±2%				0.5(0.4)	1(0.4)	8	3.66
MAX805L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✓	✓	1.6		✓	10	400		✓				0.35(0.2)	5(0.05)	8	3.26
MAX806R/S/T	2.63/2.93/3.08	140	✓	✓	✓			✓	6	400		✓/±2%	✓		✓	0.5(0.4)	1(0.4)	8	3.90
MAX807L/N/M	4.68/4.58/4.43	140	✓/±1.5%	✓/±1.5%	✓	1.6	✓	✓	TBD	TBD	✓	✓	✓	✓	✓	TBD	TBD	8	††
MAX808L/N/M	4.68/4.58/4.43	140	✓/±1.5%		✓			✓	TBD	TBD	✓			✓		TBD	TBD	16	††
MAX809L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✓		✓											0.06 (0.024)		3	††
MAX810L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✓	✓											0.06 (0.024)		3	††
MAX813L	4.65	140		✓	✓	1.6	✓					✓/±2%	✓			0.35(0.2)		8	1.02*
MAX814K/L/N/T	4.80/4.70/4.55/3.03	140	✓/±1%	✓/±1%	✓							✓/±2%	✓	✓		TBD	TBD	8	††
MAX815K/L/N/T	4.80/4.70/4.55/3.03	140	✓/±1%		✓	1.6	✓					✓/±2%	✓			TBD	TBD	8	††
MAX816	Adj/±1%	140	✓	✓	✓							✓/±2%	✓			TBD	TBD	8	††
MAX820L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✓	✓	✓	1	✓	✓			✓/10ns	✓/±2%	✓	✓		0.15 (0.07)		16	3.82
MAX1210	4.37/4.62							✓	2.5	667	✓					0.5 (0.23)	0.1(0.002)	8	2.44

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.
8 μ MAX	U8+1	21-0036
8 Plastic DIP	P8+1	21-0043
8 SO	S8+2	21-0041

Chip Topography



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/92	Initial release	—
8	3/10	Updated the <i>Features</i> , <i>Absolute Maximum Ratings</i> , <i>Typical Operating Characteristics</i> , Figures 3, 7, 8, and the <i>Package Information</i> sections	1, 2, 4, 7, 8, 10
9	1/13	Updated package code for 8 SO package	11
10	4/15	Deleted “Automotive Systems” from <i>Applications</i> and updated <i>Benefits and Features</i> sections	1
11	7/18	Updated <i>Pin Description</i> table	5

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