Absolute Maximum Ratings

V_{CC}, ENABLE, $\overline{ENABLE}$, IN .....-0.3V to +6V
OUT, $\overline{OUT}$ (push-pull).....-0.3V to (V_{CC} + 0.3V)
OUT, $\overline{OUT}$ (open-drain).....-0.3V to +30V
CDELAY .....-0.3V to (V_{CC} + 0.3V)
Output Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin µDFN (derate 2.1mW/°C above +70°C) 167.7mW
6-Pin Thin SOT23 (derate 9.1mW/°C above +70°C)....727.3mW

Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

µDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....477°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....122C/W

Thin SOT23
Junction-to-Ambient Thermal Resistance (θ_{JA}).....110°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....50°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four layer board. For detailed information on package thermal considerations refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 1.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Operating Voltage Range	V_{CC}		1.5		5.5	V
Undervoltage Lockout (Note 3)	UVLO	V_{CC} falling	1.20		1.35	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 3.3V, no load		10	20	µA
IN						
Threshold Voltage	V_{TH}	V_{IN} rising, 1.5V < V_{CC} < 5.5V	0.491	0.5	0.509	V
Hysteresis	V_{HYST}	V_{IN} falling		5		mV
Input Current (Note 4)	I_{IN}	V_{IN} = 0V or V_{CC}	-15		+15	nA
CDELAY						
Delay Charge Current	I_{CD}		200	250	300	nA
Delay Threshold	V_{TCD}	CDELAY rising	0.95	1.00	1.05	V
CDELAY Pulldown Resistance	R_{CDELAY}			130	500	Ω
ENABLE/$\overline{ENABLE}$						
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.4			V
Input Leakage Current	I_{LEAK}	ENABLE, $\overline{ENABLE}$ = V_{CC} or GND	-100		+100	nA

Electrical Characteristics (continued)

(V_{CC} = 1.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

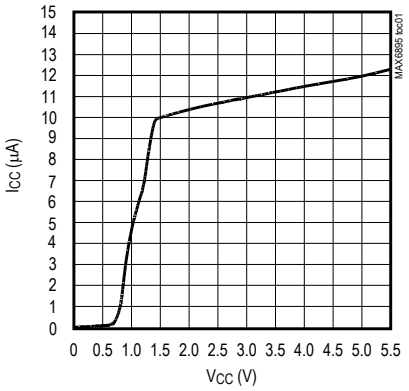
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT/OUT							
Output Low Voltage (Open-Drain or Push-Pull)	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90µA, MAX6895/MAX6897/MAX6899 only				0.3	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA				0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 1mA				0.4	
Output High Voltage (Push-Pull)	V_{OH}	V_{CC} ≥ 2.25V, I_{SOURCE} = 500µA		0.8 x V_{CC}			V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA		0.8 x V_{CC}			
Output Open-Drain Leakage Current	I_{LKG}	Output high impedance, V_{OUT} = 28V				1	µA
TIMING							
IN to OUT/$\overline{OUT}$ Propagation Delay	t_{DELAY}	V_{IN} rising	C_{CDELAY} = 0µF		40		µs
			C_{CDELAY} = 0.047µF		190		ms
	t_{DL}	V_{IN} falling			16		µs
Startup Delay (Note 5)					2		ms
ENABLE/$\overline{ENABLE}$ Minimum Input Pulse Width	t_{PW}			1			µs
ENABLE/$\overline{ENABLE}$ Glitch Rejection					100		ns
ENABLE/$\overline{ENABLE}$ to OUT/$\overline{OUT}$ Delay	t_{OFF}	From device enabled to device disabled			150		ns
ENABLE/$\overline{ENABLE}$ to OUT/$\overline{OUT}$ Delay	t_{PROPP}	From device disabled to device enabled (P version)			150		ns
	t_{PROPA}	From device disabled to device enabled (A version)	C_{CDELAY} = 0µF		20		µs
			C_{CDELAY} = 0.047µF		190		ms

Note 2: All devices are production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 3: When V_{CC} falls below the UVLO threshold, the outputs will deassert (OUT goes low, $\overline{OUT}$ goes high). When V_{CC} falls below 1.2V, the out cannot be determined.
Note 4: Guaranteed by design.
Note 5: During the initial power-up, V_{CC} must exceed 1.5V for at least 2ms before the output is guaranteed to be in the correct state.

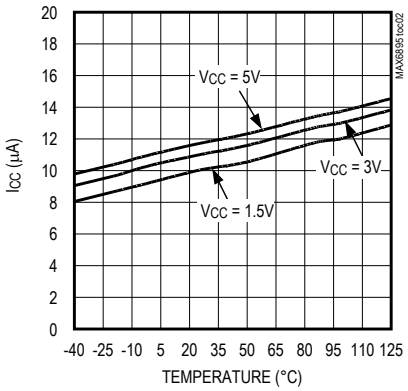
Typical Operating Characteristics

(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)

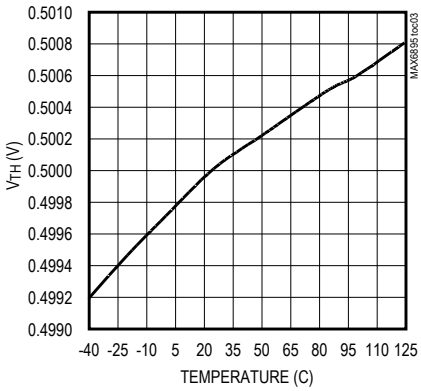
SUPPLY CURRENT vs. SUPPLY VOLTAGE



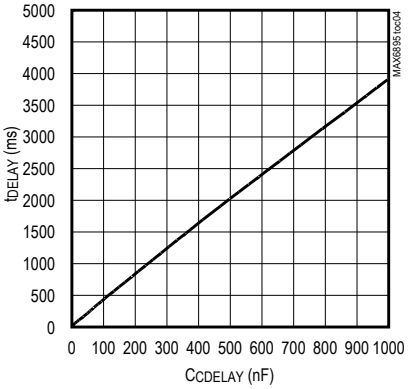
SUPPLY CURRENT vs. TEMPERATURE



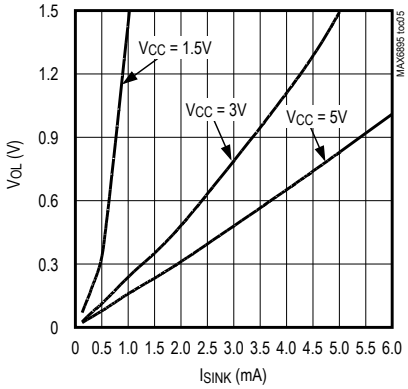
IN THRESHOLD vs. TEMPERATURE



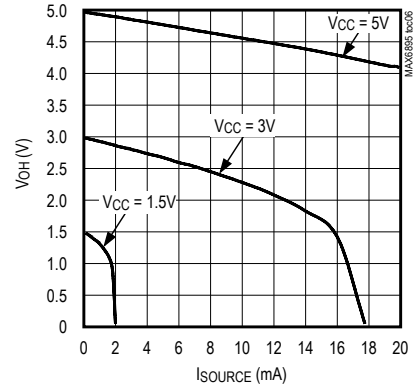
OUT DELAY vs. CCDELAY



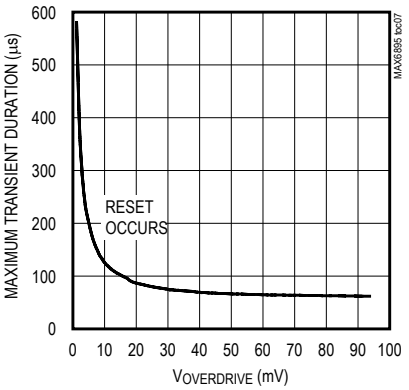
OUTPUT LOW VOLTAGE vs. SINK CURRENT



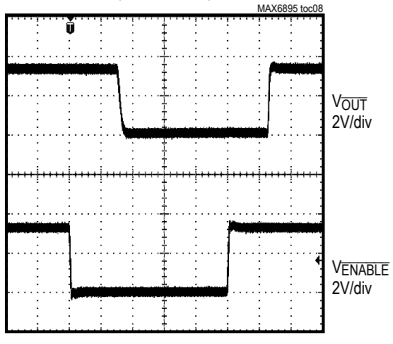
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



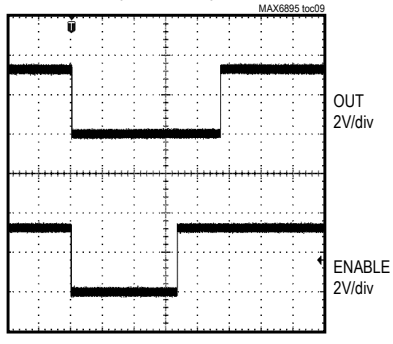
MAXIMUM TRANSIENT DURATION vs. INPUT OVERDRIVE



ENABLE TURN-ON/OFF (MAX6896P)



ENABLE TURN-ON/OFF DELAY (MAX6895A)



Pin Description

PIN						NAME	FUNCTION
MAX6895/ MAX6897		MAX6896/ MAX6898		MAX6899			
µDFN	THIN SOT23	µDFN	THIN SOT23	µDFN	THIN SOT23		
1	1	—	—	—	—	ENABLE	Active-High Logic-Enable Input. Drive ENABLE low to immediately deassert the output to its false state (OUT = low or $\overline{OUT}$ = high) independent of V_{IN}. With V_{IN} above V_{TH}, drive ENABLE high to assert the output to its true state (OUT = high or $\overline{OUT}$ = low) after the adjustable delay period (MAX689_A) or a 150ns propagation delay (MAX689_P).
—	—	1	1	1	1	$\overline{ENABLE}$	Active-Low Logic-Enable Input. Drive $\overline{ENABLE}$ high to immediately deassert the output to its false state (OUT = low or $\overline{OUT}$ = high) independent of V_{IN}. With V_{IN} above V_{TH}, drive $\overline{ENABLE}$ low to assert the output to its true state (OUT = high or $\overline{OUT}$ = low) after the adjustable delay period (MAX689_A) or a 150ns propagation delay (MAX689_P).
2	2	2	2	2	2	GND	Ground
3	3	3	3	3	3	IN	High-Impedance Monitor Input. Connect IN to an external resistive divider to set the desired monitored threshold. The output changes state when V_{IN} rises above 0.5V and when V_{IN} falls below 0.495V.
4	4	—	—	4	4	OUT	Active-High Sequencer/Monitor Output, Push-Pull (MAX6895/MAX6899) or Open-Drain (MAX6897). OUT is asserted to its true state (OUT = high) when V_{IN} is above V_{TH} and the enable input is in its true state (ENABLE = high or $\overline{ENABLE}$ = low) for the capacitor-adjusted delay period. OUT is deasserted to its false state (OUT = low) immediately after V_{IN} drops below V_{TH} - 5mV or the enable input is in its false state (ENABLE = low or $\overline{ENABLE}$ = high). The open-drain version requires an external pullup resistor.
—	—	4	4	—	—	$\overline{OUT}$	Active-Low Sequencer/Monitor Output, Push-Pull (MAX6896) or Open-Drain (MAX6898). OUT is asserted to its true state ($\overline{OUT}$ = low) when V_{IN} is above V_{TH} and the enable input is in its true state (ENABLE = high or $\overline{ENABLE}$ = low) after the CDELAY adjusted timeout period. OUT is deasserted to its false state ($\overline{OUT}$ = high) immediately after V_{IN} drops below V_{TH} - 5mV or the enable input is in its false state (ENABLE = low or $\overline{ENABLE}$ = high). The open-drain version requires an external pullup resistor.
5	6	5	6	5	6	CDELAY	Capacitor-Adjustable Delay. Connect an external capacitor (C_{CDELAY}) from CDELAY to GND to set the IN to OUT (and ENABLE to OUT or $\overline{ENABLE}$ to OUT for A version devices) delay period. t_{DELAY} = (C_{CDELAY} x 4.0 x 10^6) + 40µs. There is a fixed short delay (40µs, typ) for the output deasserting when V_{IN} falls below V_{TH}.
6	5	6	5	6	5	V_{CC}	Supply Voltage Input. Connect a 1.5V to 5.5V supply to V_{CC} to power the device. For noisy systems, bypass with a 0.1µF ceramic capacitor to GND.

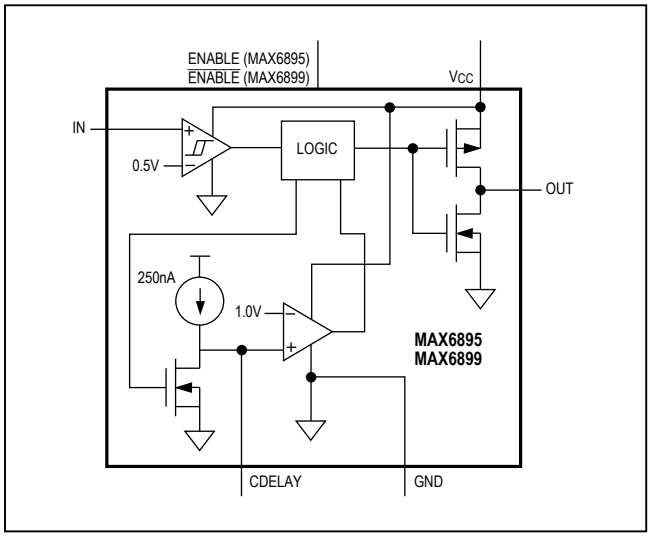


Figure 1. MAX6895/MAX6899 Functional Diagram

Detailed Description

The MAX6895–MAX6899 is a family of ultra-small, low-power, sequencing/supervisory circuits. These devices provide adjustable voltage monitoring for inputs down to 0.5V. They are ideal for use in power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

Voltage monitoring is performed through a high-impedance input (IN) with an internally fixed 0.5V threshold. When the voltage at IN falls below 0.5V or when the enable input is deasserted (ENABLE = low or $\overline{\text{ENABLE}}$ = high), the output deasserts (OUT goes low or $\overline{\text{OUT}}$ goes high). When VIN rises above 0.5V and the enable input is asserted (ENABLE = high or $\overline{\text{ENABLE}}$ = low), the output asserts (OUT goes high or OUT goes low) after a capacitor-programmable time delay.

With VIN above 0.5V, the enable input can be used to turn the output on or off. After the enable input is asserted, the output turns on with a capacitor-programmable delay period (A version) or with a 150ns propagation delay (P version). Tables 1, 2, and 3 detail the output state depending on the various input and enable conditions.

Table 1. MAX6895/MAX6897 Output

IN	ENABLE	OUT
$V_{IN} < V_{TH}$	Low	Low
$V_{IN} < V_{TH}$	High	Low
$V_{IN} > V_{TH}$	Low	Low
$V_{IN} > V_{TH}$	High	OUT = V_{CC} (MAX6895)
		OUT = high Impedance (MAX6897)

Table 2. MAX6896/MAX6898 Output

IN	$\overline{\text{ENABLE}}$	$\overline{\text{OUT}}$
$V_{IN} < V_{TH}$	Low	$\overline{\text{OUT}}$ = V_{CC} (MAX6896)
		$\overline{\text{OUT}}$ = high impedance (MAX6898)
$V_{IN} < V_{TH}$	High	$\overline{\text{OUT}}$ = V_{CC} (MAX6896)
		$\overline{\text{OUT}}$ = high impedance (MAX6898)
$V_{IN} > V_{TH}$	Low	Low
$V_{IN} > V_{TH}$	High	$\overline{\text{OUT}}$ = V_{CC} (MAX6896)
		$\overline{\text{OUT}}$ = high impedance (MAX6898)

Table 3. MAX6899 Output

IN	$\overline{\text{ENABLE}}$	OUT
$V_{IN} < V_{TH}$	Low	Low
$V_{IN} < V_{TH}$	High	Low
$V_{IN} > V_{TH}$	Low	High
$V_{IN} > V_{TH}$	High	Low

Supply Input (V_{CC})

The device operates with a V_{CC} supply voltage from 1.5V to 5.5V. To maintain a 1.8% accurate threshold, VCC must be above 1.5V. When V_{CC} falls below the UVLO threshold, the output deasserts. When V_{CC} falls below 1.2V the output state cannot be determined. For noisy systems, connect a 0.1µF ceramic capacitor from V_{CC} to GND as close to the device as possible. For the push-pull active-high output option, a 100kΩ external pulldown resistor to ground ensures the correct logic state for V_{CC} down to 0.

Monitor Input (IN)

Connect the center point of a resistive divider to IN to monitor external voltages (see R1 and R2 of the *Typical Operating Circuit*). IN has a rising threshold of V_{TH} = 0.5V and a falling threshold of 0.495V (5mV hysteresis). When V_{IN} rises above V_{TH} and $\overline{ENABLE}$ is high (or $\overline{ENABLE}$ is low) OUT goes high (OUT goes low) after the programmed t_{DELAY} period. When V_{IN} falls below 0.495V, OUT goes low (OUT goes high) after a 16µs delay. IN has a maximum input current of 15nA so large-value resistors are permitted without adding significant error to the resistive divider.

Adjustable Delay (CDELAY)

When V_{IN} rises above V_{TH} with ENABLE high ($\overline{ENABLE}$ low), the internal 250nA current source begins charging an external capacitor connected from CDELAY to GND. When the voltage at CDELAY reaches 1V, the output asserts (OUT goes high or $\overline{OUT}$ goes low). When the output asserts, C_{CDELAY} is immediately discharged. Adjust the delay (t_{DELAY}) from when V_{IN} rises above V_{TH} (with ENABLE high or $\overline{ENABLE}$ low) to OUT going high ($\overline{OUT}$ going low) according to the equation:

$$t_{DELAY} = C_{CDELAY} \times 4.0 \times 10^6 + 40\mu s$$

where C_{CDELAY} is the external capacitor from CDELAY to GND.

For adjustable delay devices (A version), when V_{IN} > 0.5V and ENABLE goes from low to high ($\overline{ENABLE}$ goes from high to low) the output asserts after a t_{DELAY} period. For nonadjustable delay devices (P version) there is a 1µs propagation delay from when the enable input is asserted to when the output asserts. Figures 2 through 5 show the timing diagrams for the adjustable and fixed delay versions, respectively.

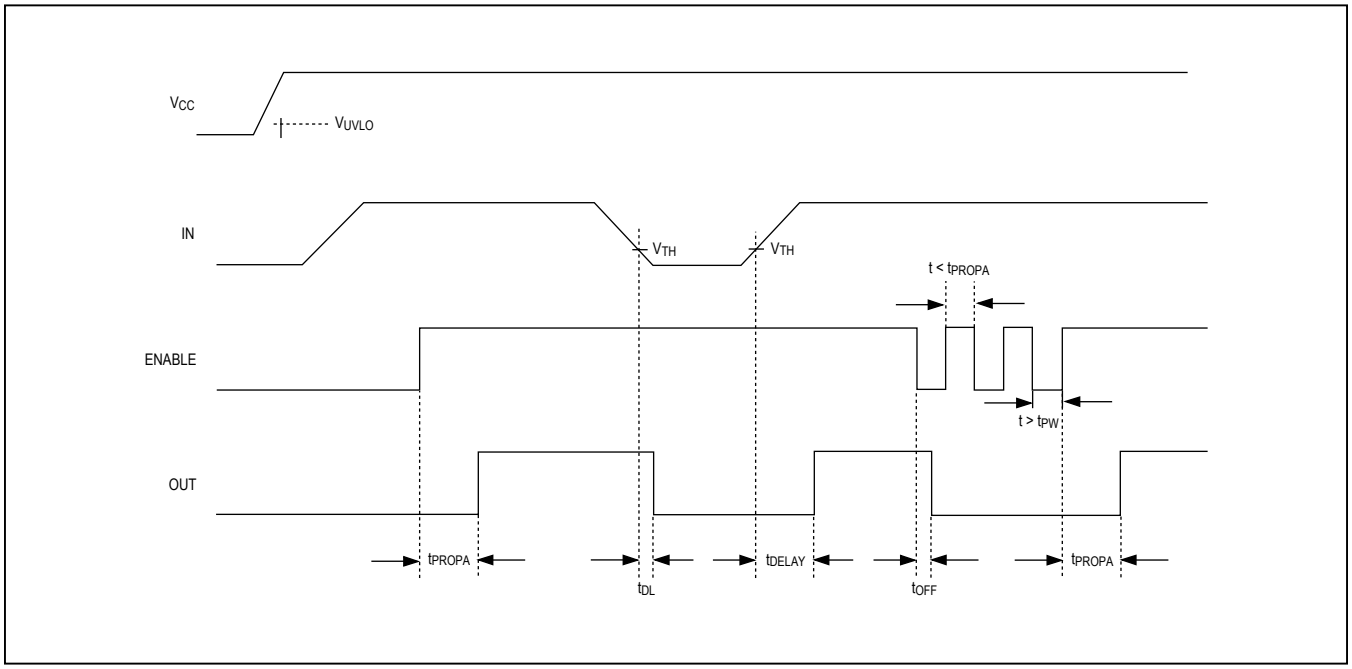


Figure 2. MAX6895A/MAX6897A Timing Diagram

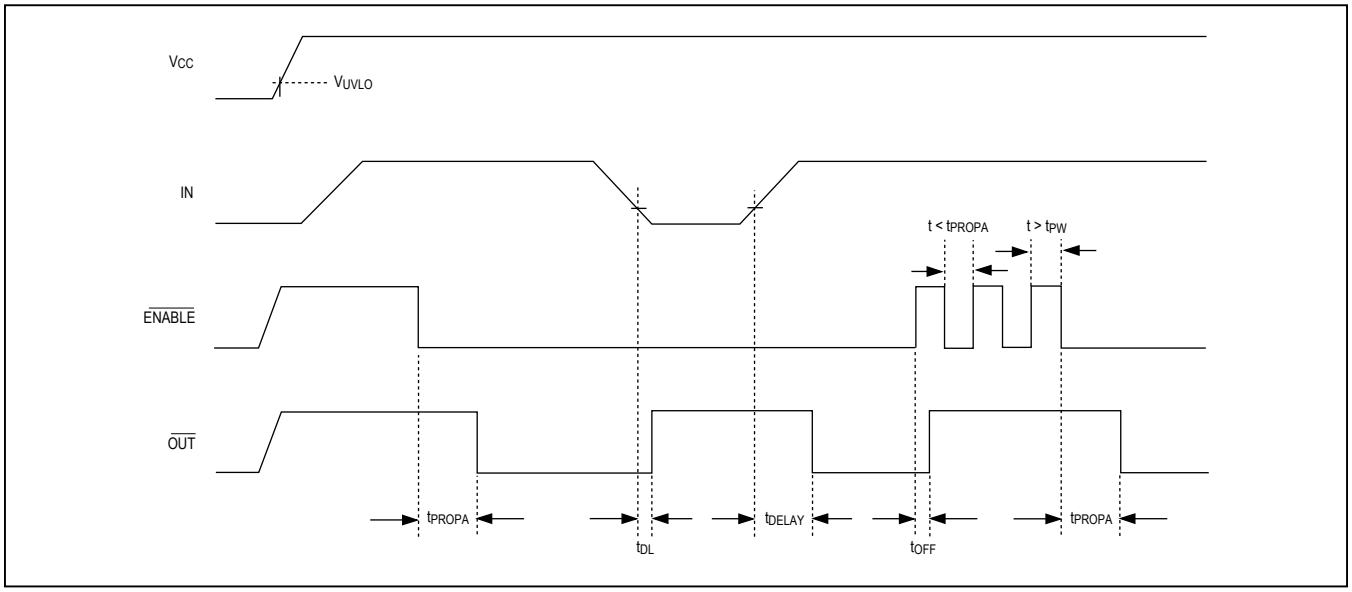


Figure 3. MAX6896A/MAX6898A Timing Diagram

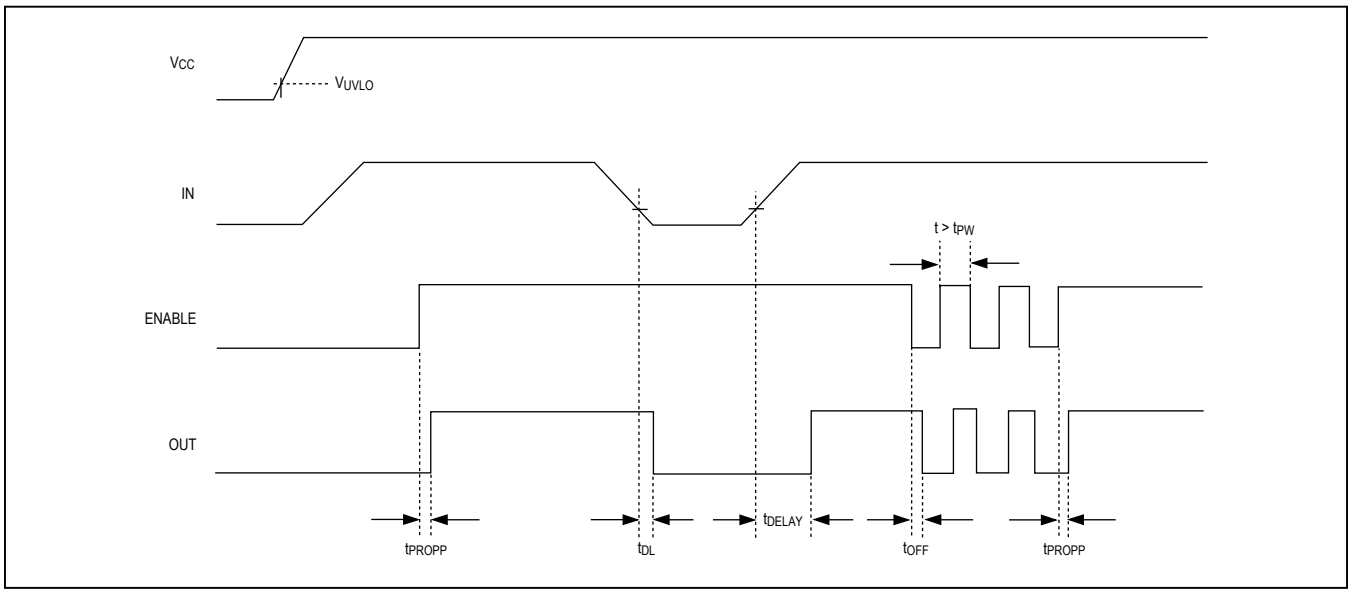


Figure 4. MAX6895P/MAX6897P Timing Diagram

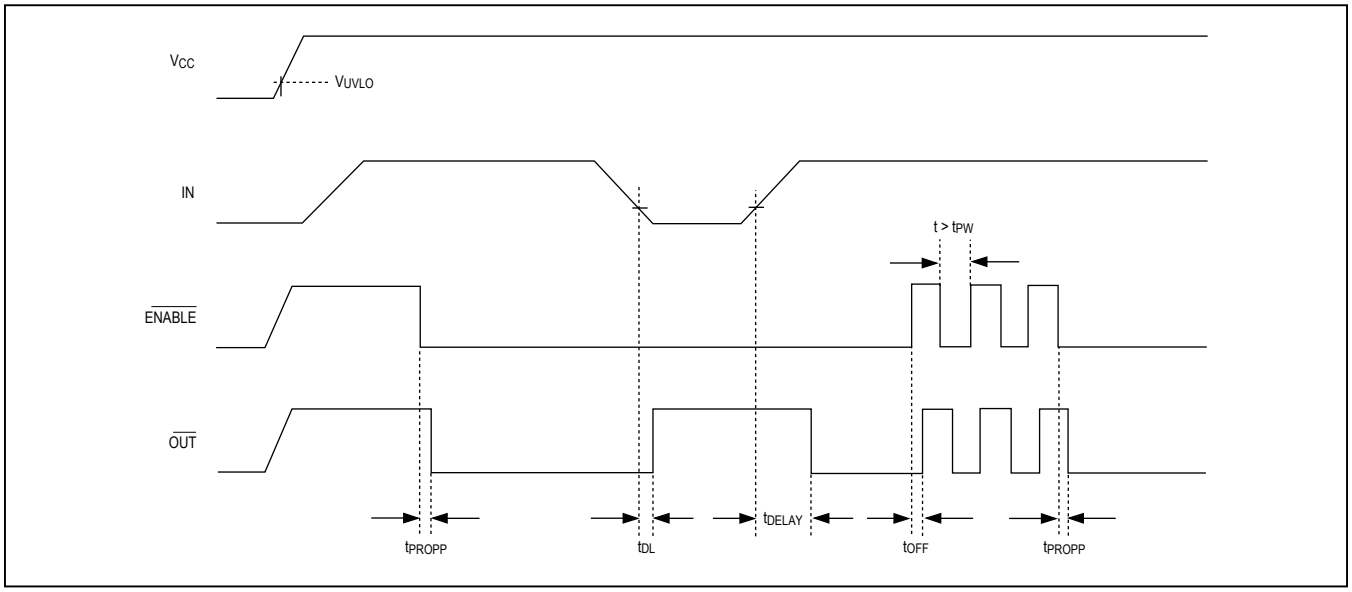


Figure 5. MAX6896P/MAX6898P Timing Diagram

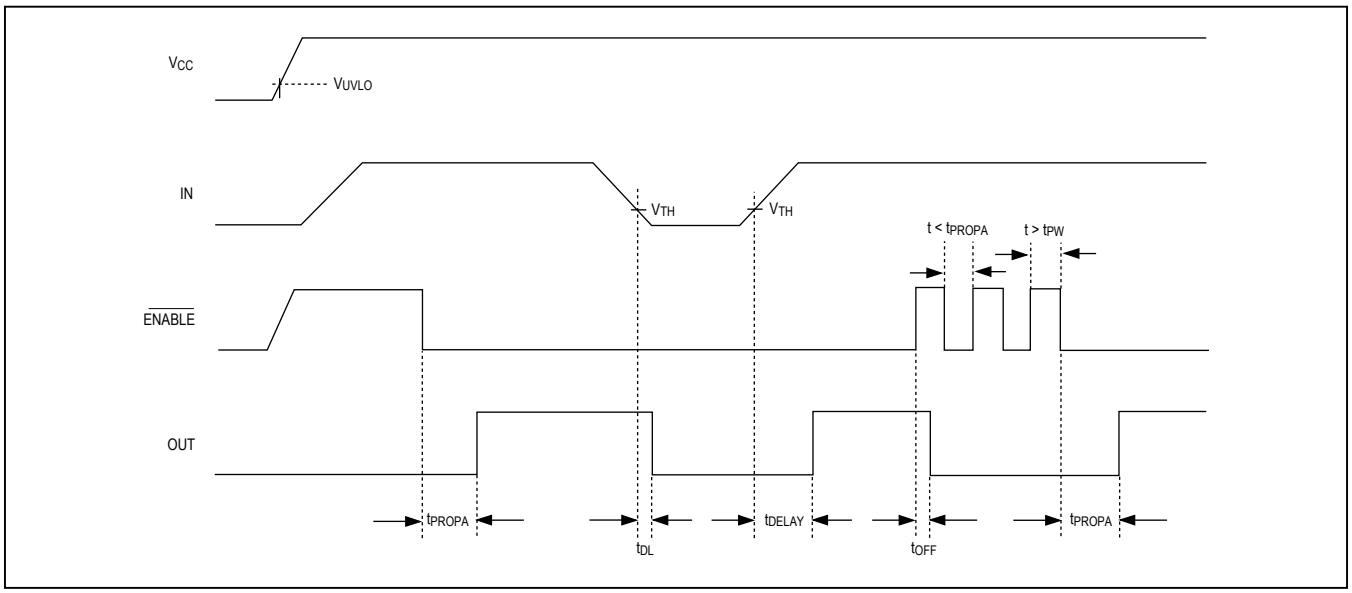


Figure 6. MAX6899A Timing Diagram

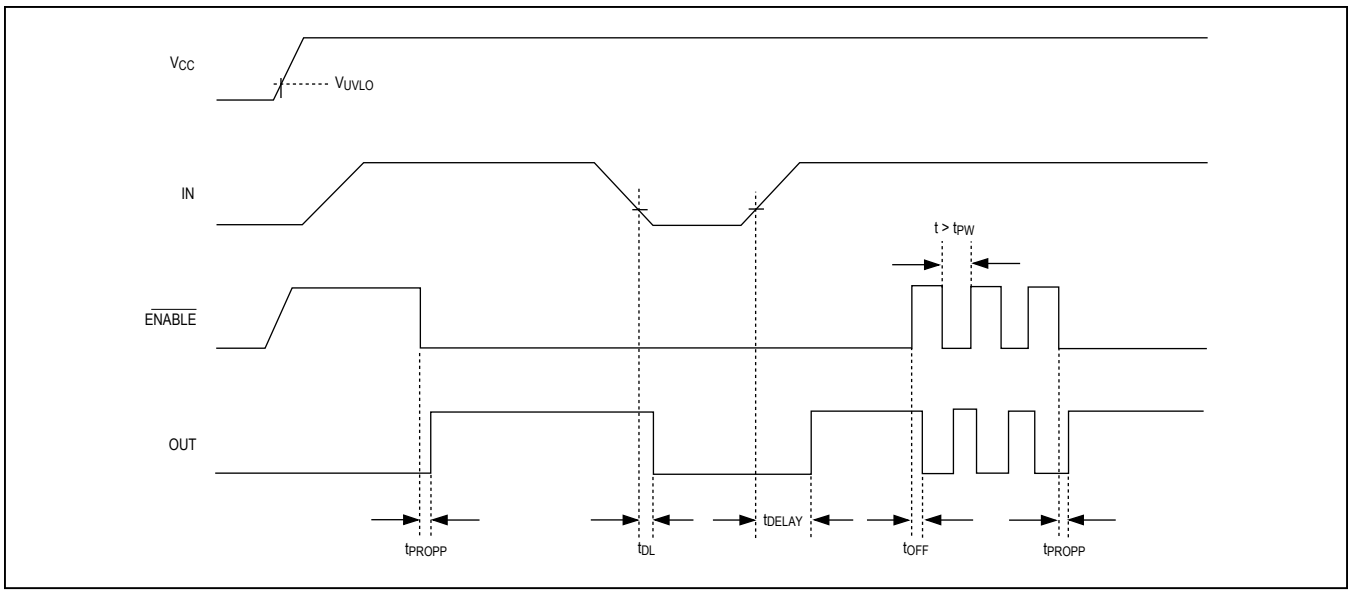


Figure 7. MAX6899P Timing Diagram

Enable Input (ENABLE or $\overline{\text{ENABLE}}$)

The MAX6895/MAX6897 offer an active-high enable input (ENABLE), while the MAX6896/MAX6898/MAX6899 offer an active-low enable input ($\overline{\text{ENABLE}}$). With V_{IN} above V_{TH}, drive ENABLE high ($\overline{\text{ENABLE}}$ low) to force OUT high ($\overline{\text{OUT}}$ low) after the adjustable delay time (A versions). For P version devices, when V_{IN} > 0.5V and enable is asserted, the output asserts after typically 150ns.

The enable input has logic-high and logic-low voltage thresholds of 1.4V and 0.4V, respectively. For both versions, when V_{IN} > 0.5V, drive ENABLE low ($\overline{\text{ENABLE}}$ high) to force OUT low ($\overline{\text{OUT}}$ high) within 150ns typ.

Output (OUT or $\overline{\text{OUT}}$)

The MAX6895/MAX6899 offer an active-high, push-pull output (OUT), and the MAX6896 offers an active-low push-pull output ($\overline{\text{OUT}}$). The MAX6897 offers an active-high open-drain output (OUT), and the MAX6898 offers an active-low open-drain output ($\overline{\text{OUT}}$).

Push-pull output devices are referenced to V_{CC}. Open-drain outputs can be pulled up to 28V.

Applications Information

Input Threshold

The MAX6895–MAX6899 monitor the voltage on IN with an external resistive divider (see R1 and R2 in the *Typical Operating Circuit*). Connect R1 and R2 as close to IN as possible. R1 and R2 can have very high values to minimize current consumption due to low IN leakage currents (±15nA max). Set R2 to some conveniently high value (1MΩ, for example) and calculate R1 based on the desired monitored voltage using the following formula:

$$R1 = R2 \times \left[\frac{V_{MONITOR}}{V_{IN}} - 1 \right] *$$

where $V_{MONITOR}$ is the desired monitored voltage and V_{IN} is the detector input threshold (0.5V).

Pullup Resistor Values (MAX6897/MAX6898)

The exact value of the pullup resistors for the open-drain outputs is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if V_{CC} = 2.25V and the pullup voltage is 28V, you would try to keep the sink current less than 0.5mA as shown in the *Electrical Characteristics* table. As a result, the pullup resistor should be greater than 56kΩ. For a 12V pullup, the resistor should be larger than 24kΩ. It should be noted that the ability to sink current is dependent on the V_{CC} supply voltage.

Typical Application Circuits

Figures 8, 9, 10 show typical applications for the MAX6895–MAX6899. Figure 8 shows the MAX6895 used with a p-channel MOSFET in an overvoltage protection circuit. Figure 9 shows the MAX6895 in a low-voltage sequencing application using an n-channel MOSFET. Figure 10 shows the MAX6895 used in a multiple-output sequencing application.

Using an n-Channel Device for Sequencing

In higher power applications, using an n-channel device reduces the loss across the MOSFETs as it offers a lower drain-to-source on-resistance. However, an n-channel MOSFET requires a sufficient VGS voltage to fully enhance it for a low RDS_ON. The application in Figure 9 shows the MAX6895 in a switch sequencing application using an n-channel MOSFET.

Similarly, if a higher voltage is present in the system, the open-drain version can be used in the same manner.

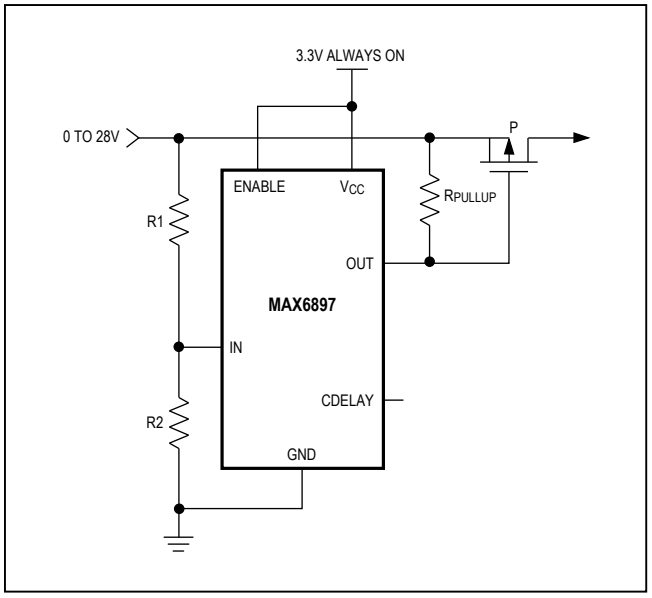


Figure 8. Overvoltage Protection

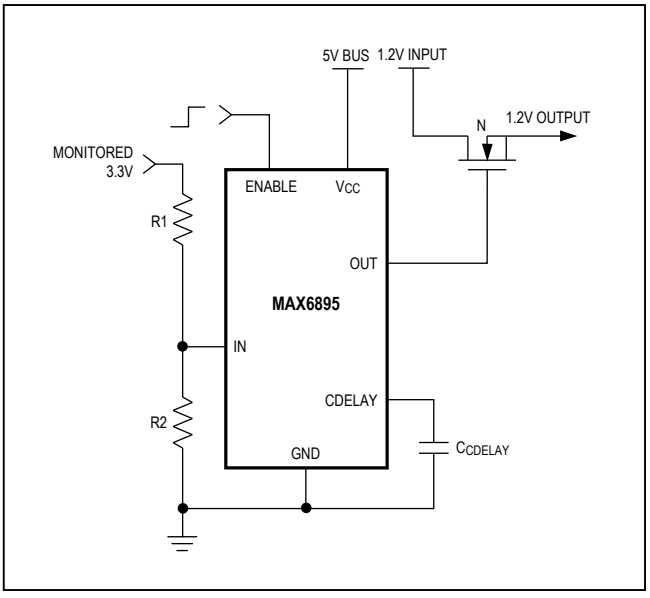


Figure 9. Low-Voltage Sequencing Using an n-Channel MOSFET

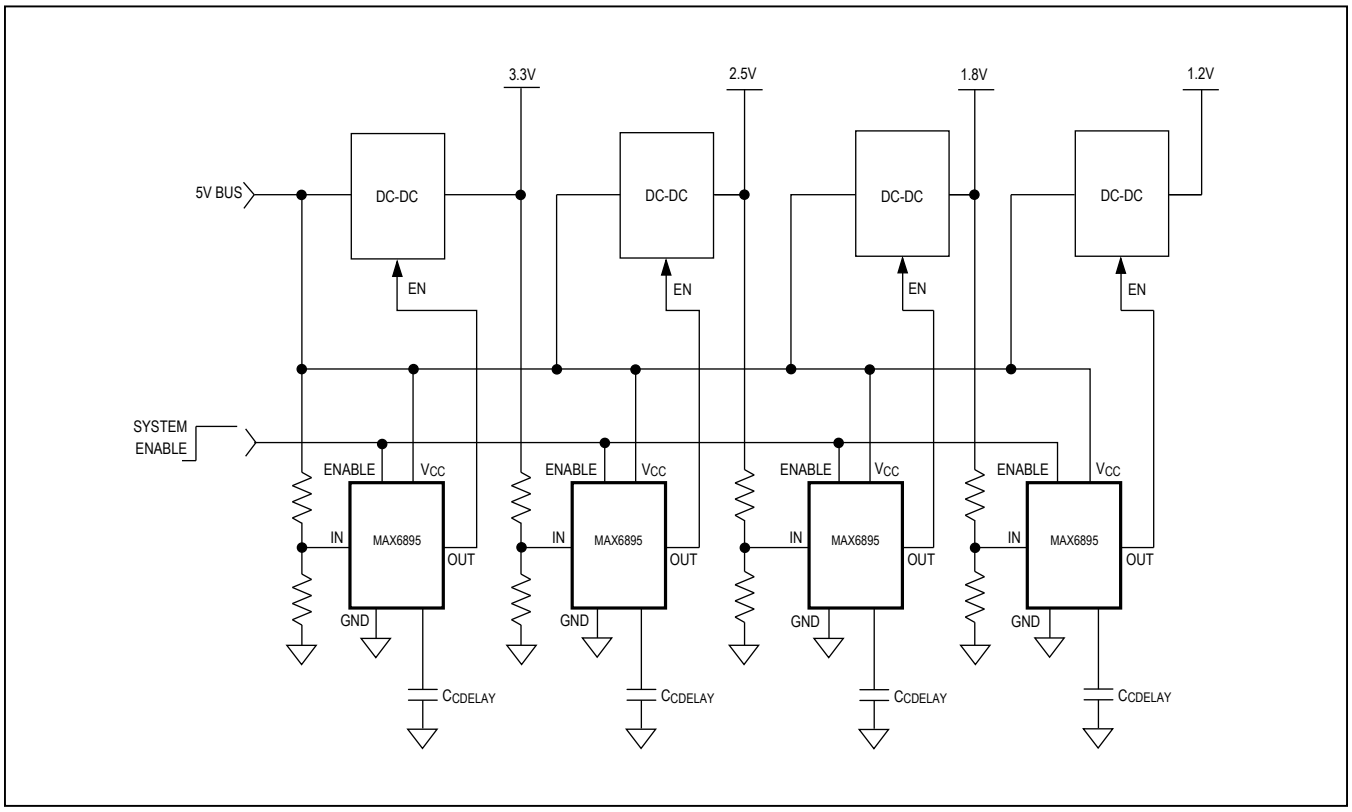


Figure 10. Multiple-Output Sequencing

Ordering Information

PART	PIN-PACKAGE	TOP MARK
MAX6895AALT+	6 µDFN	+AW
MAX6895AAZT+	6 Thin SOT23	+AADK
MAX6895AAZT/V+T	6 Thin SOT23	+AATF
MAX6895PALT+T	6 µDFN	+AX
MAX6895PAZT+	6 Thin SOT23	+AADL
MAX6896AALT+	6 µDFN	+AY
MAX6896AAZT+	6 Thin SOT23	+AADO
MAX6896AAZT/V+T	6 Thin SOT23	+AATA
MAX6896PALT+T	6 µDFN	+AZ
MAX6896PAZT+	6 Thin SOT23	+AADP
MAX6897AALT+	6 µDFN	+BA
MAX6897AAZT+	6 Thin SOT23	+AADQ
MAX6897AAZT/V+	6 Thin SOT23	+AADX
MAX6897AAZT/V+T	6 Thin SOT23	+AADX
MAX6897PALT+T	6 µDFN	+BB
MAX6897PAZT+	6 Thin SOT23	+AADR
MAX6898AALT+	6 µDFN	+BD

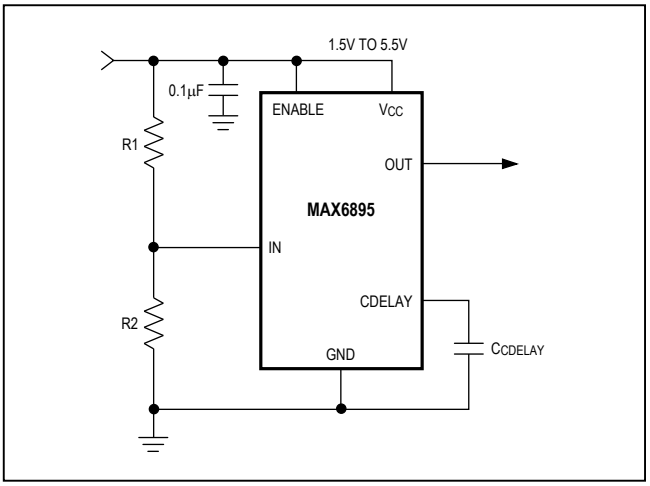
PART	PIN-PACKAGE	TOP MARK
MAX6898AAZT+	6 Thin SOT23	+AADS
MAX6898AAZT/V+*	6 Thin SOT23	—
MAX6898AAZT/V+T*	6 Thin SOT23	—
MAX6898PALT+T	6 µDFN	+BC
MAX6898PAZT+	6 Thin SOT23	+AADT
MAX6899AALT+	6 µDFN	+LO
MAX6899AAZT+	6 Thin SOT23	+AADM
MAX6899PALT+T	6 µDFN	+LP
MAX6899PAZT+	6 Thin SOT23	+AADN

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part; T = Tape and reel.
**Future product—Contact factory for availability.*

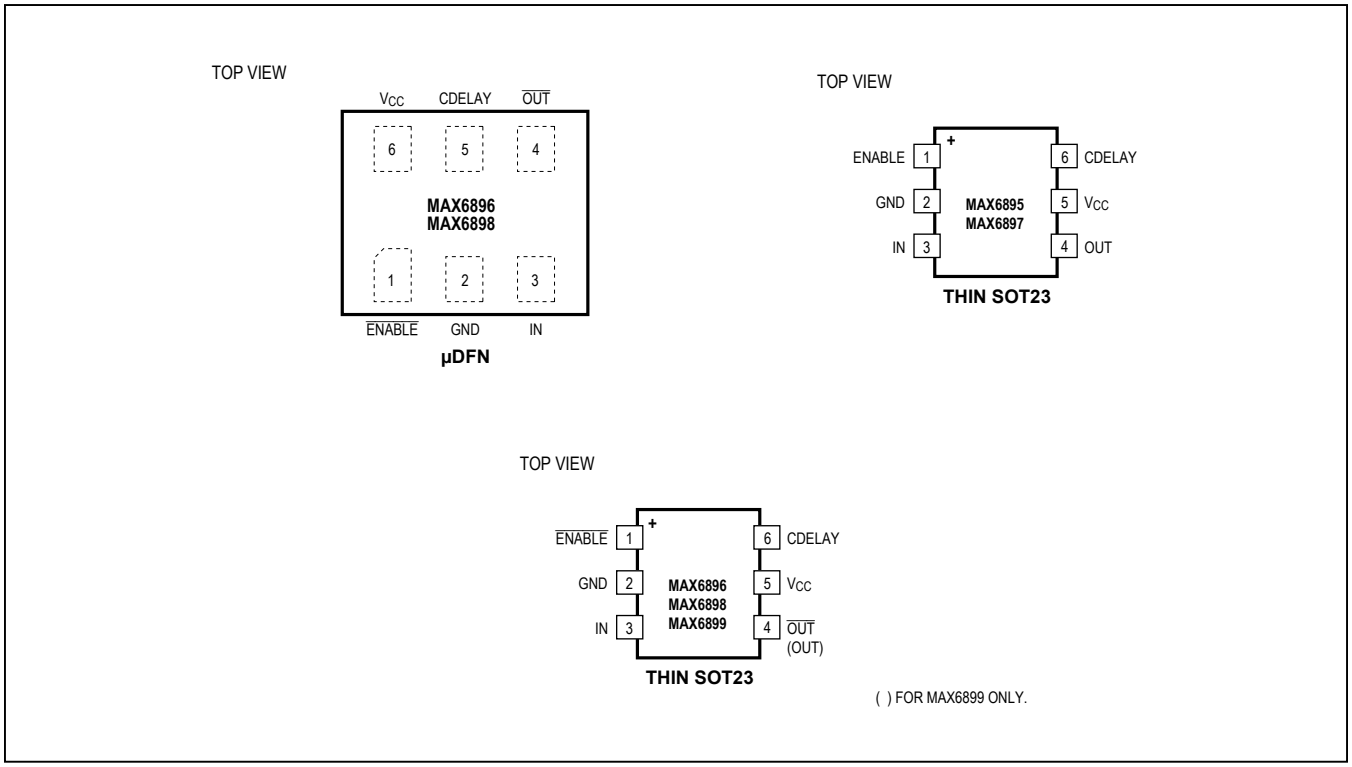
Selector Guide

PART	ENABLE INPUT	OUTPUT	INPUT (IN) DELAY	ENABLE DELAY
MAX6895AALT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX6895AAZT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX6895PALT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay
MAX6895PAZT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay
MAX6896AALT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX6896AAZT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX6896PALT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	150ns Delay
MAX6896PAZT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	150ns Delay
MAX6897AALT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX6897AAZT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX6897PALT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	150ns Delay
MAX6897PAZT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	150ns Delay
MAX6898AALT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX6898AAZT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX6898PALT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	150ns Delay
MAX6898PAZT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	150ns Delay
MAX6899AALT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX6899AAZT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX6899PALT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay
MAX6899PAZT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay

Typical Operating Circuit



Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 µDFN	L611+1	21-0147	90-0080
6 Thin SOT23	Z6+1, Z6+1A	21-0114	90-0242

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	10/07	—	1, 13, 18
6	11/09	Corrected *Absolute Maximum Ratings* and made style corrections *to Electrical Characteristics* and TOC8 and TOC9	2–5
7	7/10	Revised Figures 3, 4, and 6	7–9
8	7/11	Added automotive packages for MAX6896A and MAX6896P; added top mark to MAX6896AAZT/V+1 in the *Ordering Information* table	1
9	12/13	Added automotive packages for MAX6897 in the *Ordering Information* table	13
10	3/14	Added automotive packages for MAX6898 in the *Ordering Information* table	13
11	12/17	Added AEC statement and updated *Ordering Information* table	1, 12
12	3/18	Updated *Ordering Information* table	12
13	8/18	Updated *Ordering Information* table	12
14	9/18	Updated *Features* section	1