Absolute Maximum Ratings

V_{CC} ..... -0.3V to +6.0V
All Other Pins ..... -0.3V to (V_{CC} + 0.3V)
Input Current, WDI 20mA
Output Current, $\overline{WDO}$ 20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C) 247mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +2.25V to +5.5V, T_A = T_{MIN} to T_{MAX}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

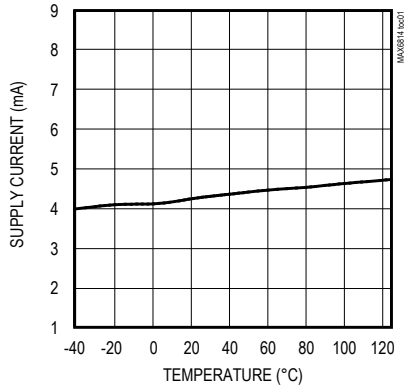
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	T_A = 0°C to +70°C		2.25		5.5	V
Supply Current	I_{SUPPLY}	WDI unconnected	V_{CC} = 5.5V		10	24	µA
			V_{CC} = 2.5V		4	12	
Undervoltage Lockout Threshold	UVLO	(Note 2)			2.19		V
Watchdog Pulse Period	t_{PP}	(Note 3)		140	200	280	ms
$\overline{WDO}$ Output Voltage	V_{OH}	I_{SOURCE} = 30µA, V_{CC} = 2.3V		0.8 × V_{CC}			V
	V_{OL}	I_{SINK} = 1.2mA, V_{CC} = 2.1V				0.3	
$\overline{WDO}$ Output Short-Circuit Current	I_{SOURCE}	V_{CC} = 3.6V (Note 4)				400	µA
Watchdog Timeout Period	t_{WD}			1.12	1.60	2.40	s
WDI Pulse Width	t_{WDI}	V_{IL} = 0.4V, V_{IH} = 0.8 × V_{CC}		50			ns
WDI Input Voltage (Note 5)	V_{IL}					0.3 × V_{CC}	V
	V_{IH}			0.7 × V_{CC}			
WDI Input Current (Note 6)		WDI = V_{CC}, time average			120	160	µA
		WDI = 0, time average		-20	-15		

Note 1: Overtemperature limits are guaranteed by design, production testing performed at +25°C only.
Note 2: $\overline{WDO}$ is low when V_{CC} falls below the undervoltage threshold. When V_{CC} rises above the undervoltage threshold, $\overline{WDO}$ goes high after the watchdog pulse period.
Note 3: Watchdog pulse period occurs when the watchdog times out or after V_{CC} rises above the undervoltage threshold.
Note 4: The $\overline{WDO}$ short-circuit current is the maximum pullup current when $\overline{WDO}$ is driven low.
Note 5: WDI is internally serviced within the watchdog period if WDI is left unconnected.
Note 6: The WDI input current is specified as the average input current when the WDI input is driven high or low. The WDI input is designed to drive a three-stated output device with a 10µA maximum leakage current and a maximum capacitive load of 200pF. This output device must be able to source and sink at least 200µA when active.

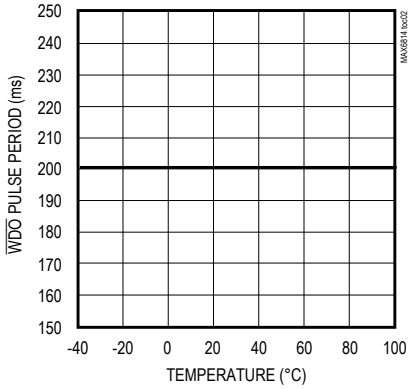
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

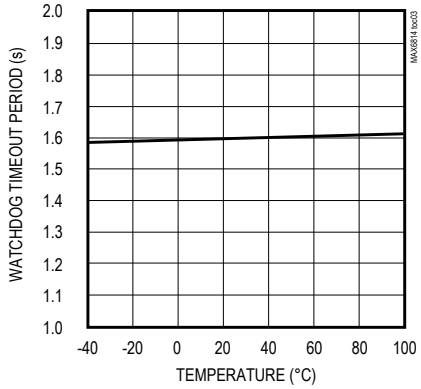
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



$\overline{WDO}$ PULSE PERIOD vs. TEMPERATURE



WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	$\overline{WDO}$	Active-Low Watchdog Output. Pulses low for 140ms (min) when the watchdog timer exceeds the watchdog timeout period. $\overline{WDO}$ is low when V_{CC} is below the UVLO threshold and remains low for 140ms (min) after V_{CC} exceeds the UVLO threshold.
2	GND	Ground
3	N.C.	No Connection. Leave unconnected or connect to V_{CC}.
4	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a watchdog pulse period is triggered. The internal watchdog timer clears whenever a watchdog pulse period is asserted, or whenever WDI sees a rising or falling edge. If WDI is left unconnected or is connected to a three-stated buffer output, the watchdog is disabled.
5	V_{CC}	Supply Voltage

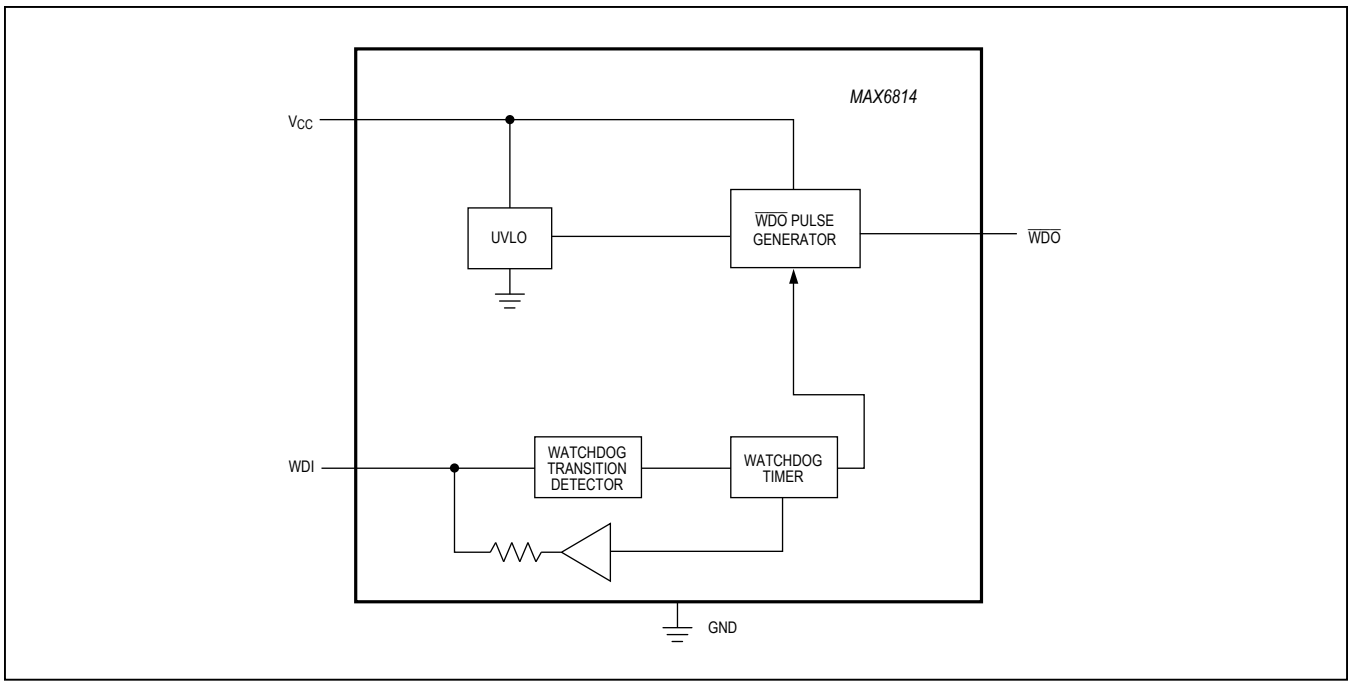


Figure 1. Functional Diagram

Detailed Description

Watchdog Input

In the MAX6814, the watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within t_{WD} (1.6s), $\overline{WDO}$ asserts. The internal 1.6s timer is cleared by either a $\overline{WDO}$ pulse or by toggling WDI, which detects pulses as short as 50ns. While $\overline{WDO}$ is asserted, the timer remains cleared and does not count. As soon as $\overline{WDO}$ is released, the timer starts counting (Figure 3).

Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period and high for the last 1/8 of the watchdog timeout period. When WDI is left unconnected, this internal driver clears the 1.6s timer every 1.4s. When WDI is three-stated or unconnected, the maximum allowable leakage current is 10µA and the maximum allowable load capacitance is 200pF.

Applications Information

Watchdog Input Current

The MAX6814 WDI inputs are internally driven through a buffer and series resistor from the watchdog counter (Figure 1). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 7/8 of the watchdog timeout period to clear the watchdog timer. If WDI is externally driven high for the majority of the timeout period, up to 160µA can flow into WDI.

Watchdog Software Considerations

One way to help the watchdog timer monitor software execution more closely is to set and clear the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be cleared inside the loop, keeping the watchdog from timing out.

Figure 4 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing an interrupt to be issued. This scheme results in higher time average WDI input current than does leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low (see the *Watchdog Input Current* section).

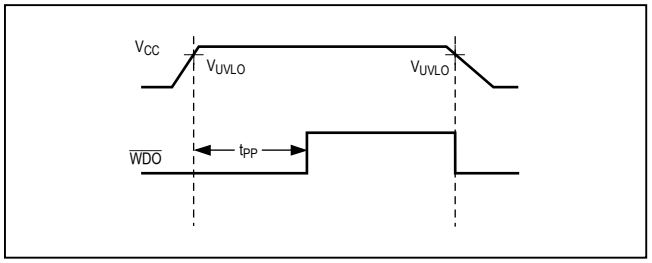


Figure 2. Power-Up Timing Diagram

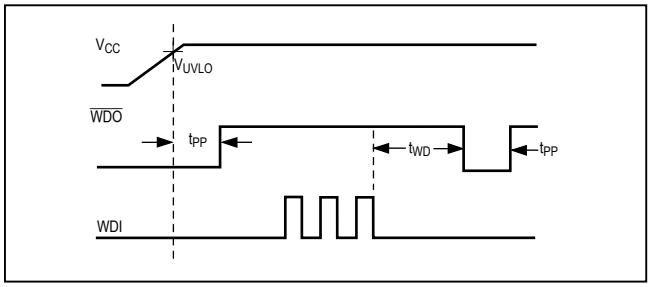


Figure 3. Watchdog Timing Relationship

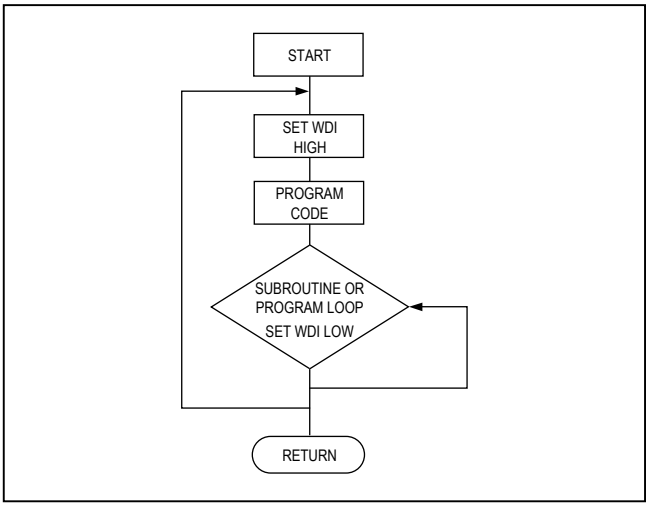


Figure 4. Watchdog Flow Diagram

Chip Information

TRANSISTOR COUNT: 607

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SC70	X5+1	21-0076	90-0188

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	7/14	No /V OPNs; removed Automotive reference from *Applications* section	1

