

MAX5487/MAX5488/ MAX5489

Dual, 256-Tap, Nonvolatile, SPI-Interface, Linear-Taper Digital Potentiometers

Absolute Maximum Ratings

V_{DD} to GND	-0.3V to +6.0V
All Other Pins to GND	-0.3V to the lower of ($V_{DD} + 0.3V$) and +6.0V
Maximum Continuous Current into H_{-} , W_{-} , and L_{-} MAX5487	±5.0mA
MAX5488	±1.3mA
MAX5489	±0.6mA

Continuous Power Dissipation ($T_A = +70^{\circ}\text{C}$)	
16-Pin TQFN (derate 17.5mW/ $^{\circ}\text{C}$ above $+70^{\circ}\text{C}$)	1398mW
14-Pin TSSOP (derate 9.1mW/ $^{\circ}\text{C}$ above $+70^{\circ}\text{C}$)	727mW
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$
Junction Temperature	$+150^{\circ}\text{C}$
Storage Temperature Range	-60°C to $+150^{\circ}\text{C}$
Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$
Soldering Temperature (reflow)	$+260^{\circ}\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

($V_{DD} = +2.7V$ to $+5.25V$, $V_H = V_{DD}$, $V_L = \text{GND}$, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted. Typical values are at $V_{DD} = +5.0V$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (Voltage-Divider Mode, Figure 1)						
Resolution	N		256			Taps
Integral Nonlinearity	INL	(Note 2)			±1	LSB
Differential Nonlinearity	DNL	(Note 2)			±0.5	LSB
Dual-Code Matching		Register A = register B			2	LSB
End-to-End Resistor Tempco	TC _R			35		ppm/°C
Ratiometric Resistor Tempco				5		ppm/°C
Full-Scale Error		MAX5487		3.5	6	LSB
		MAX5488		-0.6	+1.2	
		MAX5489		-0.3	+1.2	
Zero-Scale Error		MAX5487		3.5	6	LSB
		MAX5488		-0.6	1.5	
		MAX5489		0.3	1	
DC PERFORMANCE (Variable-Resistor Mode, Figure 1)						
Resolution			256			Taps
Integral Nonlinearity (Note 3)		V _{DD} = 5.0V			±1.5	LSB
		V _{DD} = 3.0V			±3	
Differential Nonlinearity (Note 3)		V _{DD} = 5.0V			±1	LSB
		V _{DD} = 3.0V			±1	
DC PERFORMANCE (Resistor Characteristics)						
Wiper Resistance (Note 4)	R _W	V _{DD} = 5.0V		200	350	Ω
		V _{DD} = 3.0V		325	675	
Wiper Capacitance	C _W			50		pF
End-to-End Resistance	R _{HL}	MAX5487	7.5	10	12.5	kΩ
		MAX5488	37.5	50	62.5	
		MAX5489	75	100	125	

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DC Electrical Characteristics (continued)

($V_{DD} = +2.7V$ to $+5.25V$, $V_H = V_{DD}$, $V_L = GND$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{DD} = +5.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input High Voltage (Note 5)	V _{IH}	V _{DD} = 3.6V to 5.25V		2.4			V
		V _{DD} = 2.7V to 3.6V		0.7 x V _{DD}			
Input Low Voltage	V _{IL}	V _{DD} = 2.7V to 5.25V (Note 5)			0.8		V
Input Leakage Current	I _{IN}				±1.0		µA
Input Capacitance	C _{IN}				5.0		pF
AC PERFORMANCE							
Crosstalk		f _H = 1kHz, L ₋ = GND, measurement at W ₋ (Note 6)		-90			dB
-3dB Bandwidth	BW	Wiper at midscale C _{W₋} = 10pF	MAX5487	350		kHz	
			MAX5488	90			
			MAX5489	45			
Total Harmonic Distortion	THD	V _H = 1V _{RMS} at 1kHz, L ₋ = GND, measurement at W ₋		0.02		%	
TIMING CHARACTERISTICS (Analog)							
Wiper-Settling Time	t _S	Code 0 to 127 (Note 7)	MAX5487	0.5		µs	
			MAX5488	0.75			
			MAX5489	1.5			
TIMING CHARACTERISTICS (Digital, Figure 2, Note 8)							
SCLK Frequency				5			MHz
SCLK Clock Period	t _{CP}			200			ns
SCLK Pulse-Width High	t _{CH}			80			ns
SCLK Pulse-Width Low	t _{CL}			80			ns
CS Fall to SCLK Rise Setup	t _{CSS}			80			ns
SCLK Rise to CS Rise Hold	t _{CSH}			0			ns
DIN to SCLK Setup	t _{DS}			50			ns
DIN Hold after SCLK	t _{DH}			0			ns
SCLK Rise to CS Fall Delay	t _{CS0}			20			ns
CS Rise to SCLK Rise Hold	t _{CS1}			80			ns
CS Pulse-Width High	t _{CSW}			200			ns
Write NV Register Busy Time	t _{BUSY}			12			ms
Read NV Register Access Time	t _{ACC}			1			µs
Write Wiper Register to Output Delay	t _{WO}			1			µs
NONVOLATILE MEMORY RELIABILITY							
Data Retention		T _A = +85°C		50			Years
Endurance		T _A = +25°C		200,000			Stores
		T _A = +85°C		50,000			

DC Electrical Characteristics (continued)

($V_{DD} = +2.7V$ to $+5.25V$, $V_H = V_{DD}$, $V_L = GND$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{DD} = +5.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		2.70		5.25	V
Supply Current	I_{DD}	During write cycle only, digital inputs = V_{DD} or GND			400	μA
Standby Current		Digital inputs = V_{DD} or GND, $T_A = +25^{\circ}C$		0.5	1	μA

Note 1: All devices are production tested at $T_A = +85^{\circ}C$ and are guaranteed by design and characterization for $-40^{\circ}C < T_A < +85^{\circ}C$.

Note 2: DNL and INL are measured with the potentiometer configured as a voltage-divider with $H_- = V_{DD}$ and $L_- = 0$. The wiper terminal is unloaded and measured with an ideal voltmeter.

Note 3: DNL and INL are measured with the potentiometer configured as a variable resistor. H_- is unconnected and $L_- = 0$. For $V_{DD} = +5V$, the wiper terminal is driven with a source current of $400\mu A$ for the $10k\Omega$ configuration, $80\mu A$ for the $50k\Omega$ configuration, and $40\mu A$ for the $100k\Omega$ configuration. For $V_{DD} = +3V$, the wiper terminal is driven with a source current of $200\mu A$ for the $10k\Omega$ configuration, $40\mu A$ for the $50k\Omega$ configuration, and $20\mu A$ for the $100k\Omega$ configuration.

Note 4: The wiper resistance is the worst value measured by injecting the currents given in Note 3 into W_- with $L_- = GND$. $R_W = (V_W - V_H) / I_W$.

Note 5: The device draws higher supply current when the digital inputs are driven with voltages between $(V_{DD} - 0.5V)$ and $(GND + 0.5V)$. See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics* section.

Note 6: Wiper at midscale with a $10pF$ load.

Note 7: Wiper-settling time is the worst-case 0-to-50% rise time, measured between tap 0 and tap 127. $H_- = V_{DD}$, $L_- = GND$, and the wiper terminal is unloaded and measured with a $10pF$ oscilloscope probe (see Tap-to-Tap Switching Transient in the *Typical Operating Characteristics* section).

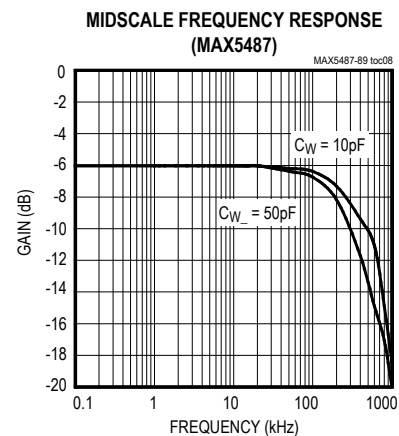
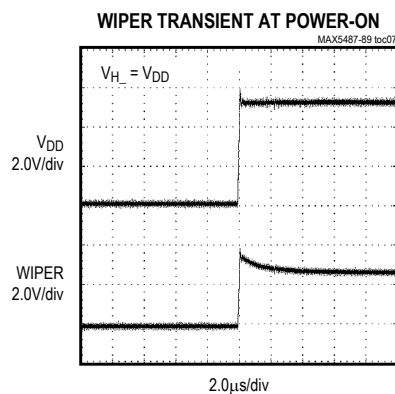
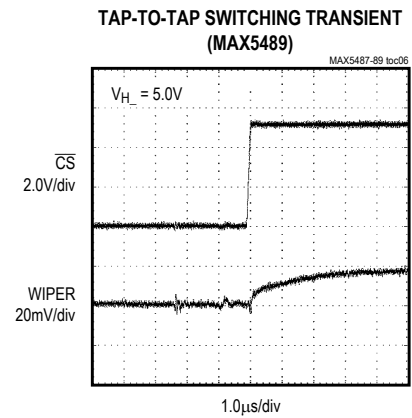
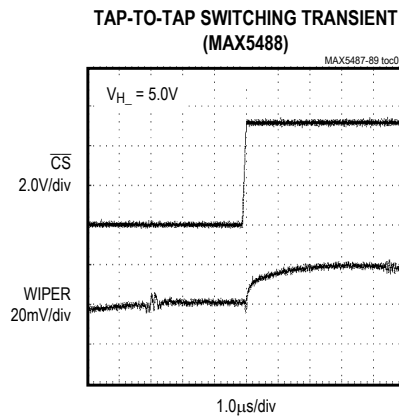
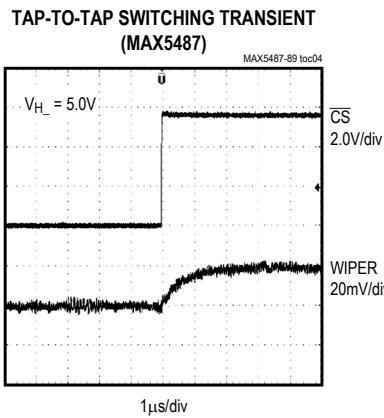
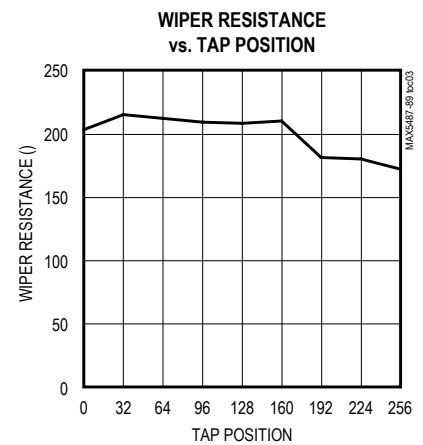
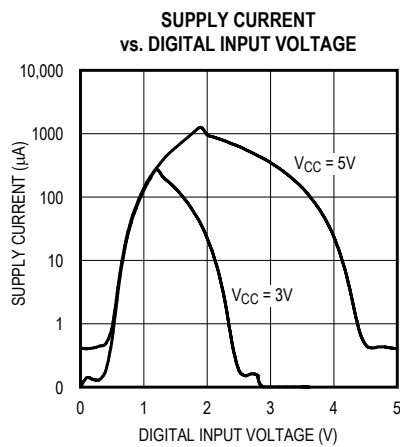
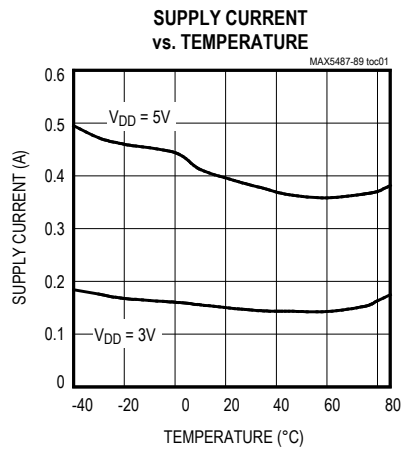
Note 8: Digital timing is guaranteed by design and characterization, and is not production tested.

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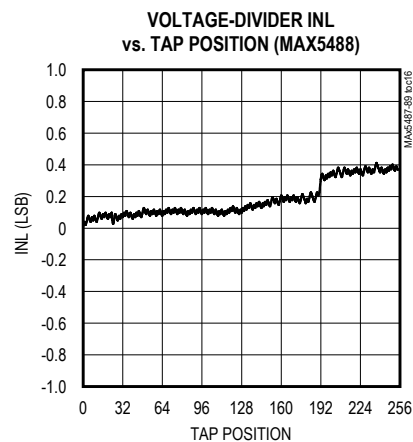
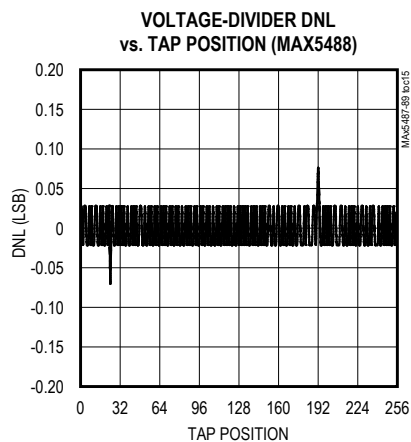
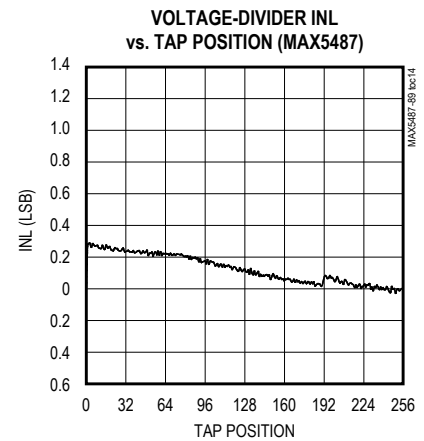
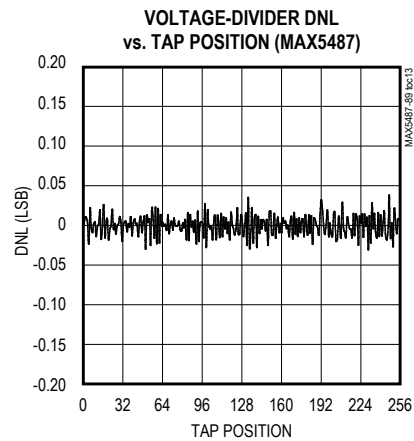
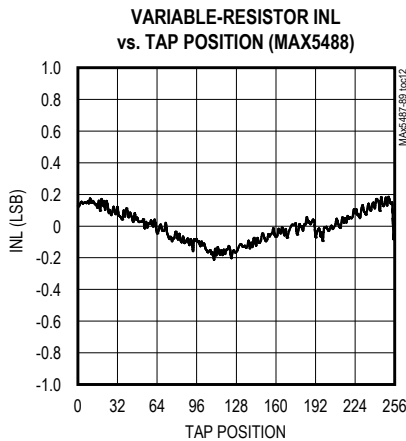
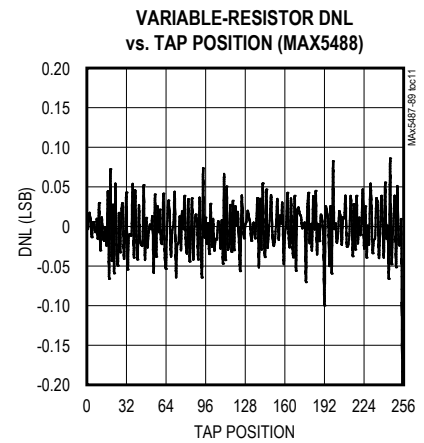
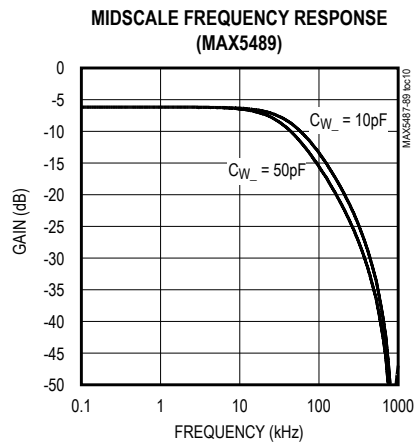
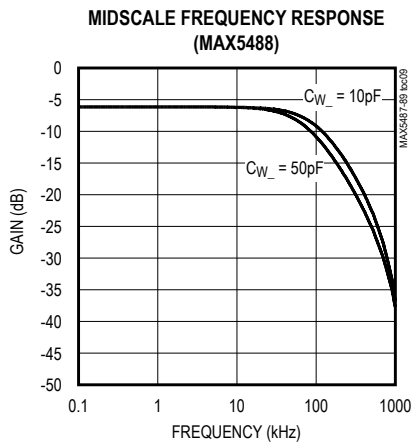
Typical Operating Characteristics

($V_{DD} = +5.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

($V_{DD} = +5.0V$, $T_A = +25^\circ C$, unless otherwise noted.)

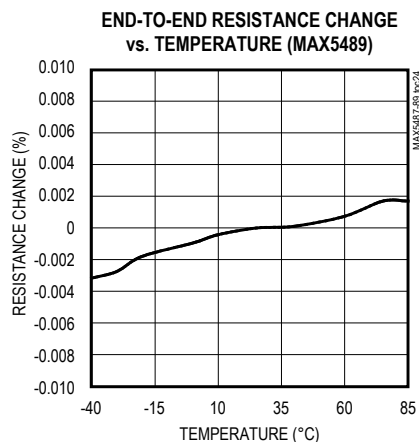
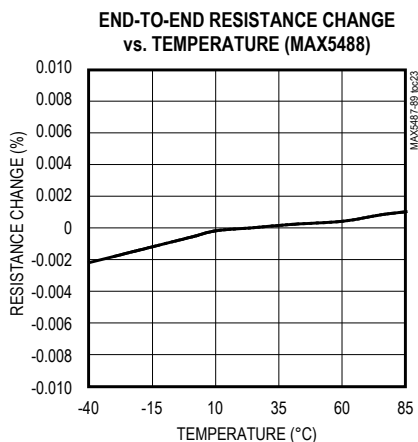
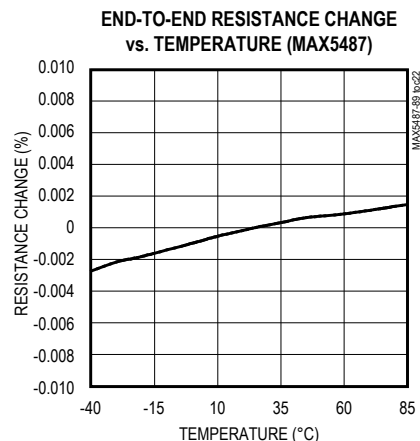
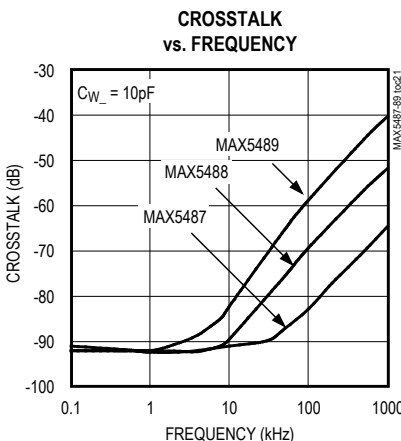
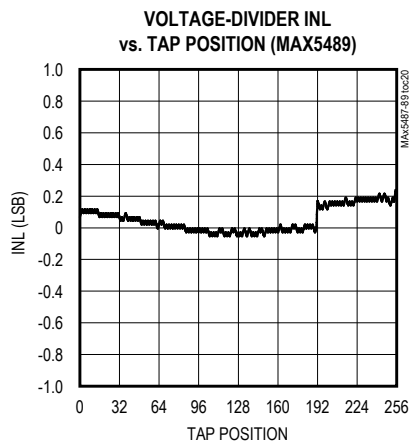
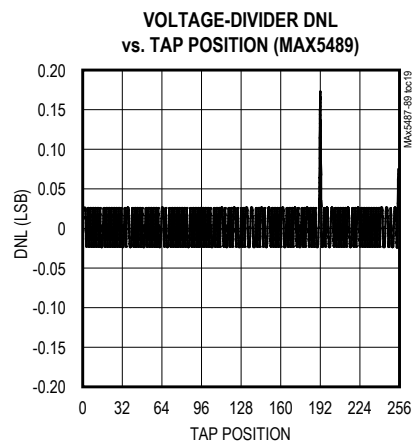
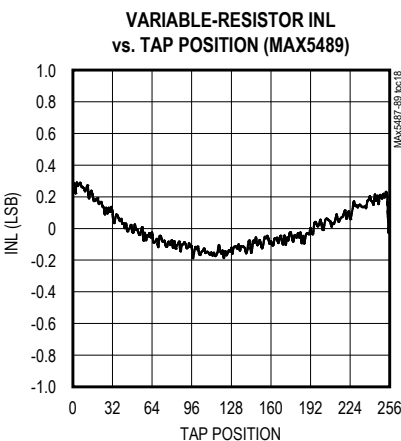
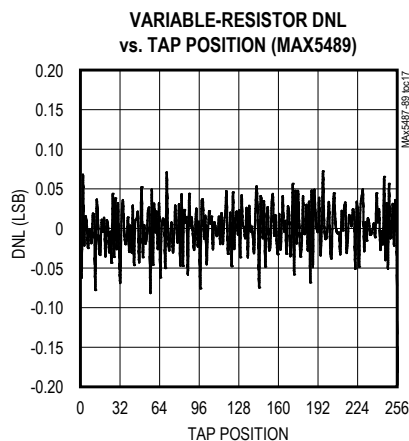


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Typical Operating Characteristics (continued)

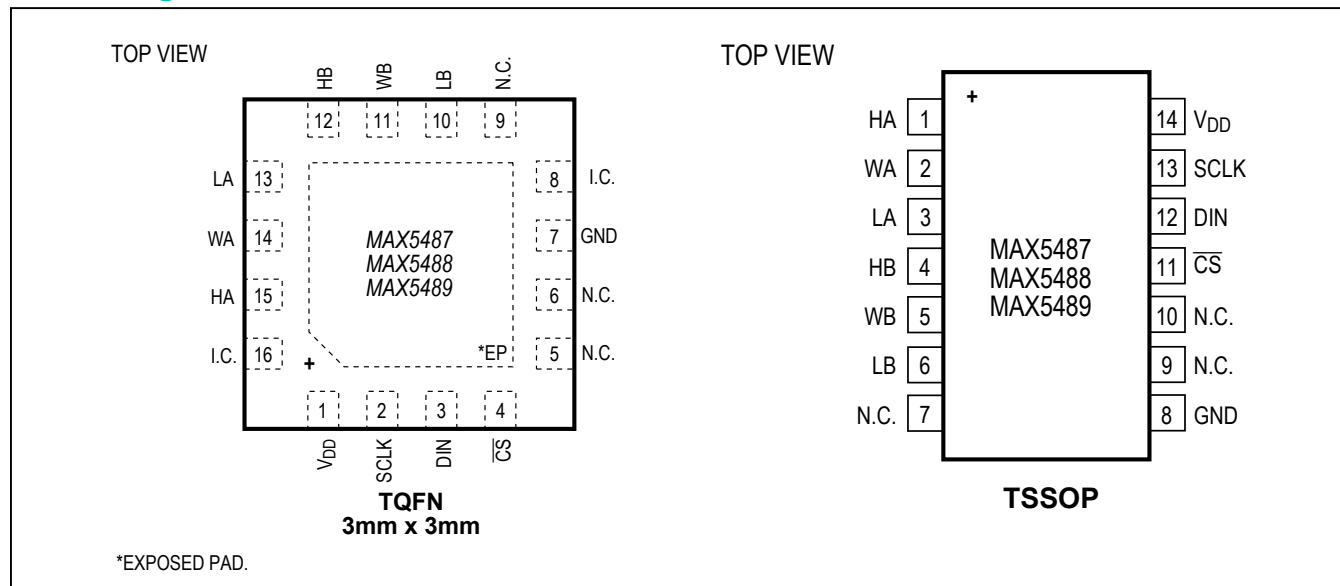
($V_{DD} = +5.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Configurations



Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	14	V _{DD}	Power Supply. Bypass V _{DD} to GND with a 0.1μF capacitor as close to the device as possible.
2	13	SCLK	Serial-Interface Clock Input
3	12	DIN	Serial-Interface Data Input
4	11	CS	Active-Low Chip-Select Digital Input
5, 6, 9	7, 9, 10	N.C.	No Connection. Not internally connected.
7	8	GND	Ground
8, 16	—	I.C.	Internally connected to EP. Leave unconnected.
10	6	LB	Low Terminal of Resistor B. The voltage at L can be greater than or less than the voltage at H. Current can flow into or out of L.
11	5	WB	Wiper Terminal of Resistor B
12	4	HB	High Terminal of Resistor B. The voltage at H can be greater than or less than the voltage at L. Current can flow into or out of H.
13	3	LA	Low Terminal of Resistor A. The voltage at L can be greater than or less than the voltage at H. Current can flow into or out of L.
14	2	WA	Wiper Terminal of Resistor A
15	1	HA	High Terminal of Resistor A. The voltage at H can be greater than or less than the voltage at L. Current can flow into or out of H.
—	—	EP	Exposed Pad (TQFN only). Internally connected to pins 8 and 16. Leave unconnected.

Detailed Description

The MAX5487/MAX5488/MAX5489 contain two resistor arrays, with 255 resistive elements each. The MAX5487 has an end-to-end resistance of 10k Ω , while the MAX5488 and MAX5489 have resistances of 50k Ω and 100k Ω , respectively. These devices allow access to the high, low, and wiper terminals on both potentiometers for a standard voltage-divider configuration. Connect the wiper to the high terminal, and connect the low terminal to ground, to make the device a variable resistor (see [Figure 1](#)).

A simple 3-wire serial interface programs either wiper directly to any of the 256 tap points. The nonvolatile memory stores the wiper position prior to power-down and recalls the wiper to the same point upon power-up or by using an interface command (see [Table 1](#)). The nonvolatile memory is guaranteed for 200,000 wiper store cycles and 50 years for wiper data retention.

SPI Digital Interface

These devices use a 3-wire SPI-compatible serial data interface ([Figure 2](#) and [Figure 3](#)). This write-only interface contains three inputs: chip-select (\overline{CS}), data clock (SCLK), and data in (DIN). Drive \overline{CS} low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge.

The WRITE commands (C1, C0 = 00 or 01) require 16 clock cycles to clock in the command, address, and data ([Figure 3a](#)). The COPY commands (C1, C0 = 10, 11) can use either eight clock cycles to transfer only command and address bits ([Figure 3b](#)) or 16 clock cycles, with the device disregarding 8 data bits ([Figure 3a](#)).

After loading data into the shift register, drive \overline{CS} high to latch the data into the appropriate potentiometer control register and disable the serial interface. Keep \overline{CS} low during the entire serial data stream to avoid corruption of the data.

Digital-Interface Format

The data format consists of three elements: command bits, address bits, and data bits (see [Table 1](#) and [Figure 3](#)). The command bits (C1 and C0) indicate the action to be taken such as changing or storing the wiper position. The address bits (A1 and A0) specify which potentiometer the command affects and the 8 data bits (D7 to D0) specify the wiper position.

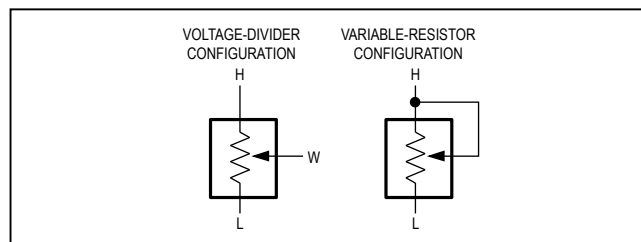


Figure 1. Voltage-Divider/Variable-Resistor Configurations

Table 1. Register Map

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	—	—	C1	C0	—	—	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register A	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register B	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register A	0	0	0	1	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register B	0	0	0	1	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Copy Wiper Register A to NV Register A	0	0	1	0	0	0	0	1	—	—	—	—	—	—	—	—
Copy Wiper Register B to NV Register B	0	0	1	0	0	0	1	0	—	—	—	—	—	—	—	—
Copy Both Wiper Registers to NV Registers	0	0	1	0	0	0	1	1	—	—	—	—	—	—	—	—
Copy NV Register A to Wiper Register A	0	0	1	1	0	0	0	1	—	—	—	—	—	—	—	—
Copy NV Register B to Wiper Register B	0	0	1	1	0	0	1	0	—	—	—	—	—	—	—	—
Copy Both NV Registers to Wiper Registers	0	0	1	1	0	0	1	1	—	—	—	—	—	—	—	—

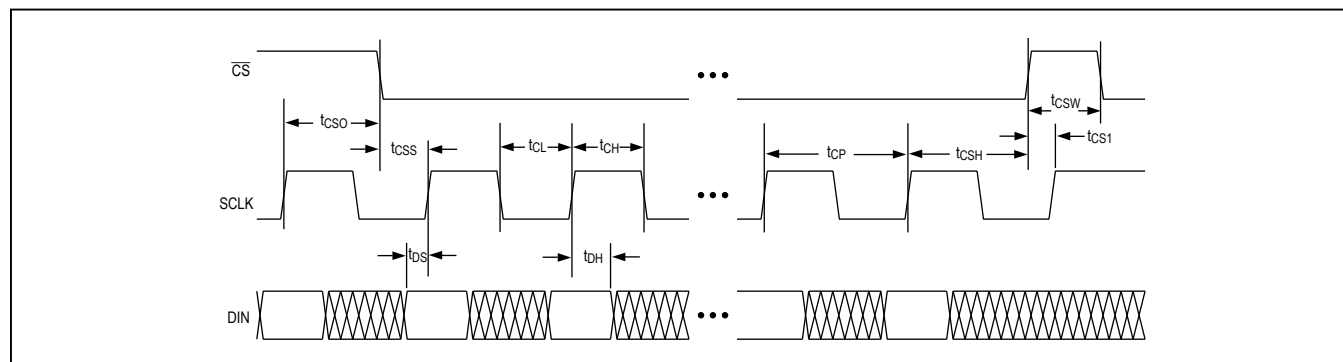


Figure 2. Timing Diagram

Write-Wiper Register (Command 00)

Data written to the write-wiper registers (C1, C0 = 00) controls the wiper positions. The 8 data bits (D7 to D0) indicate the position of the wiper. For example, if DIN = 0000 0000, the wiper moves to the position closest to L₋. If DIN = 1111 1111, the wiper moves closest to H₋.

This command writes data to the volatile RAM, leaving the NV registers unchanged. When the device powers up, the data stored in the NV registers transfers to the volatile wiper register, moving the wiper to the stored position.

Write-NV Register (Command 01)

This command (C1, C0 = 01) stores the position of the wipers to the NV registers for use at power-up. Alternatively, the “copy wiper register to NV register” command can be used to store the position of the wipers to the NV registers. Writing to the NV registers does not affect the position of the wipers.

Copy Wiper Register to NV Register (Command 10)

This command (C1, C0 = 10) stores the current position of the wiper to the NV register, for use at power-up. This command may affect one potentiometer at a time,

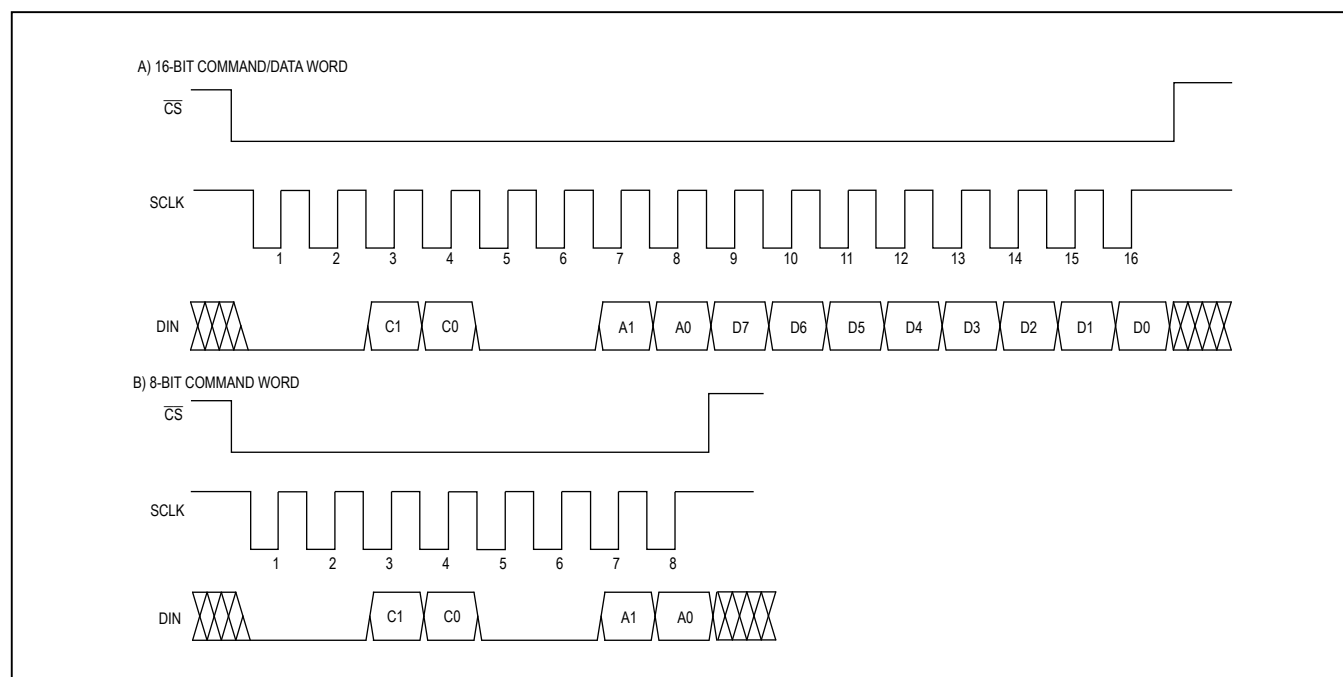


Figure 3. Digital-Interface Format

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or both simultaneously, depending on the state of A1 and A0. Alternatively, the “write NV register” command can be used to store the current position of the wiper to the NV register.

Copy NV Register to Wiper Register (Command 11)

This command (C1, C0 = 11) restores the wiper position to the previously stored position in the NV register. This command may affect one potentiometer at a time, or both simultaneously, depending on the state of A1 and A0.

Nonvolatile Memory

The internal EEPROM consists of a nonvolatile register that retains the last stored value prior to power-down. The nonvolatile register is programmed to midscale at the factory. The nonvolatile memory is guaranteed for 200,000 wiper write cycles and 50 years for wiper data retention.

Power-Up

Upon power-up, these devices load the data stored in the nonvolatile wiper register into the volatile memory register, updating the wiper position with the data stored in the nonvolatile wiper register. This initialization period takes 5 μ s.

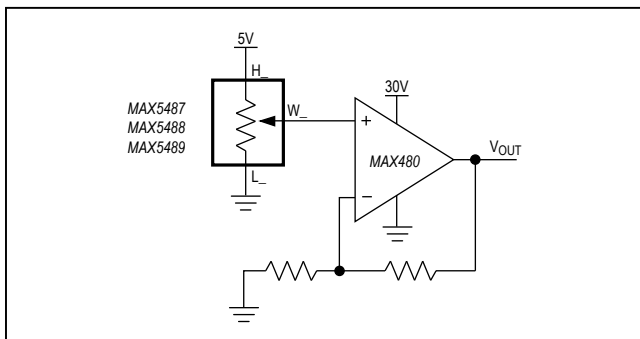


Figure 4. Positive LCD-Bias Control Using a Voltage-Divider

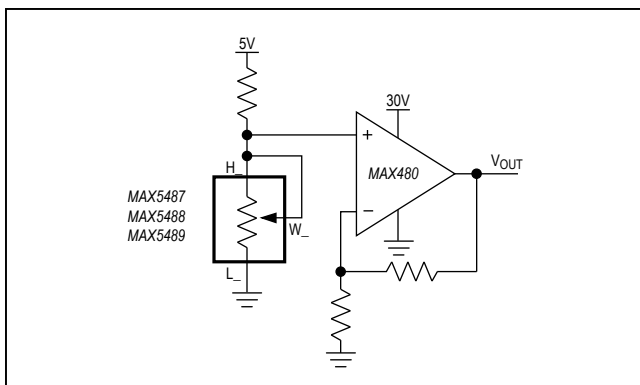


Figure 5. Positive LCD-Bias Control Using a Variable Resistor

Standby

The MAX5487/MAX5488/MAX5489 feature a low-power standby mode. When the device is not being programmed, it enters into standby mode and supply current drops to 0.5 μ A (typ).

Applications Information

The MAX5487/MAX5488/MAX5489 are ideal for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or for programmable filters with adjustable gain and/or cutoff frequency.

Positive LCD Bias Control

Figure 4 and Figure 5 show an application where the devices provide an adjustable, positive LCD-bias voltage. The op amp provides buffering and gain to the resistor-divider network made by the potentiometer (Figure 4) or by a fixed resistor and a variable resistor (Figure 5).

Programmable Filter

Figure 6 shows the MAX5487/MAX5488/MAX5489 in a 1st-order programmable-filter application. Adjust the gain of the filter with R₂, and set the cutoff frequency with R₃.

Use the following equations to calculate the gain (A) and the -3dB cutoff frequency (f_C)

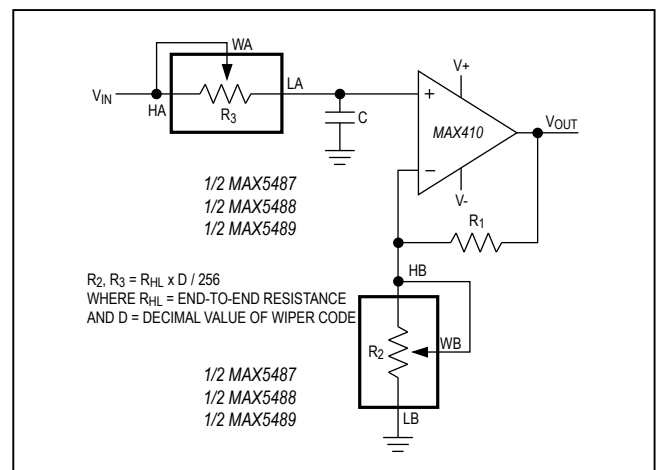


Figure 6. Programmable Filter

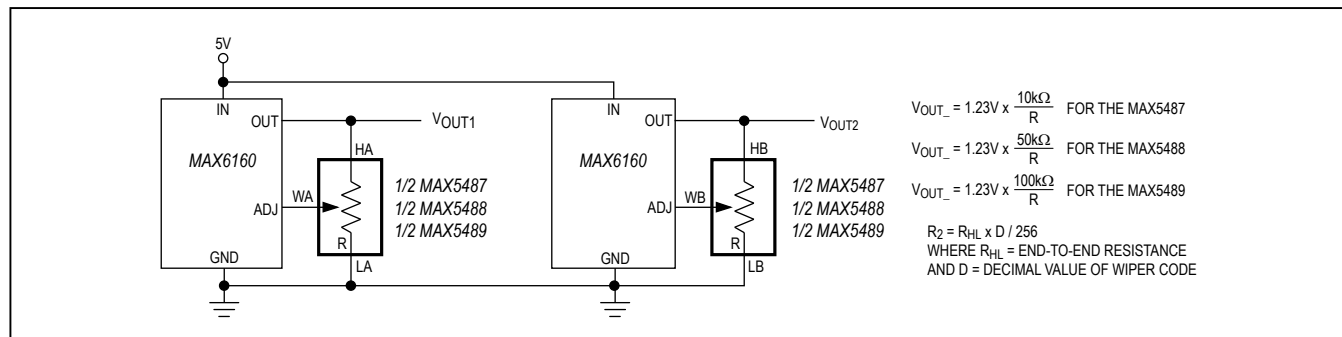


Figure 7. Adjustable Voltage Reference

$$A = 1 + \frac{R_1}{R_2}$$

$$f_C = \frac{1}{2\pi \times R_3 \times C}$$

Adjustable Voltage Reference

Figure 7 shows the devices used as the feedback resistors in multiple adjustable voltage-reference applications. Independently adjust the output voltages of the MAX6160s from 1.23V to $V_{IN} - 0.2V$ by changing the wiper positions of the MAX5487/MAX5488/MAX5489.

Offset Voltage and Gain Adjustment

Connect the high and low terminals of one potentiometer of a MAX5487/MAX5488/MAX5489 to the NULL inputs of a MAX410, and connect the wiper to the op amp's positive supply to nullify the offset voltage over the operating temperature range. Install the other potentiometer in the feedback path to adjust the gain of the MAX410 (see **Figure 8**).

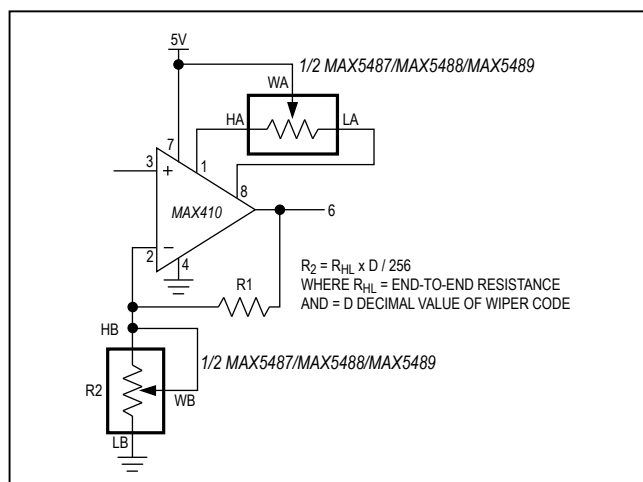


Figure 8. Offset Voltage and Gain Adjustment

MAX5487/MAX5488/ MAX5489

Dual, 256-Tap, Nonvolatile, SPI-Interface,
Linear-Taper Digital Potentiometers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	END-TO-END RESISTANCE (k Ω)	TOP MARK
MAX5487 ETE+	-40°C to +85°C	16 TQFN-EP*	10	ABR
MAX5487EUD+	-40°C to +85°C	14 TSSOP	10	—
MAX5488 ETE+	-40°C to +85°C	16 TQFN-EP*	50	ABS
MAX5488EUD+	-40°C to +85°C	14 TSSOP	50	—
MAX5489 ETE+	-40°C to +85°C	16 TQFN-EP*	100	ABT
MAX5489EUD+	-40°C to +85°C	14 TSSOP	100	—
MAX5489ETE/V+	-40°C to +85°C	16 TQFN-EP*	100	AIE

*EP = Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633F+3	21-0036	90-0033
14 TSSOP	U14+1	21-0066	90-0113

Chip Information

PROCESS: BiCMOS

MAX5487/MAX5488/
MAX5489

Dual, 256-Tap, Nonvolatile, SPI-Interface,
Linear-Taper Digital Potentiometers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	1/07	—	1, 8, 12, 15
4	4/10	Updated <i>Ordering Information</i> (added lead-free packaging and automotive qualified part, released TSSOP package), and updated <i>Absolute Maximum Ratings</i>	1, 2, 12

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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