

High-Speed, Low-Voltage, 4 Ω , SPDT CMOS Analog Switch

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

| | |
|---|----------------------|
| V+ | -0.3V to +6V |
| IN, COM, NO, NC (Note 1) | -0.3V to (V+ + 0.3V) |
| Continuous Current (any terminal) | $\pm 20\text{mA}$ |
| Continuous Current (NO, NC, and COM) | $\pm 50\text{mA}$ |
| Peak Current (NO, NC, and COM, pulsed at 1ms, 10% duty cycle) | $\pm 100\text{mA}$ |

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

| | |
|---|---|
| 6-Pin SOT23 (derate 8.70mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) | 696mW |
| 8-Pin μMAX (derate 4.5mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) | 362mW |
| Operating Temperature Range | -40°C to $+85^\circ\text{C}$ |
| Junction Temperature | $+150^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (soldering, 10s) | $+300^\circ\text{C}$ |
| Soldering Temperature (reflow) | $+260^\circ\text{C}$ |

Note 1: Signals on NO, NC, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, $V_{\text{INH}} = 2.4\text{V}$, $V_{\text{INL}} = 0.8\text{V}$, $T_A = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|--|---|---|-------|-------|------|-------|
| ANALOG SWITCH | | | | | | | |
| Analog-Signal Range | V _{COM} , V _{NO} , V _{NC} | | | 0 | | V+ | V |
| On-Resistance | R _{ON} | V+ = 4.5V, I _{COM} = 10mA, V _{NO} or V _{NC} = 0 to V+ | T _A = +25°C | 2.5 | | 4 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | | 4.75 | |
| On-Resistance Match Between Channels (Note 2) | ΔR _{ON} | V+ = 4.5V, I _{COM} = 10mA, V _{NO} or V _{NC} = 0 to V+ | T _A = +25°C | 0.1 | | | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | | 0.4 | |
| On-Resistance Flatness (Note 3) | R _{FLAT} | V+ = 4.5V, I _{COM} = 10mA, V _{NO} or V _{NC} = 0 to V+ | T _A = +25°C | 0.75 | | 1 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | | 1.2 | |
| NO, NC Off-Leakage Current (Note 4) | I _{NO(OFF)} , I _{NC(OFF)} | V+ = 5.5V, V _{COM} = 1V or 4.5V, V _{NO} or V _{NC} = 4.5V or 1V | T _A = +25°C | -0.25 | 0.01 | 0.25 | nA |
| | | | T _A = T _{MIN} to T _{MAX} | -0.35 | | 0.35 | |
| COM Off-Leakage Current (Note 4) | I _{COM(OFF)} | V+ = 5.5V, V _{COM} = 1V or 4.5V, V _{NO} or V _{NC} = 4.5V or 1V | T _A = +25°C | -0.25 | 0.01 | 0.25 | nA |
| | | | T _A = T _{MIN} to T _{MAX} | -0.35 | | 0.35 | |
| COM On-Leakage Current (Notes 4, 5) | I _{COM(ON)} | V+ = 5.5V, V _{COM} = 1V or 4.5V | T _A = +25°C | -0.25 | 0.01 | 0.25 | nA |
| | | | T _A = T _{MIN} to T _{MAX} | -0.35 | | 0.35 | |
| DIGITAL INPUTS | | | | | | | |
| Input-Logic High | V _{IH} | | | 2.4 | | | V |
| Input-Logic Low | V _{IL} | | | | | 0.8 | V |
| Input Current | I _{IN} | V _{IN} = 0.8V or 2.4V | | -0.1 | 0.005 | 0.1 | μA |

High-Speed, Low-Voltage, 4Ω, SPDT CMOS Analog Switch

ELECTRICAL CHARACTERISTICS — Single +5V Supply (continued)

(V₊ = +4.5V to +5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|---|--|---|-------|-----|-------|
| DYNAMIC | | | | | | |
| Turn-On Time (Note 4) | t _{ON} | R _L = 300Ω; C _L = 35pF; V _{NO} , V _{NC} = 3V; Figure 2 | T _A = +25°C | 11 | 15 | ns |
| | | | T _A = T _{MIN} to T _{MAX} | | 18 | |
| Turn-Off Time (Note 4) | t _{OFF} | R _L = 300Ω; C _L = 35pF; V _{NO} , V _{NC} = 3V; Figure 2 | T _A = +25°C | 3 | 5 | ns |
| | | | T _A = T _{MIN} to T _{MAX} | | 6 | |
| Break-Before-Make (Note 4) | t _{BBM} | R _L = 300Ω; C _L = 35pF; V _{NO} or V _{NC} = +3V; Figure 2 | T _A = +25°C | 8 | | ns |
| | | | T _A = T _{MIN} to T _{MAX} | 1 | | |
| Charge Injection | Q | V _{GEN} = 0V, R _{GEN} = 0V, C _L = 1nF, Figure 4 | | 5 | | pC |
| NO, NC Off-Capacitance | C _{NO(OFF)} , C _{NC(OFF)} | NO or NC = GND, f = 1MHz, Figure 5 | | 12 | | pF |
| Switch On-Capacitance | C _(ON) | f = 1MHz, Figure 5 | | 34 | | pF |
| Off-Isolation (Note 6) | V _{ISO} | C _L = 5pF, R _L = 50Ω, Figure 3 | f = 10MHz | -55 | | dB |
| | | | f = 1MHz | -80 | | |
| Crosstalk (Note 7) | V _{CT} | C _L = 5pF, R _L = 50Ω, Figure 3 | f = 10MHz | -62 | | dB |
| | | | f = 1MHz | -82 | | |
| Total Harmonic Distortion | THD | R _L = 600Ω, 0.5Vp-p, f = 20Hz to 20kHz | | 0.018 | | % |
| SUPPLY | | | | | | |
| Positive Supply Current | I ₊ | V ₊ = 5.5V, V _{IN} = 0V or V ₊ | | 0.001 | 1.0 | μA |

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V₊ = +2.7V to +3.3V, V_{INH} = 2.0V, V_{INL} = 0.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|--|---|-----|----------------|-------|
| ANALOG SWITCH | | | | | | |
| Analog-Signal Range | V _{COM} , V _{NO} , V _{NC} | | 0 | | V ₊ | V |
| On-Resistance | R _{ON} | V ₊ = 2.7V, I _{COM} = 10mA, V _{NO} or V _{NC} = 0 to V ₊ | T _A = +25°C | 6 | 8 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 9 | |
| On-Resistance Match Between Channels (Note 2) | ΔR _{ON} | V ₊ = 2.7V, I _{COM} = 10mA, V _{NO} or V _{NC} = 0 to V ₊ | T _A = +25°C | 0.1 | | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 0.4 | |
| On-Resistance Flatness (Note 3) | R _{FLAT} | V ₊ = 2.7V, I _{COM} = 10mA, V _{NO} or V _{NC} = 0 to V ₊ | T _A = +25°C | 1.5 | 3 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 3.5 | |

High-Speed, Low-Voltage, 4Ω, SPDT CMOS Analog Switch

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.3V, V_{INH} = 2.0V, V_{INL} = 0.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|----------------------------|---|--|---|-------|-------|-----|-------|
| DIGITAL INPUTS | | | | | | | |
| Input-Logic High | V _{IH} | | | 2.0 | | | V |
| Input-Logic Low | V _{IL} | | | | | 0.4 | V |
| Input Current | I _{IN} | V _{IN} = 0.4V or 2.0V | | -0.1 | 0.005 | 0.1 | μA |
| DYNAMIC | | | | | | | |
| Turn-On Time (Note 4) | t _{ON} | R _L = 300Ω; C _L = 35pF; V _{NO} , V _{NC} = 2V; Figure 2 | T _A = +25°C | 14 | 20 | ns | |
| | | | T _A = T _{MIN} to T _{MAX} | 22 | | | |
| Turn-Off Time (Note 4) | t _{OFF} | R _L = 300Ω; C _L = 35pF; V _{NO} , V _{NC} = 2V; Figure 2 | T _A = +25°C | 4 | 7.5 | ns | |
| | | | T _A = T _{MIN} to T _{MAX} | 8 | | | |
| Break-Before-Make (Note 4) | t _{BBM} | R _L = 300Ω; C _L = 35pF; V _{NO} , V _{NC} = 2V; Figure 2 | T _A = +25°C | 8 | | ns | |
| | | | T _A = T _{MIN} to T _{MAX} | 1 | | | |
| Charge Injection | Q | V _{GEN} = 0V, R _{GEN} = 0V, C _L = 1nF, Figure 4 | | 5 | | pC | |
| NO, NC Off-Capacitance | C _{NO(OFF)} , C _{NC(OFF)} | NO or NC = GND, f = 1MHz, Figure 5 | | 12 | | pF | |
| Switch On-Capacitance | C _(ON) | f = 1MHz, Figure 5 | | 34 | | pF | |
| Off-Isolation (Note 6) | V _{ISO} | C _L = 5pF, R _L = 50Ω, Figure 3 | f = 10MHz | -55 | | dB | |
| | | | f = 1MHz | -80 | | | |
| Crosstalk (Note 7) | V _{CT} | C _L = 5pF, R _L = 50Ω, Figure 3 | f = 10MHz | -62 | | dB | |
| | | | f = 1MHz | -82 | | | |
| SUPPLY | | | | | | | |
| Positive Supply Current | I ₊ | V ₊ = 3.3V, V _{IN} = 0V or V ₊ | | 0.001 | | 1.0 | μA |

Note 2: ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)}.

Note 3: R_{ON} flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog-signal range.

Note 4: Guaranteed by design.

Note 5: On-Leakage performed with voltage applied to COM, with NO and NC left unconnected.

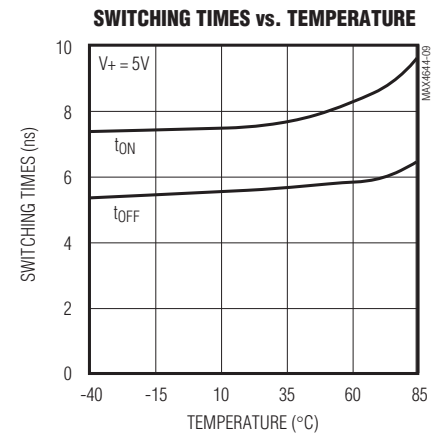
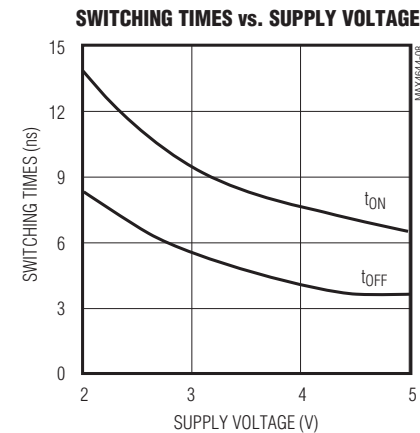
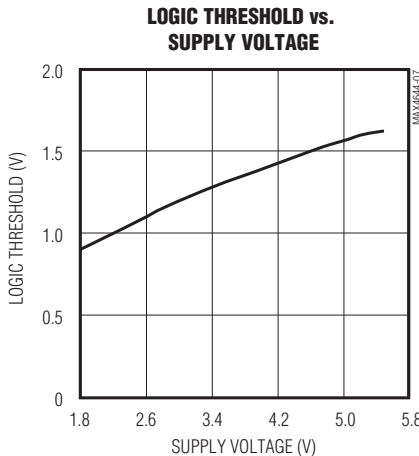
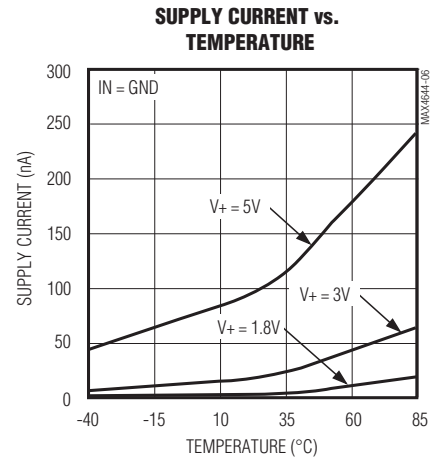
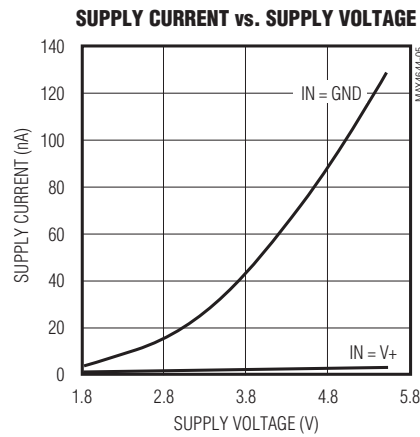
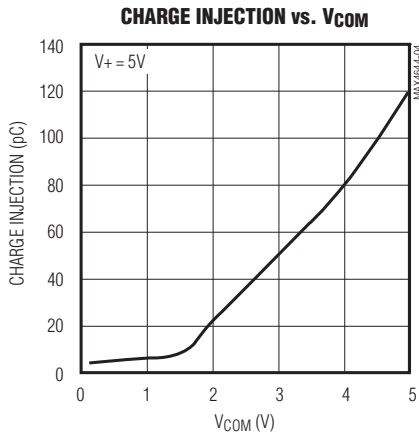
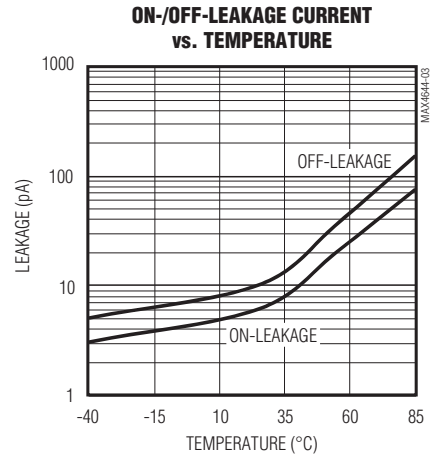
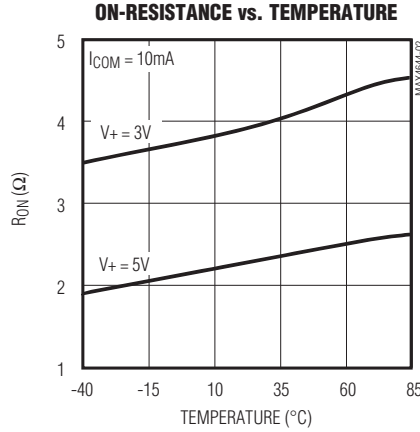
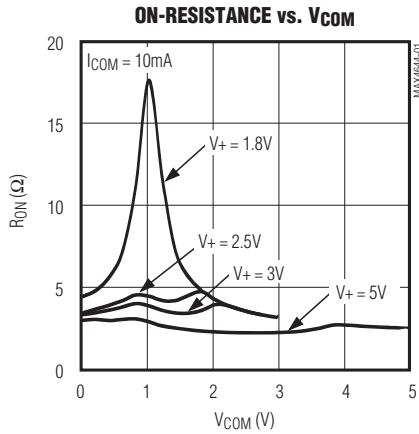
Note 6: Off-Isolation = 20log₁₀ (V_O / V_I), where V_O is V_{COM} and V_I is either V_{NC} or V_{NO} from the network analyzer.

Note 7: Crosstalk is measured between the two switches.

High-Speed, Low-Voltage, 4Ω , SPDT CMOS Analog Switch

Typical Operating Characteristics

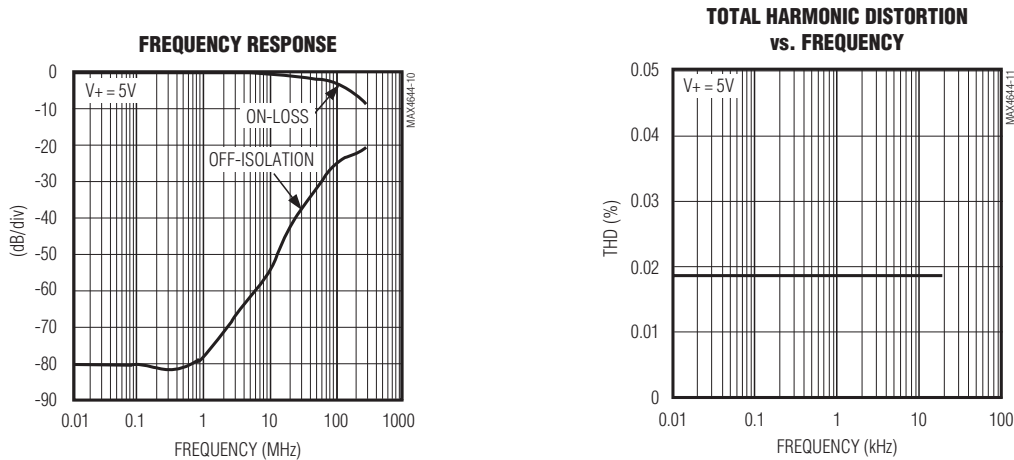
($V_+ = +5V$ or $+3V$, $V_{INH} = V_+$, $INL = GND$, $T_A = +25^\circ C$, unless otherwise noted.)



High-Speed, Low-Voltage, 4Ω, SPDT CMOS Analog Switch

Typical Operating Characteristics (continued)

(V+ = +5V or +3V, VINH = V+, INL = GND, TA = +25°C, unless otherwise noted.)



Pin Description

| MAX4644 | | NAME | FUNCTION |
|---------|------|------|--|
| SOT23 | μMAX | | |
| 1 | 6 | IN | Logic-Controlled Input |
| 2 | 4 | V+ | Positive Supply Voltage Input. Bypass with a 0.1μF capacitor to GND. |
| 3 | 3 | GND | Ground |
| — | 5, 7 | N.C. | No Connection. Not internally connected. |
| 4 | 2 | NC | Analog-Switch Normally Closed Terminal |
| 5 | 1 | COM | Analog-Switch Common Terminal |
| 6 | 8 | NO | Analog-Switch Normally Open Terminal |

Note: The switches are bidirectional, which means that a signal can be passed through either side of the on switch. However, the typical off-capacitances differ as shown in the *Electrical Characteristics*.

High-Speed, Low-Voltage, 4Ω, SPDT CMOS Analog Switch

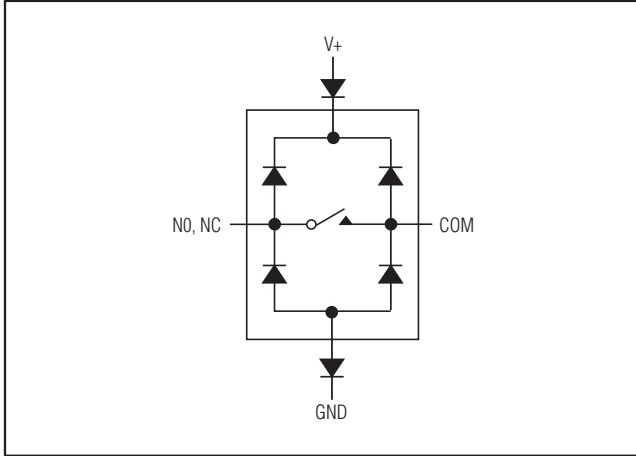


Figure 1. Overvoltage Protection Using External Blocking Diodes

Applications Information

The MAX4644 operates from a single supply ranging from +1.8V to +5.5V. The device is guaranteed to be functional over that supply range, but TTL/CMOS compatibility is only valid for operation using a +5V supply. All voltage levels are referenced to GND. Positive and negative DC analog inputs or AC signals can be accommodated by shifting V+ and GND.

ESD-protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND (Figure 1). Virtually all of the analog leakage current comes from the ESD diodes to V+

or GND. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no normal current path between the analog-signal paths and V+ or GND. V+ and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic level into switched V+ and GND signals to drive the analog signal gates.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 6 SOT23 | U6+4 | 21-0058 | 90-0175 |
| 8 μMAX | U8+1 | 21-0036 | 90-0092 |

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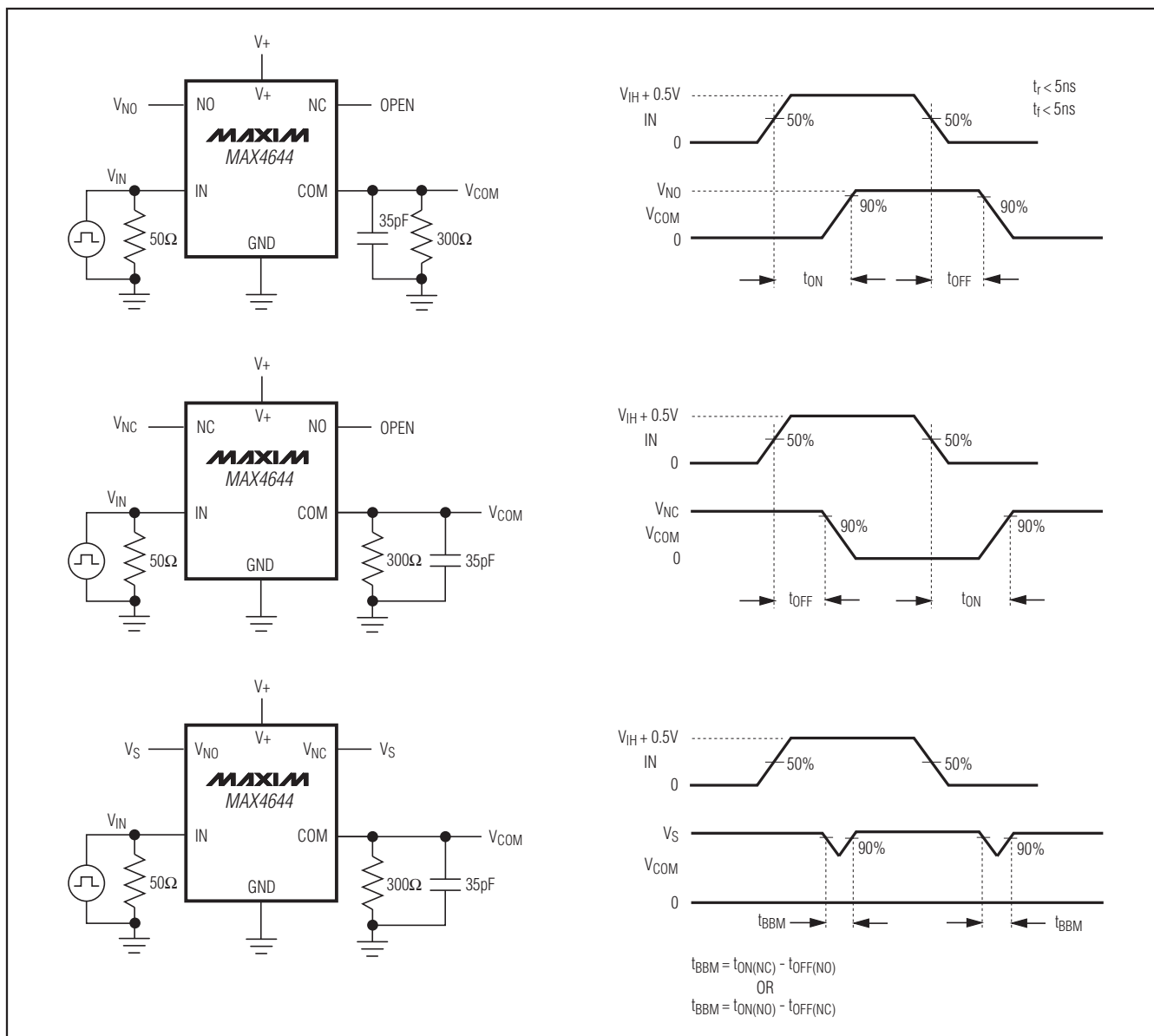


Figure 2. Switching Times

High-Speed, Low-Voltage, 4Ω, SPDT CMOS Analog Switch

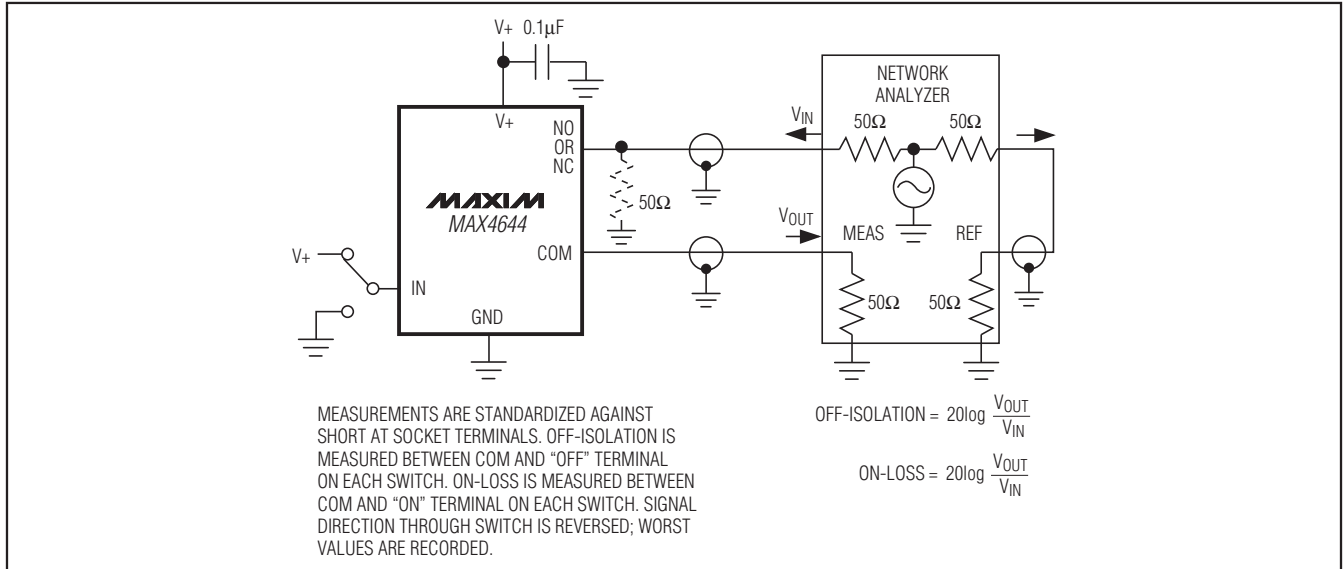


Figure 3. Off-Isolation and On-Loss

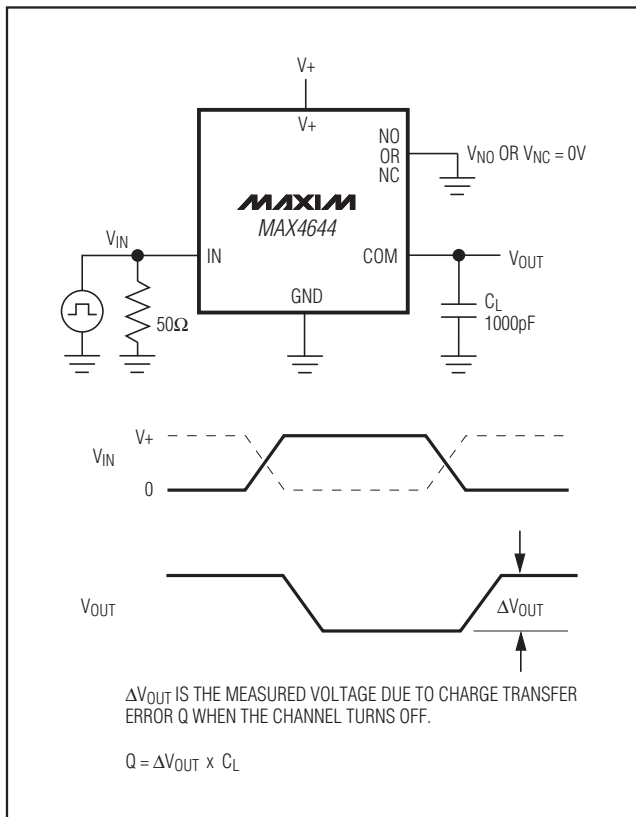


Figure 4. Charge Injection

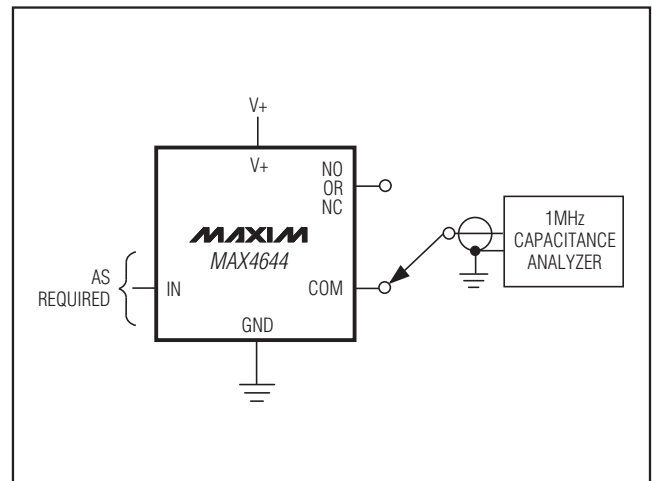


Figure 5. NO, NC, and COM Capacitance

High-Speed, Low-Voltage, 4Ω, SPDT CMOS Analog Switch

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|------------------|--|------------------|
| 0 | 3/00 | Initial release | — |
| 1 | 1/11 | Added lead-free parts to the <i>Ordering Information</i> table | 1 |

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