Serially Controlled Audio/Video Switches

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +6V
COM_ and NO_ _ to GND (Note 1) .....-0.3V to (V+ + 0.3V)
A, CS, SDA, DIN, SCL, and SCLK to GND.....-0.3V to +6V
Continuous Current into Any Terminal.....±20mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle).....±40mA
ESD per Method 3015.7.....>2kV

Continuous Power Dissipation (T_A = +70°C)
µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Signals on NO_ _ or COM_ exceeding V+ or ground are clamped by internal diodes. Limit forward-diode current to maximum current rating.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCHES							
Analog Signal Range (Note 3)	$V_{NO\_\_}$, $V_{COM\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 4.75V, $V_{NO\_\_}$ = 3V, $I_{COM\_}$ = 4mA	T_A = +25°C		45	65	Ω
			T_A = T_{MIN} to T_{MAX}			80	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 4.75V, $V_{NO\_\_}$ = 3V, $I_{COM\_}$ = 4mA	T_A = +25°C		2	4	Ω
			T_A = T_{MIN} to T_{MAX}			5	
On-Resistance Flatness (Note 5)	R_{FLAT}	V+ = 4.75V; $V_{NO\_\_}$ = 1V, 2V, 3V; $I_{COM\_}$ = 4mA	T_A = +25°C		2	5	Ω
			T_A = T_{MIN} to T_{MAX}			6.5	
NO_ _ Off-Leakage Current (Note 6)	$I_{NO\_\_(OFF)}$	V+ = 5.25V; $V_{NO\_\_}$ = 1V, 4.5V; $V_{COM\_}$ = 4.5V, 1V	T_A = +25°C	-1	0.001	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ Off-Leakage Current (Note 6)	$I_{COM\_(OFF)}$	V+ = 5.25V; $V_{NO\_\_}$ = 1V, 4.5V; $V_{COM\_}$ = 4.5V, 1V	T_A = +25°C	-1	0.001	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ On-Leakage Current (Note 6)	$I_{COM\_(ON)}$	V+ = 5.25V; $V_{NO\_\_}$ = 1V, 4.5V, or floating; $V_{COM\_}$ = 1V, 4.5V	T_A = +25°C	-1	0.002	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
AUDIO PERFORMANCE							
Off-Isolation (Note 7)	$V_{ISO(A)}$	V_A = $1V_{RMS}$, f_{IN} = 20kHz, R_L = 600Ω, Figure 8			-83		dB
Channel-to-Channel Crosstalk	$V_{CT(A)}$	V_A = $1V_{RMS}$, f_{IN} = 20kHz, R_S = 600Ω, Figure 8			-84		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VIDEO PERFORMANCE							
Off-Isolation (Note 7)	$V_{ISO(V)}$	V_A = $1V_{RMS}$, f_{IN} = 10MHz, R_L = 50Ω, Figure 8			-48		dB
Channel-to-Channel Crosstalk	$V_{CT(V)}$	V_A = $1V_{RMS}$, f_{IN} = 10MHz, R_S = 50Ω, Figure 8			-60		dB
-0.1dB Bandwidth	BW	R_S = 75Ω, R_L = 1kΩ			5		MHz
-3dB Bandwidth	BW	R_S = 50Ω, R_L = 50Ω			300		MHz
NO_ _ Off-Capacitance	C_{OFF}	f_{IN} = 1MHz			5		pF
DYNAMIC TIMING (Notes, 8, 11, and Figure 5)							
Turn-On Time	t_{ON}	$V_{NO\_\_}$ = 2.5V, C_L = 35pF, R_L = 5kΩ	T_A = +25°C		275	400	ns
			T_A = T_{MIN} to T_{MAX}			500	
Turn-Off Time	t_{OFF}	$V_{NO\_\_}$ = 2.5V, C_L = 35pF, R_L = 300Ω	T_A = +25°C		125	200	ns
			T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Time	t_{BBM}	$V_{NO\_\_}$ = 2.5V, Figure 6		10	50		ns
Charge Injection	Q	C_L = 1.0nF, V_S = 0, R_S = 0, Figure 7			3		pC
POWER SUPPLY							
Power-Supply Voltage Range	V+			2.7		5.5	V
Supply Current	I+	All logic inputs = 0 or V+			5	10	µA

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCHES							
Analog Signal Range (Note 3)	$V_{NO\_\_}$, $V_{COM\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 2.7V, $V_{NO\_\_}$ = 1V, $I_{COM\_}$ = 4mA	T_A = +25°C		65	110	Ω
			T_A = T_{MIN} to T_{MAX}			130	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 2.7V, $V_{NO\_\_}$ = 1V, $I_{COM\_}$ = 4mA	T_A = +25°C		3	5	Ω
			T_A = T_{MIN} to T_{MAX}			6	
On-Resistance Flatness (Note 5)	R_{FLAT}	V+ = 2.7V; $V_{NO\_\_}$ = 1V, 1.5V, 2V; $I_{COM\_}$ = 4mA	T_A = +25°C		3	10	Ω
			T_A = T_{MIN} to T_{MAX}			12	
NO_ _ Off-Leakage Current (Notes 6, 9)	$I_{NO\_\_(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 0.5V, 3V; $V_{NO\_\_}$ = 3V, 0.5V	T_A = +25°C	-1	0.001	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ Off-Leakage Current (Notes 6, 9)	$I_{COM\_(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 0.5V, 3V; $V_{NO\_\_}$ = 3V, 0.5V	T_A = +25°C	-1	0.001	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM _ On-Leakage Current (Notes 6, 9)	$I_{COM\_(ON)}$	V+ = 3.6V; $V_{COM\_}$ = 0.5V, 3V; $V_{NO\_\_}$ = 0.5V, 3V, or floating	T_A = +25°C	-1	0.002	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
AUDIO PERFORMANCE							
Off-Isolation (Note 7)	$V_{ISO(A)}$	V_A = 0.5V_{RMS}, f_{IN} = 20kHz, R_L = 600Ω, Figure 8			-83		dB
Channel-to-Channel Crosstalk	$V_{CT(A)}$	V_A = 0.5V_{RMS}, f_{IN} = 20kHz, R_S = 600Ω, Figure 8			-84		dB
VIDEO PERFORMANCE							
Off-Isolation	$V_{ISO(V)}$	V_A = 0.5V_{RMS}, f_{IN} = 10MHz, R_L = 50Ω, Figure 8			-48		dB
Channel-to-Channel Crosstalk	$V_{CT(V)}$	V_A = 0.5V_{RMS}, f_{IN} = 10MHz, R_S = 50Ω, Figure 8			-60		dB
-3dB Bandwidth	BW	R_S = 50Ω, R_L = 50Ω			200		MHz
NO_ _ Off-Capacitance	C_{OFF}	f_{IN} = 1MHz			5		pF
DYNAMIC TIMING (Notes 8, 11, and Figure 5)							
Turn-On Time	t_{ON}	$V_{NO\_\_}$ = 1.5V, R_L = 5kΩ, C_L = 35pF	T_A = +25°C		400	800	ns
			T_A = T_{MIN} to T_{MAX}			1000	
Turn-Off Time	t_{OFF}	$V_{NO\_\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF	T_A = +25°C		200	350	ns
			T_A = T_{MIN} to T_{MAX}			500	
Break-Before-Make Time	t_{BBM}	$V_{NO\_\_}$ = 1.5V, Figure 6		10	100		ns

I/O INTERFACE CHARACTERISTICS

(V+ = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, SCL, SDA, A)						
Input Low Voltage	V_{IL}	V+ = 5V			0.8	V
		V+ = 3V			0.6	
Input High Voltage	V_{IH}	V+ = 5V	3			V
		V+ = 3V	2			
Input Hysteresis	V_{HYST}			0.2		V
Input Leakage Current	I_{LEAK}	Digital inputs = 0 or V+	-1	0.01	1	µA
Input Capacitance	C_{IN}			5		pF
DIGITAL OUTPUT (SDA)						
Output Low Voltage	V_{OL}	I_{SINK} = 6mA			0.4	V

2-WIRE TIMING CHARACTERISTICS

(Figures 1 and 2, V+ = +2.7V to +5.25V, f_{SCL} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	V+ = 2.7V to 5.25V	0		100	kHz
		V+ = 4.75V to 5.25V			400	
Bus Free Time Between Stop and Start Conditions	t_{BUF}		4.7			µs
Hold Time After Start Condition	$t_{HD:STA}$	The first clock is generated after this period.	4.0			µs
Stop Condition Setup Time	$t_{SU:STO}$		4.0			µs
Data Hold Time	$t_{HD:DAT}$		0			µs
Data Setup Time	$t_{SU:DAT}$		250			ns
Clock Low Period	t_{LOW}		4.7			µs
Clock High Period	t_{HIGH}		4.0			µs
SCL/SDA Rise Time (Note 10)	t_R		20 + 0.1C_B		300	ns
SCL/SDA Fall Time (Note 10)	t_F		20 + 0.1C_B		300	ns

3-WIRE TIMING CHARACTERISTICS

(Figures 3 and 4, V+ = +2.75V to +5.25V, f_{OP} = 2.1MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

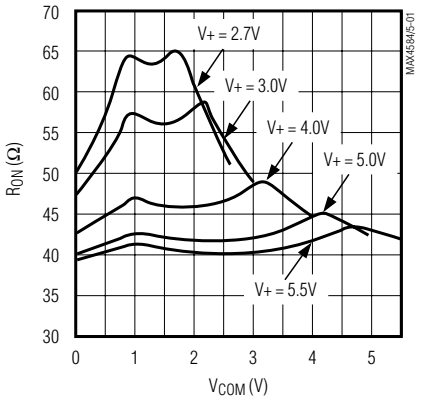
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{OP}	V+ = 2.7V to 5.25V	0		2.1	MHz
		V+ = 4.75V to 5.25V			10	
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ Rise to SCLK Hold	t_{CSH}		0			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Pulse Width High	t_{CH}		200			ns
Rise Time (SCLK, DIN, $\overline{CS}$)	t_R				2	µs
Fall Time (SCLK, DIN, $\overline{CS}$)	t_F				2	µs
$\overline{CS}$ Pulse Width High	t_{CSW}			40		ns

Note 2: Algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design. Not subject to production testing.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and minimum on-resistance values, as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum rated temperature and guaranteed by correlation at T_A = +25°C.
Note 7: Off-isolation = 20 log ($V_{COM\_}$ / $V_{NO\_\_}$), $V_{COM\_}$ = output, $V_{NO\_\_}$ = input to off switch.
Note 8: All timing is measured from the clock's falling edge preceding the ACK signal for 2-wire and from the rising edge of $\overline{CS}$ for 3-wire. Turn-off time is defined at the output of the switch for a 0.5V change, tested with a 300Ω load to ground. Turn-on time is defined at the output of the switch for a 0.5V change and measured with a 5kΩ load resistor to GND. All timing is shown with respect to 20% V+ and 70% V+, unless otherwise noted.
Note 9: Leakage testing is guaranteed by testing with a +5.25V supply.
Note 10: C_B = capacitance of one bus line in pF. Tested with C_B = 400pF.
Note 11: Typical values are for MAX4584 devices.

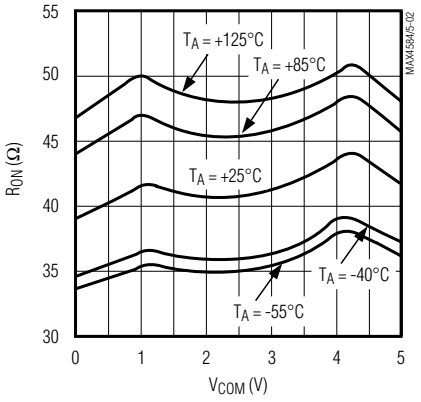
Typical Operating Characteristics

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

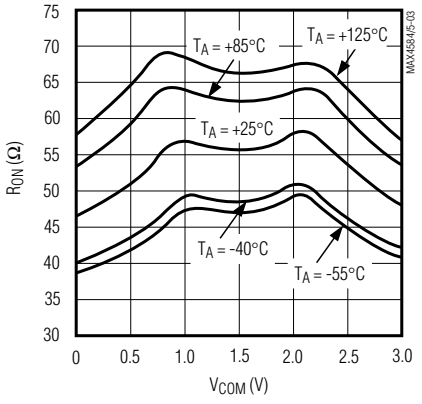
ON-RESISTANCE vs. V_{COM} AND SUPPLY VOLTAGE



ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (V+ = 5V)



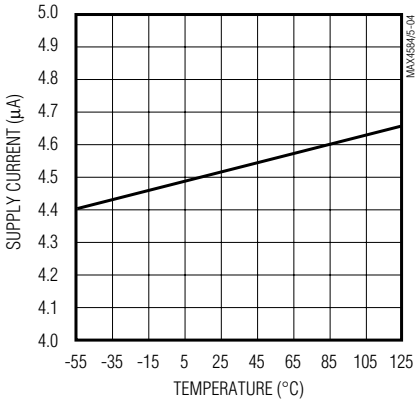
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (V+ = 3.3V)



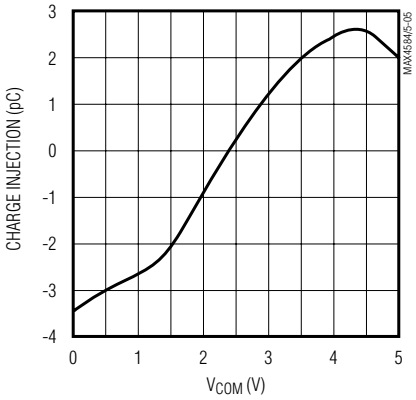
Typical Operating Characteristics (continued)

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

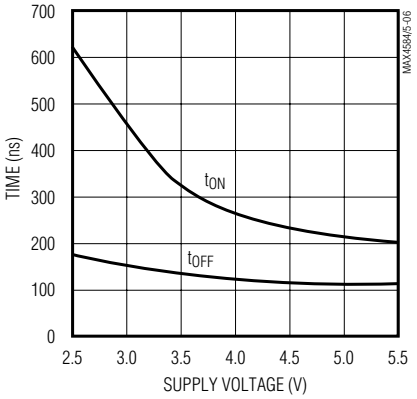
SUPPLY CURRENT vs. TEMPERATURE



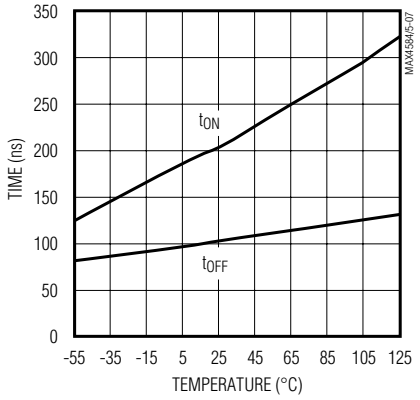
CHARGE INJECTION vs. V_{COM}



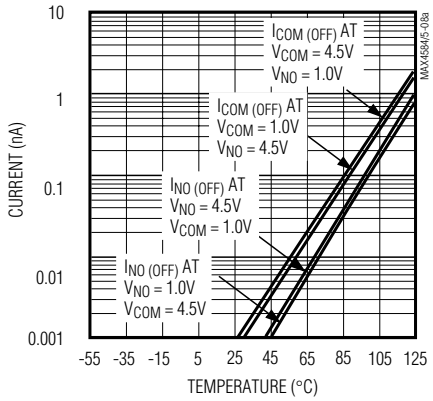
TURN-ON/TURN-OFF TIMES vs. SUPPLY VOLTAGE



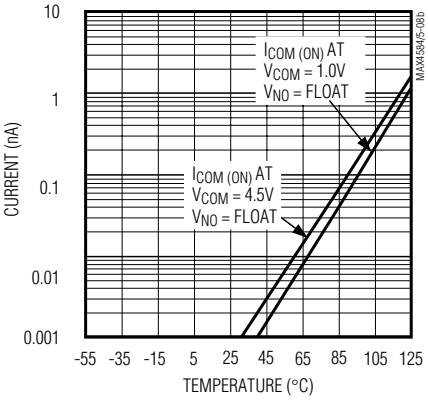
TURN-ON/TURN-OFF TIMES vs. TEMPERATURE



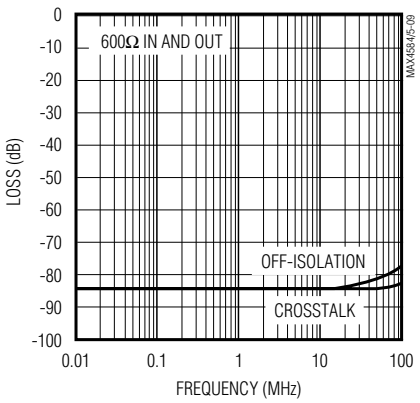
OFF-LEAKAGE CURRENT vs. TEMPERATURE



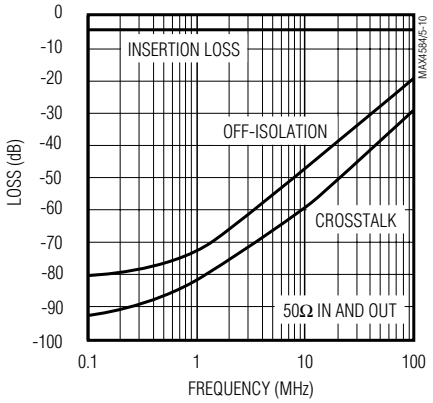
ON-LEAKAGE CURRENT vs. TEMPERATURE



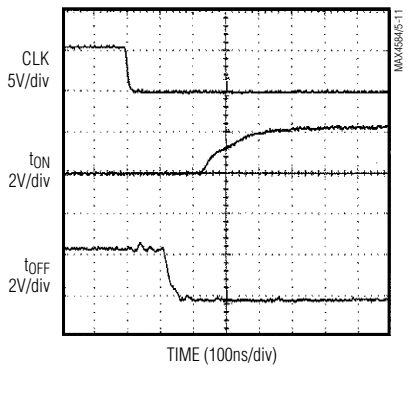
AUDIO FREQUENCY RESPONSE



VIDEO FREQUENCY RESPONSE



TURN-ON/TURN-OFF TIMES



Serially Controlled Audio/Video Switches

Pin Description

PIN		NAME	FUNCTION
MAX4584	MAX4585		
1	1	COM1	Analog Switch SPDT Common Terminal
2	—	A	LSB+2 of the 2-Wire Serial-Interface Address Field
—	2	$\overline{CS}$	Chip Select of the 3-Wire Serial Interface
3	—	SDA	Data Input of the 2-Wire Serial Interface
—	3	DIN	Data Input of the 3-Wire Serial Interface
4	4	V+	Supply Voltage
5	—	SCL	Clock Input of the 2-Wire Serial Interface
—	5	SCLK	Clock Input of the 3-Wire Serial Interface
6	6	NO2	Normally Open SPST Terminal
7	7	COM2	Analog Switch SPST Common Terminal
8	8	GND	Ground
9	9	NO1B	Normally Open Terminal
10	10	NO1A	Normally Open Terminal

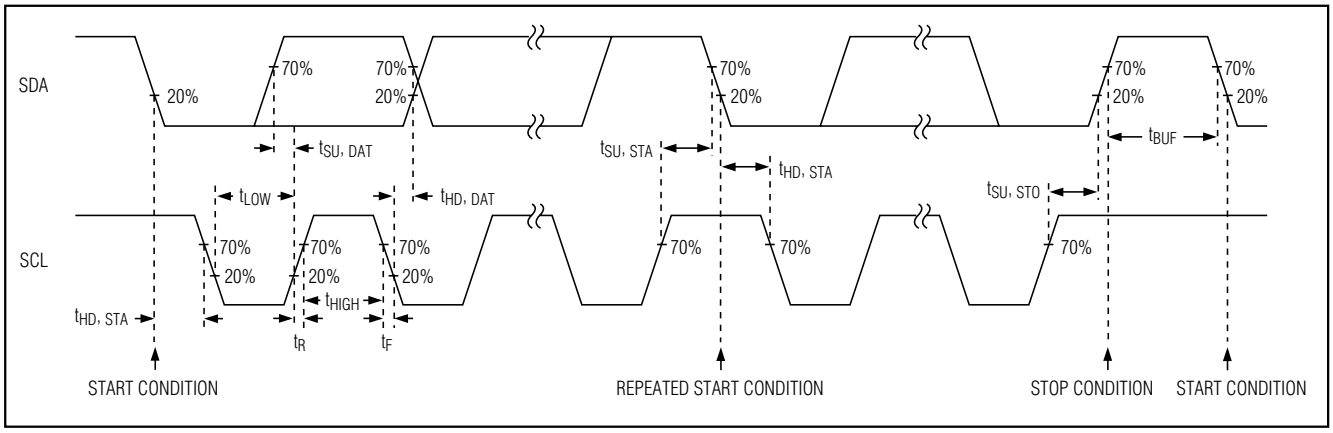


Figure 1. 2-Wire Serial-Interface Timing Diagram

Detailed Description

The MAX4584/MAX4585 are serial-interface, programmable switches. Each device contains one normally open (NO) single-pole/single-throw (SPST) switch and one single-pole/double-throw (SPDT) switch. The switches are independently controlled through the on-chip serial interface. The MAX4584 uses a 2-wire I^2C-compatible serial communications protocol; the MAX4585 uses a 3-wire SPI/QSPI/MICROWIRE-compatible serial communications protocol.

These devices operate from a single +2.7V to +5.5V supply and are optimized for use with an audio frequency of 20kHz and video frequencies up to 10MHz. They feature 65Ω on-resistance, 4Ω on-resistance matching between channels, and 5Ω on-resistance flatness. Audio off-isolation is -83dB at 20kHz, and crosstalk is at least -84dB at 20kHz. Video off-isolation is -48dB at 10MHz, and crosstalk is at least -60dB at 10MHz.

Applications Information

Switch Control

The MAX4584/MAX4585 have a common command-bit structure; the only difference between them is the interface type (2-wire or 3-wire, respectively).

The command controls the open/closed states of the various switches. Table 1 shows the configuration of the data bits and their related switches. After a command is issued, a logic “1” in any data-bit location clos-

Table 1. Command-Bit Mapping

COMMAND BIT	SWITCH	TERMINALS	POWER-UP STATE
D7 (MSB)	X	—	X
D6	X	—	X
D5	X	—	X
D4	X	—	X
D3	X	—	X
D2	NO2 to COM2	6, 7	0 (Open)
D1	NO1B to COM1	9, 1	1 (Closed)
D0 (LSB)	NO1A to COM1	10, 1	0 (Open)

X = Don't care

Table 2. Truth Table

LOGIC	NO1_ AND NO2
0	OPEN
1	CLOSED

Table 3. Address Bit Map

ADDRESS BIT (A)	ADDRESS
0	0110 1010
1	0110 1110

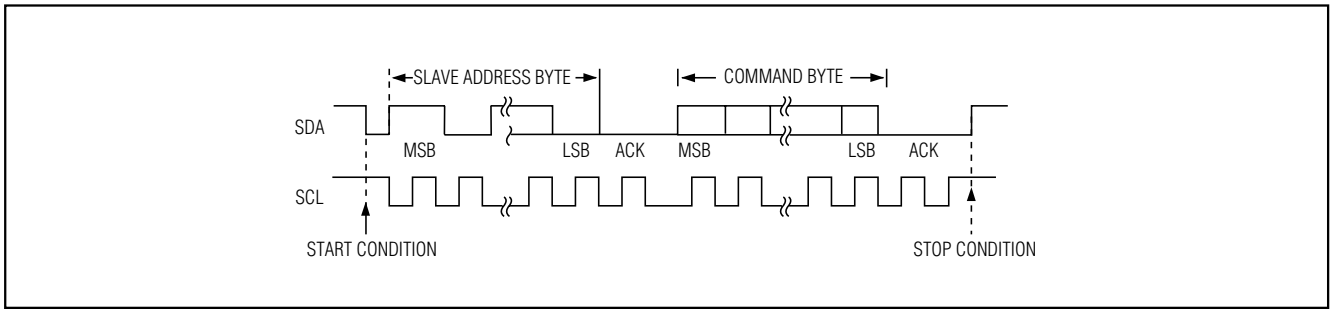


Figure 2. A Complete 2-Wire Serial-Interface Transmission

es the associated switch (Table 2). A logic "0" in any data-bit location opens the associated switch.

2-Wire Serial Interface

The MAX4584 uses a 2-wire I²C-compatible serial interface. The COM_ register uses the "SendByte" protocol, which consists of an address byte followed by a command byte (Table 1).

To address a given IC, bit A in the address byte must duplicate the value present at the A pin of that IC. The rest of the address bits must match those shown in Table 3. The command byte details are described in the *Switch Control* section.

The 2-wire serial interface requires only two I/O lines of a standard microprocessor (µP) port. Figures 1 and 2 detail the timing diagram for signals on the 2-wire bus, and Tables 1 and 3 detail the format of the signals. The MAX4584 is a receive-only device and must be controlled by the bus master device. A bus master device communicates by transmitting the address byte of the slave device over the bus and then transmitting the desired information. Each transmission consists of a start condition, an address byte, a command byte, and finally a stop condition. The slave device acknowledges the recognition of its address by pulling the SDA line low for one clock period after the address byte is transmitted. The slave device also issues a similar acknowledgment after the command byte.

Start and Stop Conditions

The bus master signals the beginning of a transmission with a start condition by transitioning SDA from high to low while SCL is high. When the bus master has finished communicating with the slave device, it issues a stop condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Slave Address (Address Byte)

The MAX4584 uses an 8-bit-long slave address. To select a slave address, connect A to V+ or GND. The MAX4584 has two possible slave addresses, so a maximum of two of these devices may share the same address line. The slave device MAX4584 monitors the serial bus continuously, waiting for a start condition followed by an address byte. When a slave device recognizes its address (01101A10), it acknowledges that it is ready for further communication by pulling the SDA line low for one clock period.

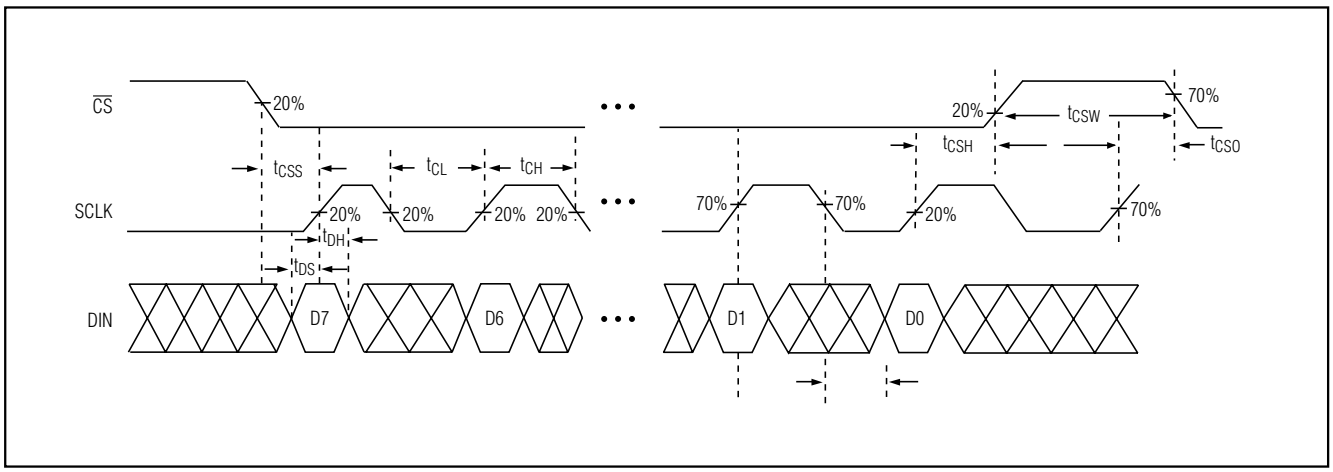


Figure 3. 3-Wire Serial-Interface Timing Diagram

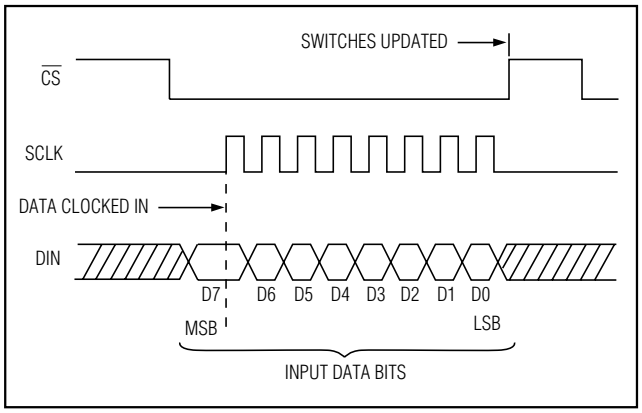


Figure 4. A Complete 3-Wire Serial Transmission

3-Wire Serial Interface

The MAX4585 3-wire serial interface is SPI/QSPI/MICROWIRE compatible. An active-low chip-select ($\overline{CS}$) input enables the device to receive data for the serial input (DIN). Data is clocked in on the rising edge of the serial-clock (SCLK) signal. A total of 8 bits are needed in each write cycle. The first bit clocked into the MAX4585 is the command byte's MSB; the last bit clocked in is the data byte's LSB. The first 5 bits of the command byte are "don't care." While shifting data, the device remains in its original configuration. After all 8 bits are clocked into the input shift register, a rising edge on $\overline{CS}$ latches the data into the MAX4585's internal registers, initiating the device's change of state. Figures 3 and 4 detail the 3-wire protocol, and Table 1 details the command byte format.

Addressable Serial Interface

To program several MAX4585s individually using a single µP, connect DIN of each MAX4585 together and control $\overline{CS}$ on each MAX4585 separately. To select a particular device, drive the corresponding $\overline{CS}$ low, clock in the 8-bit command, then drive $\overline{CS}$ high to execute the command. Typically, only one MAX4585 is addressed at a time.

Power-Up State

The MAX4584/MAX4585 feature a preset power-up state. See Table 1 to determine the power-up state of these devices.

Chip Information

TRANSISTOR COUNT: 2259

Test Circuits/Timing Diagrams

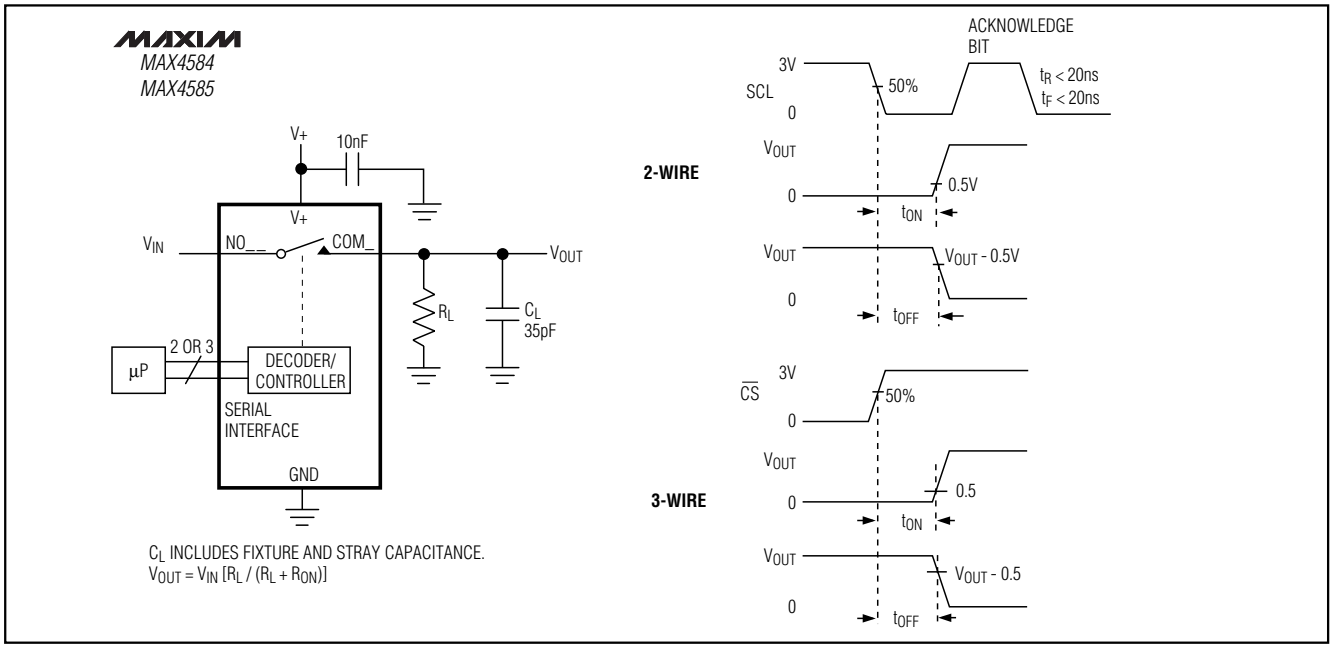


Figure 5. Switching Time

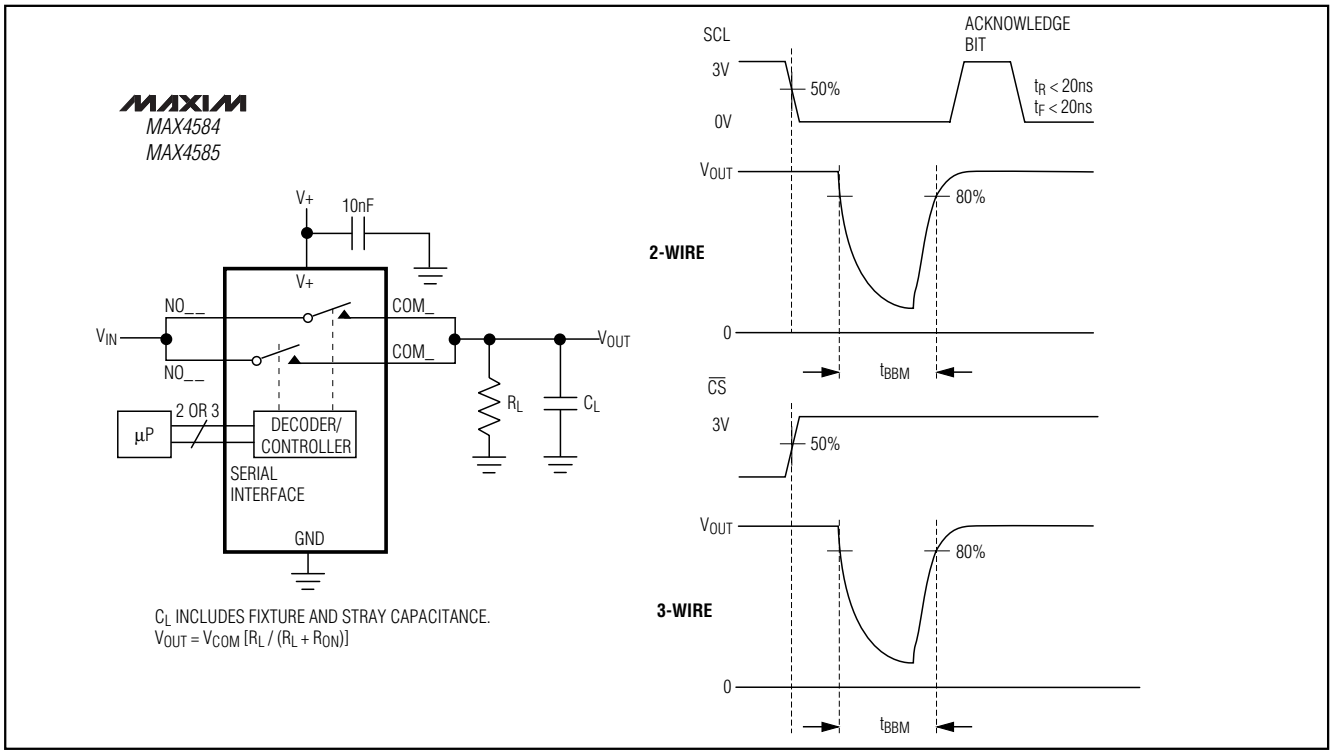


Figure 6. Break-Before-Make Interval

Serially Controlled Audio/Video Switches

Test Circuits/Timing Diagrams (continued)

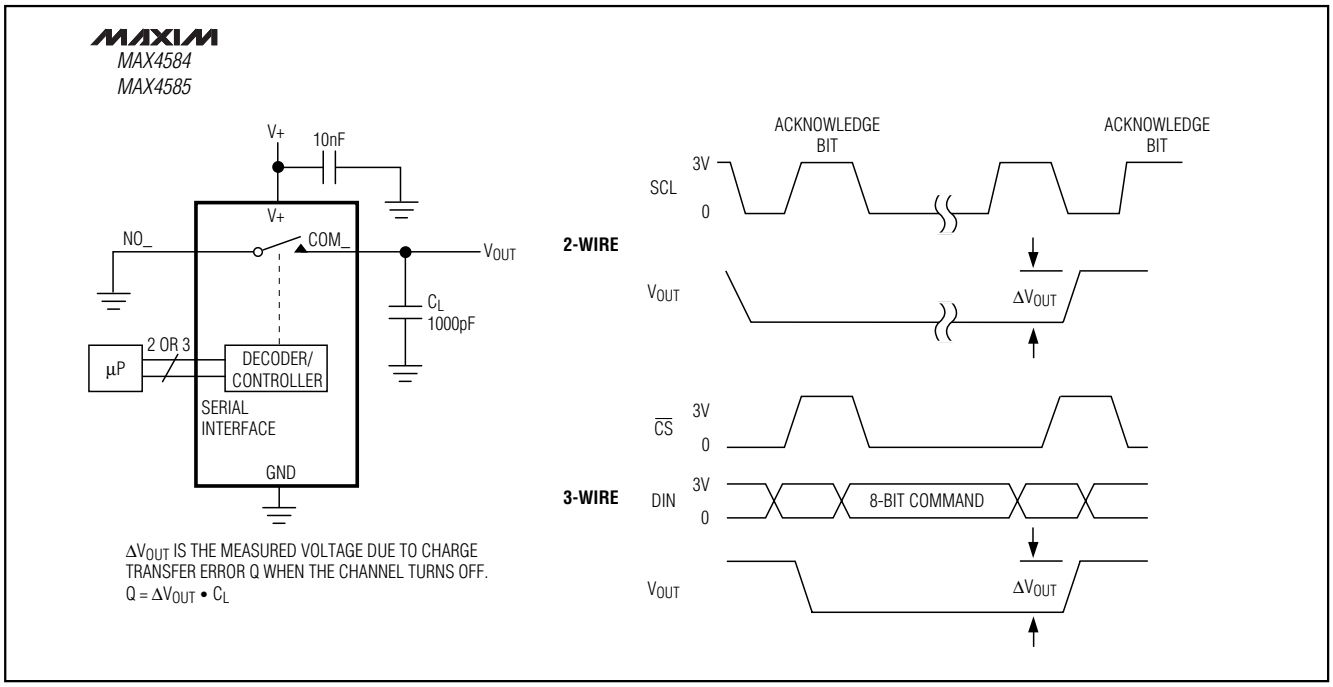


Figure 7. Charge Injection

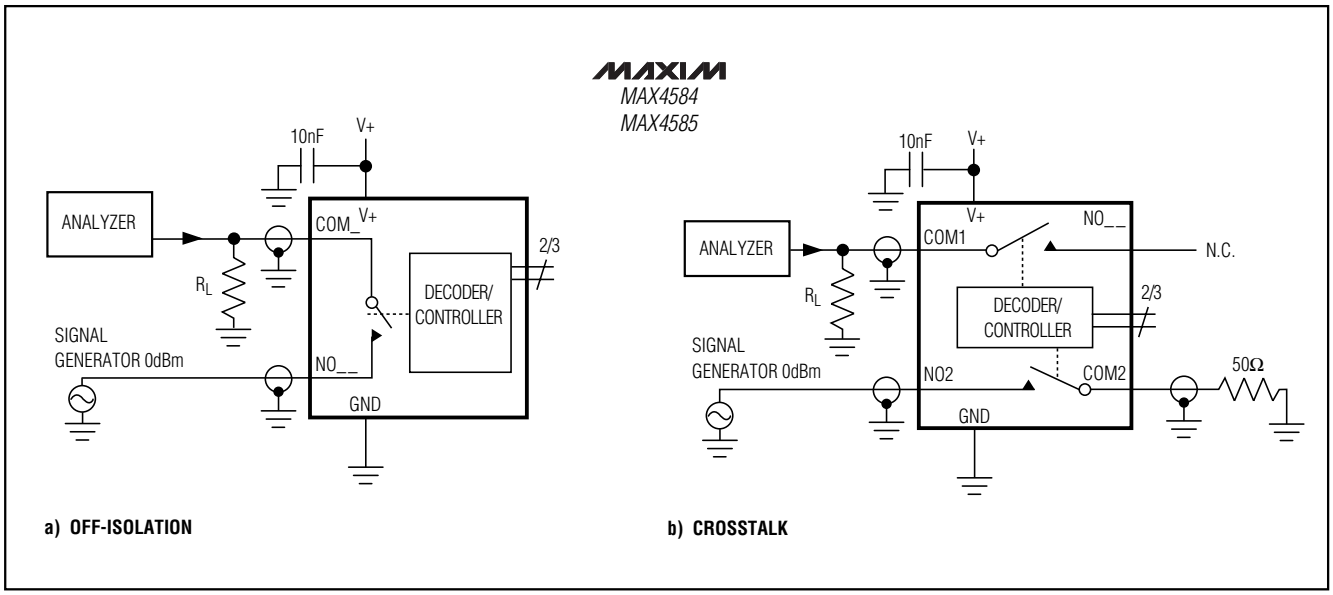


Figure 8. Off-Isolation and Crosstalk