

±15kV ESD-Protected, RS-232 Transceivers for Multidrop Applications

ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND

V_{CC}, V_L -0.3V to +6V

V₊ (Note 1) (V_{CC} - 0.3V) to +7V

V₋ (Note 1) +0.3V to -7V

V₊ + |V₋| (Note 1) +13V

Input Voltages

TIN₋, RENABLE, TXENABLE, $\overline{\text{SHDN}}$ -0.3V to +6V

RIN₋ ±25V

Output Voltages

TOUT₋ ±13.2V

ROUT₋ -0.3V to (V_L + 0.3V)

Short-Circuit Duration TOUT₋ to GND Continuous

Continuous Power Dissipation (T_A = +70°C)

16-Pin DIP (derate 10.5mW/°C above +70°C) 842mW

16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW

20-Pin TSSOP (derate 11mW/°C above +70°C) 879mW

Operating Temperature Range

MAX3322E/MAX3323E -40°C to +85°C

Junction Temperature +150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note 1: V₊ and V₋ can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V, V_L = 1.65V to 5.5V, C₁–C₄ = 0.1μF, tested at +3.3V ±10%; C₁ = 0.047μF, C₂ = C₃ = C₄ = 0.33μF, tested at +5V ±10%; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = V_L = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Current Normal Operation	I _{CC}	$\overline{\text{SHDN}} = V_L$, no load	1			mA
Supply Current in Shutdown	I _{CC} (SHDN)	$\overline{\text{SHDN}} = 0V$, no load	1		10	μA
TRANSMITTER LOGIC INPUTS						
Input Logic Threshold Low			0.4			V
Input Logic Threshold High		$V_L \leq 1.8V$	$V_L - 0.4$			V
		$V_L > 1.8V$	$2/3 \times V_L$			
Transmitter Input Hysteresis			0.2			V
Input Leakage Current	I _{IL}		±0.01	±1		μA
LOGIC INPUTS (TXENABLE, RENABLE, SHDN)						
Input Logic Threshold Low			0.4			V
Input Logic Threshold High			$2/3 \times V_L$			V
Input Leakage Current			±0.01	±1		μA
RECEIVER OUTPUTS						
Output Leakage Current	I _{OL}	Receivers disabled, $\overline{\text{SHDN}} = 0V$	±0.05	±10		μA
Output Voltage Low	V _{OL}	I _{OUT} = 1.6mA, $V_L > 1.8V$	0.4			V
		I _{OUT} = 1mA, $V_L \leq 1.8V$	0.4			
Output Voltage High	V _{OH}	I _{OUT} = -1mA, $V_L > 1.8V$	$V_L - 0.4$	$V_L - 0.1$		V
		I _{OUT} = -500μA, $V_L \leq 1.8V$	$V_L - 0.4$	$V_L - 0.1$		
RECEIVER INPUTS						
Input Voltage Range	V _{RIN}		-25		+25	V
Input Threshold Low		$V_L = 1.65V$	0.25	0.6		V
		$V_L = 3.3V$	0.6	1.2		
		$V_L = 5.0V$	0.8	1.5		

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MAX3322E/MAX3323E

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 5.5V, V_L = 1.65V to 5.5V, C₁–C₄ = 0.1μF, tested at +3.3V ±10%; C₁ = 0.047μF, C₂ = C₃ = C₄ = 0.33μF, tested at +5V ±10%; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = V_L = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Threshold High		V _L = 1.65V		1	1.4	V
		V _L = 3.3V		1.5	2.4	
		V _L = 5.0V		1.8	2.4	
Input Hysteresis				0.35		V
Input Resistance	R _{IN}	RENABLE = 1	3	5	7	kΩ
		RENABLE = 0 or $\overline{\text{SHDN}}$ = 0V, R _{IN} from -13V to +13V	1			MΩ
TRANSMITTER OUTPUTS						
Output Voltage Swing		All transmitter outputs loaded with 3kΩ to ground	±5	±5.4		V
Output Resistance		V _{CC} = V+ = V- = 0, TOUT ₋ = ±2V, TXENABLE = 1	300	10M		Ω
Output Short-Circuit Current		V _{OUT} = 0V			±60	mA
Output Leakage Current		V _{OUT} = ±12V, transmitters disabled			±25	μA
ESD PROTECTION						
R _{IN} , TOUT		Human Body Model		±15		kV
		IEC 1000-4-2 Air-Gap Discharge		±15		
		IEC 1000-4-2 Contact Discharge		±8		

TIMING CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V, V_L = 1.65V to 5.5V, C₁–C₄ = 0.1μF, tested at +3.3V ±10%; C₁ = 0.047μF, C₂ = C₃ = C₄ = 0.33μF, tested at +5V ±10%; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = V_L = 3.3V and T_A = +25°C, unless otherwise noted.)

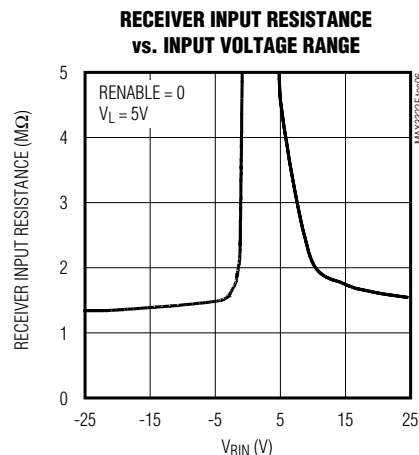
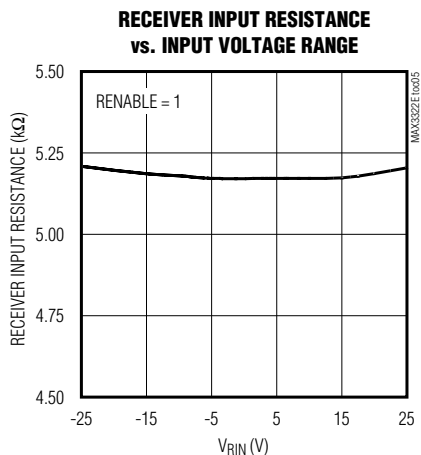
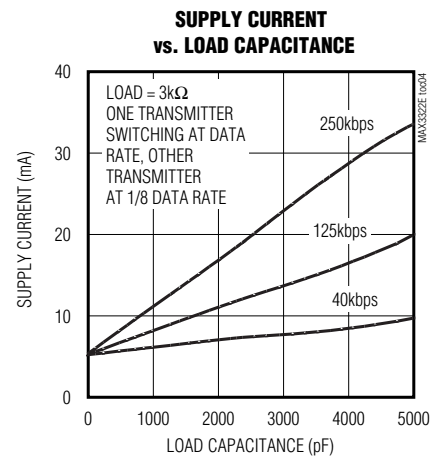
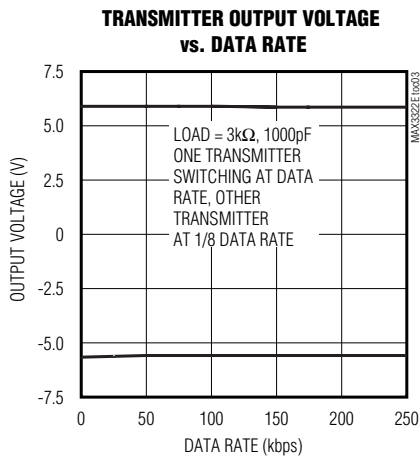
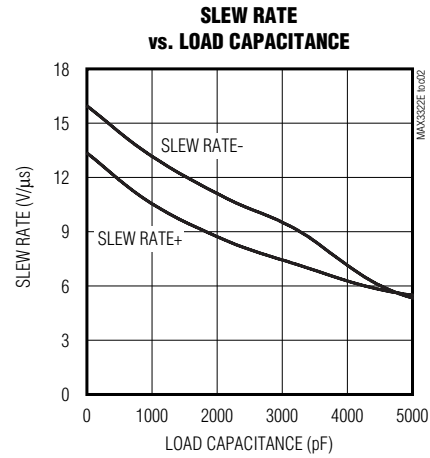
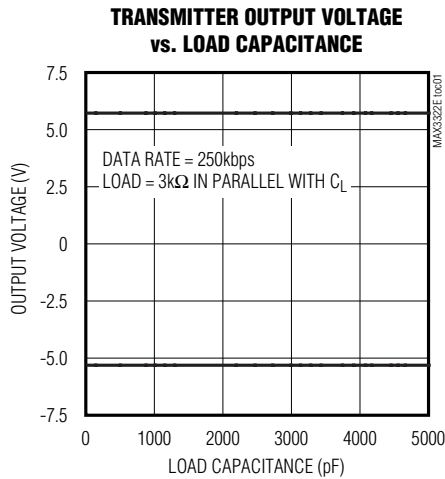
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Data Rate		R _L = 3kΩ, C _L = 1000pF, one transmitter switching	250			kbps
Receiver Propagation Delay	t _{PHL}	R _{IN} to R _{OUT} , C _L = 30pF, V _L = 3.3V, Figure 2		150		ns
	t _{PLH}			180		
Transmitter Propagation Delay	t _{PHL}	T _{IN} to TOUT, R _L = 3kΩ, C _L = 1000pF, Figure 1		0.6		μs
	t _{PLH}			0.7		
Time to Enter Three-State on Tx		(Note 2)		10	50	μs
Time to Exit Three-State on Tx		(Note 2)		3	50	μs
Time to Enable Resistor		(Note 2)		0.4	10	μs
Time to Disable Resistor		(Note 2)		0.2	10	μs
Time to Enter Shutdown				50		μs
Time to Exit Shutdown				50		μs
Transmitter Skew				100		ns
Receiver Skew				30		ns
Transition Region Slew Rate		R _L = 3kΩ to 7kΩ, C _L = 1000pF, measured from +3V to -3V or vice versa	6		30	V/μs

Note 2: Guaranteed by design. Not production tested.

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Typical Operating Characteristics

($V_{CC} = 3.3V$, $V_L = 3.3V$, $C_1-C_4 = 0.1\mu F$, $T_A = +25^\circ C$.)



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Pin Description

MAX3322E/MAX3323E

PIN		NAME	FUNCTION
MAX3322E	MAX3323E		
1	1	C1+	Positive Terminal of the Voltage-Doubler Charge-Pump Capacitor
2	2	V+	+5.5V Generated by the Charge Pump
3	3	C1-	Negative Terminal of the Voltage-Doubler Charge-Pump Capacitor
4	4	C2+	Positive Terminal of the Inverting Charge-Pump Capacitor
5	5	C2-	Negative Terminal of the Inverting Charge-Pump Capacitor
6	6	V-	-5.5V Generated by the Charge Pump
7, 9	7	TOUT ₋	Transmitter Output
8, 10	8	RIN ₋	Receiver Input
11, 13	9	ROUT ₋	Receiver Output
12, 14	10	TIN ₋	Transmitter Input
15	11	TXENABLE	Transmitter Enable. Drive TXENABLE high to enable transmitter. Drive TXENABLE low to put transmitter into high impedance.
16	12	RENABLE	Receiver Termination Enable. Drive RENABLE high for normal RS-232 5k Ω termination. Drive RENABLE low to make receiver inputs high impedance. In either case, the receiver and its output are enabled.
17	13	V _L	Logic-Level Supply. All CMOS inputs and outputs are referred to V _L , which is from 1.65V to 5.5V.
18	14	$\overline{\text{SHDN}}$	Shutdown Input. Drive $\overline{\text{SHDN}}$ low to put device into shutdown mode. Drive $\overline{\text{SHDN}}$ high for normal operation. In shutdown, all transmitter and receiver outputs are in three-state; receiver inputs are high impedance.
19	15	GND	Ground
20	16	V _{CC}	+3V to +5.5V Input Voltage. Bypass V _{CC} to GND with a 0.1 μ F capacitor.

Detailed Description

The MAX3322E/MAX3323E are RS-232 transceivers for multidrop applications (i.e., multiple-receiver operation). The devices are pin selectable between standard RS-232 operation with 5k Ω input resistance receivers or high-input-impedance receivers. Receivers of the MAX3322E/MAX3323E remain active in both modes of operation. In multidrop applications, a selected receiver is set at a 5k Ω input resistance, while the others are high-input impedance, maintaining RS-232 standards. Logic control permits selection of the functional mode: high impedance or normal load. The transmitters are enabled by logic control to allow transmission-line sharing.

The logic supply input (V_L) controls the levels of the system's I/O and works from 1.65V to 5.5V, providing compatibility with lower microprocessor I/O voltages. The transmitters are inverting level translators that convert CMOS logic levels into RS-232-compatible levels. They guarantee 250kbps with loads of R_L = 3k Ω and C_L

= 1000pF. The transmitters are enabled or disabled (three-stated) by the logic control TXENABLE, which manages transmission-line sharing in multidrop applications. When TXENABLE is high, the transmitter is enabled. When TXENABLE is low, the transmitter is put in high-impedance state. The receivers can be used in two conditions, selectable by the logic control RENABLE. When RENABLE is high, the internal 5k Ω resistor is connected across receiver input and ground. When RENABLE is low, the receiver input is high impedance, while maintaining receiving capability.

In shutdown mode, all transmitter and receiver outputs are three-stated, receiver inputs are in high impedance, the charge pump is turned off, V+ decays to V_{CC}, and V- decays to ground. ESD protection structures are incorporated in all pins to protect against ESD events encountered during handling and assembly. The receiver inputs and the transmitter outputs have ±15kV ESD structure implementation.

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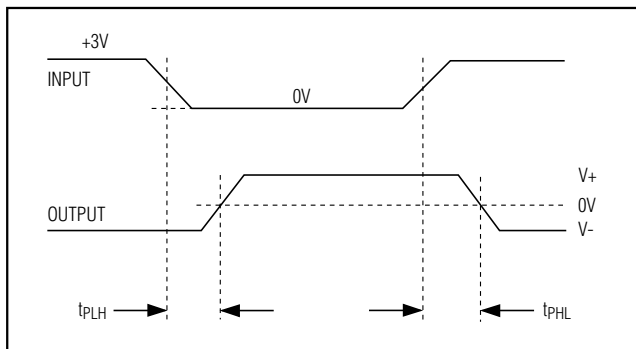


Figure 1. Transmitter Propagation-Delay Timing

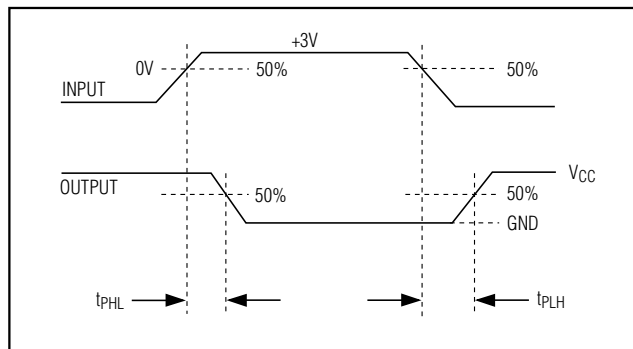


Figure 2. Receiver Propagation-Delay Timing

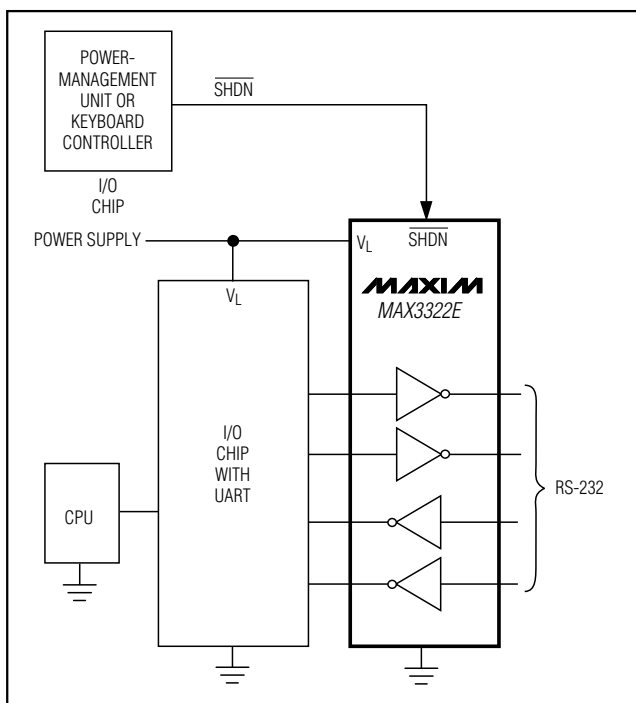


Figure 3. Interface Under Control of PMU

Dual Charge-Pump Voltage Converter

The MAX3322E/MAX3323Es' internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), regardless of the input voltage (V_{CC}), over a +3.0V to +5.5V range. The charge pumps operate in a discontinuous mode: if the output voltages are less than 5.5V, the charge pumps are enabled; if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a fly-

LapLink is a trademark of Traveling Software.

ing capacitor (C1, C2) and reservoir capacitor (C3, C4) to generate the $V+$ and $V-$ supplies. Because supply voltages can vary from +3V up to +5.5V, the selection of the capacitor values depends on the V_{CC} value. Table 2 shows minimum capacitor values.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels. The transmitters are enabled or disabled (three-stated) by the logic control TXENABLE, which manages transmission-line sharing in multidrop applications. When TXENABLE is high, the transmitter is enabled. When TXENABLE is low, the transmitter is put in a high-impedance state (see Table 1).

The MAX3322E/MAX3323Es' transmitters guarantee a 250kbps data rate with worst-case loads of $3\text{k}\Omega$ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Transmitters can be paralleled to drive multiple receivers or mice. Figure 3 shows a complete system connection.

RS-232 Receivers

MAX3322E/MAX3323E receivers convert RS-232 signals to CMOS-logic output levels. The unique feature of the receivers is the switchable input resistance. The receiver input resistance can be $5\text{k}\Omega$ or high impedance. These two conditions are selectable by the logic control RENABLE. When RENABLE is high, the $5\text{k}\Omega$ resistor is connected across the receiver input and ground. When RENABLE is low, the receiver input is high impedance, maintaining receiving capability. This feature permits the design of multidrop applications, which observe RS-232 interface standards.

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Table 1. Tx/Rx Logic

TXENABLE	RENABLE	SHDN	TRANSMITTER OUTPUT	RECEIVER OUTPUT	RECEIVER INPUT
1	1	0	High-Z	High-Z	High-Z
1	1	1	Active	Enabled	5k Ω
1	0	0	High-Z	High-Z	High-Z
1	0	1	Active	Enabled	High-Z
0	1	0	High-Z	High-Z	High-Z
0	1	1	High-Z	Enabled	5k Ω
0	0	0	High-Z	High-Z	High-Z
0	0	1	High-Z	Enabled	High-Z

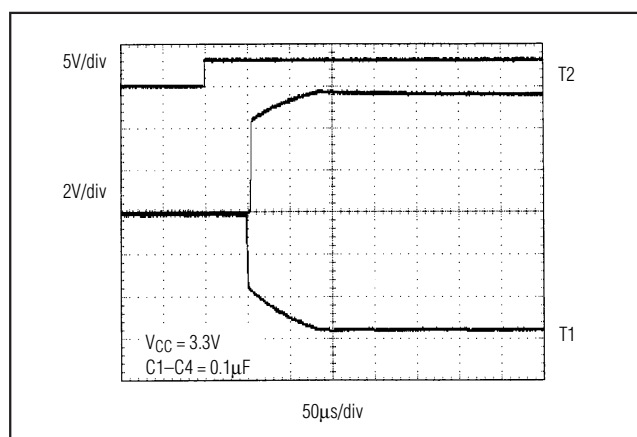


Figure 4. Transmitter Outputs when Exiting Shutdown

High-input impedance is guaranteed from -13.0V to +13.0V, when the receiver is in high-input-impedance mode. The receiver is able to withstand the RS-232 maximum input voltage of $\pm 25\text{V}$.

Shutdown Mode

Supply current falls to less than 10 μA when the MAX3322E/MAX3323E are placed in shutdown mode (logic low). When in shutdown mode, the devices' charge pumps are turned off, V_+ decays to V_{CC} , V_- is pulled to ground, the transmitter outputs and the receiver outputs are disabled (high impedance), and the receiver inputs are in high impedance (Table 1). The device enters shutdown when V_L or V_{CC} is absent.

The time required to exit shutdown is typically 50 μs , as shown in Figure 4. Connect $\overline{\text{SHDN}}$ to V_{CC} if shutdown mode is not used.

V_L Logic Supply Input

Unlike other RS-232 interface devices, in which the receiver outputs swing between 0 and V_{CC} , the MAX3322E/MAX3323E feature a separate logic supply input (V_L) that sets V_{OUT} for the receiver outputs and sets thresholds for the transmit and shutdown inputs. This feature allows a great deal of flexibility in interfacing to many types of systems with different logic levels. Connect this input to the host logic supply ($1.65\text{V} \leq V_L \leq 5.5\text{V}$).

$\pm 15\text{kV}$ ESD Protection

To protect the MAX3322E/MAX3323E against ESD, transmitters and receivers have extra protection against static electricity to protect the device up to $\pm 15\text{kV}$. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. ESD protection can be tested in various ways; the transmitter and receiver pins are characterized for protection to the following limits:

- $\pm 15\text{kV}$ using the Human Body Model
- $\pm 8\text{kV}$ using the IEC 1000-4-2 Contact Discharge method
- $\pm 15\text{kV}$ using the IEC 1000-4-2 Air-Gap method

Note: ESD performance depends on many conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 5 shows the Human Body Model, and Figure 6 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5k Ω resistor.

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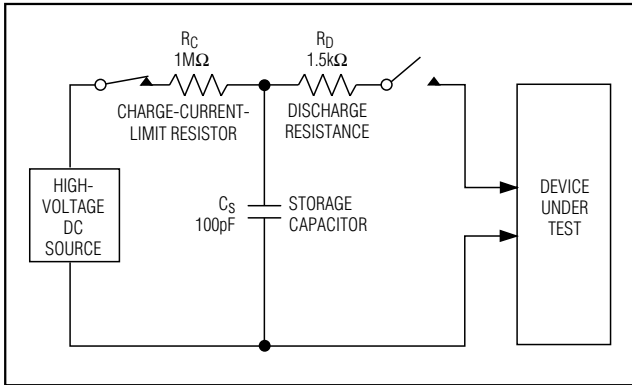


Figure 5. Human Body ESD Test Model

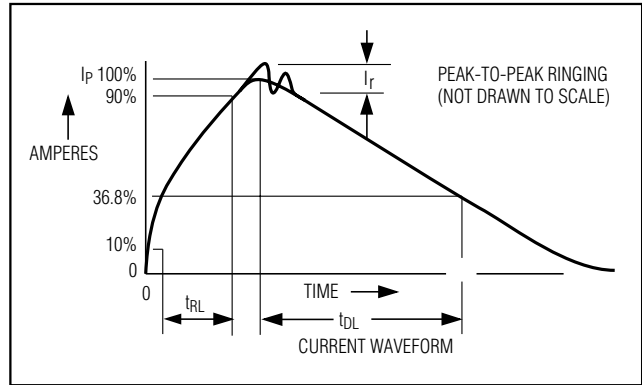


Figure 6. Human Body Model Current Waveform

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not refer specifically to integrated circuits. The MAX3322E/MAX3323E help the user design equipment that meets level 4 of IEC 1000-4-2, without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7 shows the IEC 1000-4-2 model. Figure 8 shows the current waveform it generates when discharged into a low impedance. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

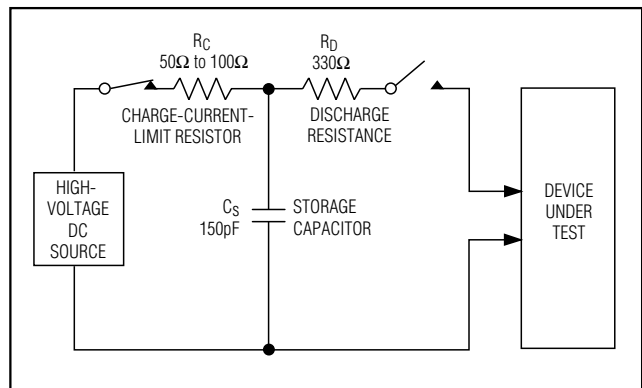


Figure 7. IEC 1000-4-2 ESD Test Model

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

The capacitor type used for C1–C4 is not critical for proper operation; polarized or nonpolarized capacitors can be used. The charge pump requires 0.1μF capacitors for 3.3V operation. For other supply voltages, see Table 2 for required capacitor values. Do not use values smaller than those listed in Table 2. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple

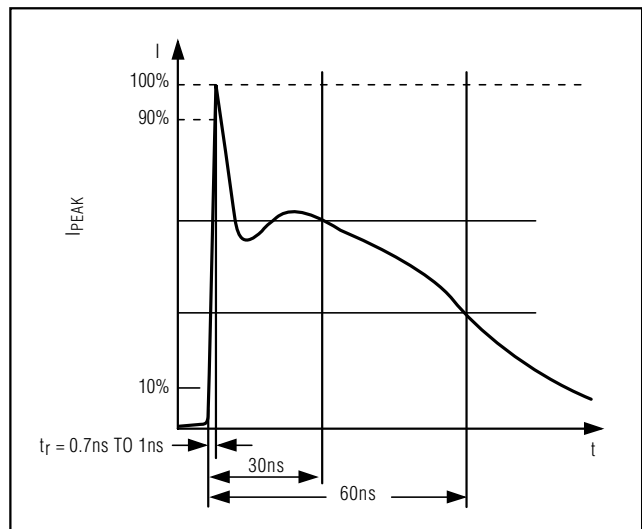


Figure 8. IEC 1000-4-2 ESD Generator Current Waveform

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on the transmitter outputs and slightly reduces power consumption. The values of C2, C3, and C4 can be increased without changing C1's value. However, do not increase C1's value without also increasing the values of C2, C3, and C4 to maintain the proper ratios (C1 to the other capacitors).

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Table 2. Minimum Required Capacitor Values

V _{CC} (V)	C1 (μF)	C2, C3, C4 (μF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1

Multidrop Applications

The MAX3323E connects to the RS-232 serial port of computer peripherals such as a bar-code scanner, video security controls, industrial multimeters, etc., and allows multiple devices to share the same communication cable connected to a PC.

Figure 9 shows a PC UART transmitting to a single receiver with a 5kΩ termination resistor while the other receivers remain in a high-impedance state. When the receiver inputs are high impedance, they remain active and maintain receiving capability. This feature permits the design of multidrop applications, which observe the RS-232 interface standard.

Transmitters are enabled and disabled through TXENABLE, allowing the sharing of a single bus line. Transmitters are high impedance when disabled. The host PC's transmitter stays enabled at all times. Only one peripheral transmitter remains enabled at any time. If the host PC wants to communicate with another peripheral, it first must tell the current peripheral to deassert its transmitter.

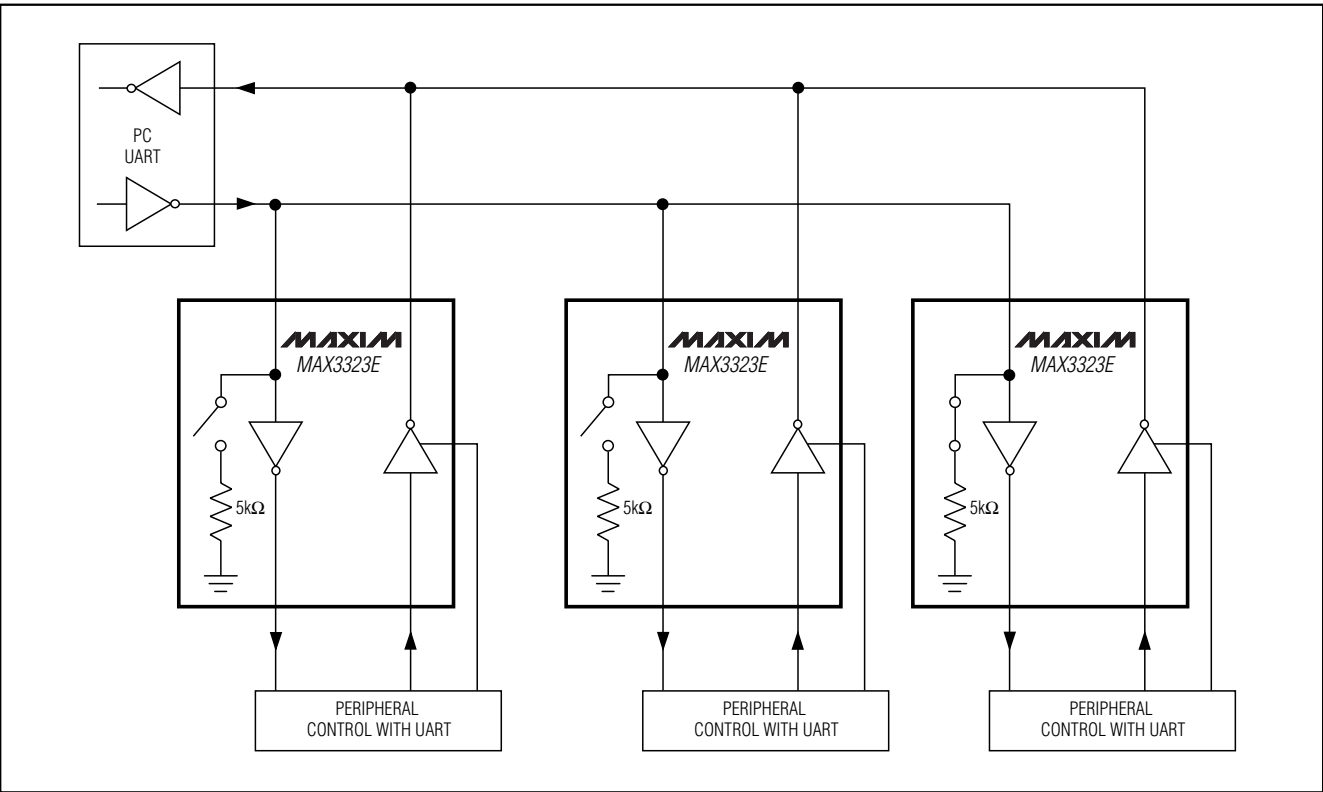


Figure 9. Multidrop Application

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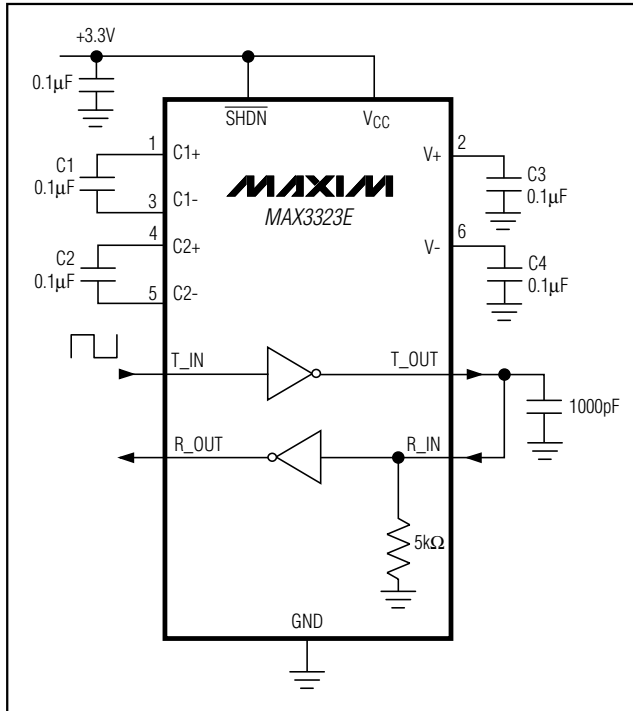


Figure 10. Loopback Test Circuit

Power-Supply Decoupling

In most circumstances, a 0.1µF bypass capacitor is adequate. In applications sensitive to power-supply noise, decouple VCC to ground with a capacitor of the same value as charge-pump capacitor C1. Connect bypass capacitors as close to the IC as possible.

High Data Rates

The MAX3322E/MAX3323E maintain the RS-232 $\pm 5.0\text{V}$ minimum transmitter output voltage even at high data rates. Figure 10 shows a transmitter loopback test circuit. Figure 11 shows a loopback test result at 125kbps, and Figure 12 shows the same test at 250kbps. For Figure 11, all transmitters were driven simultaneously at 125kbps into RS-232 loads in parallel with 1000pF. For Figure 12, a single transmitter was driven at 250kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

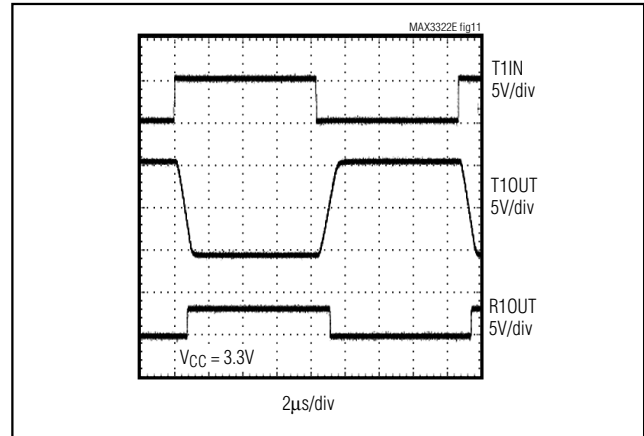


Figure 11. Loopback Test Results at 125kbps

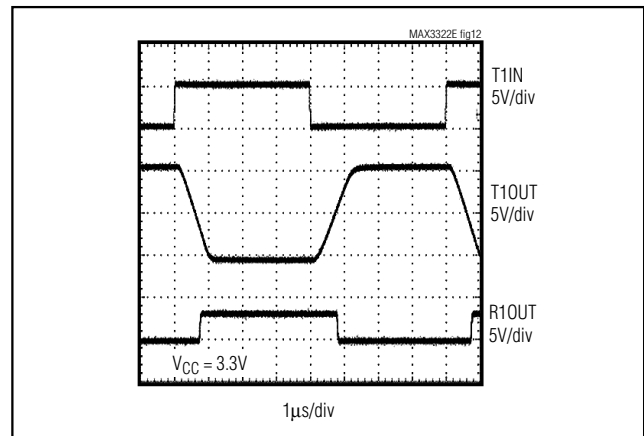


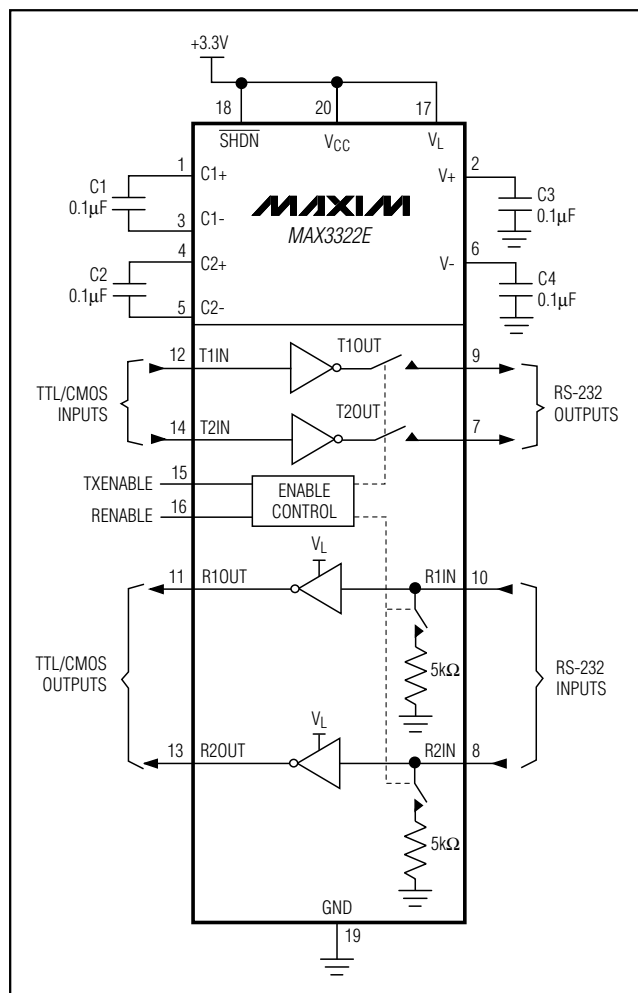
Figure 12. Loopback Test Results at 250kbps

Interconnection with 3V and 5V Logic

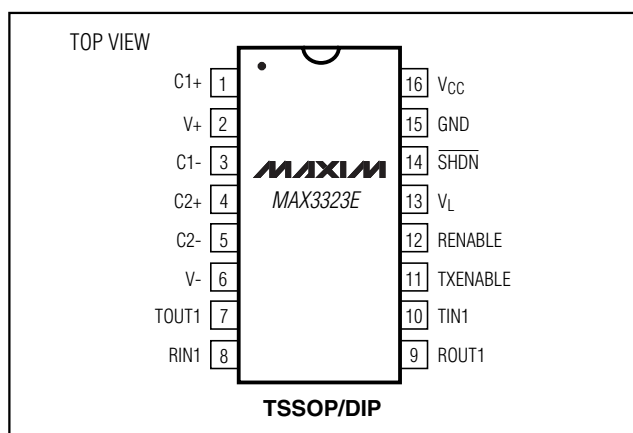
The MAX3322E/MAX3323E can directly interface with various 5V logic families, including ACT and HCT CMOS. The logic voltage power-supply pin V_L sets the output voltage level of the receivers and the input thresholds of the transmitters.

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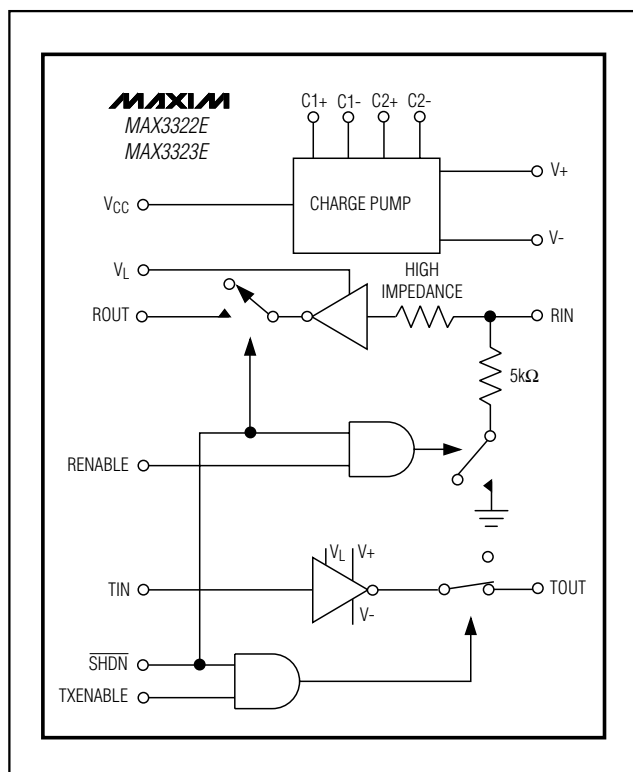
Typical Operating Circuit



Pin Configurations (continued)



Functional Diagram



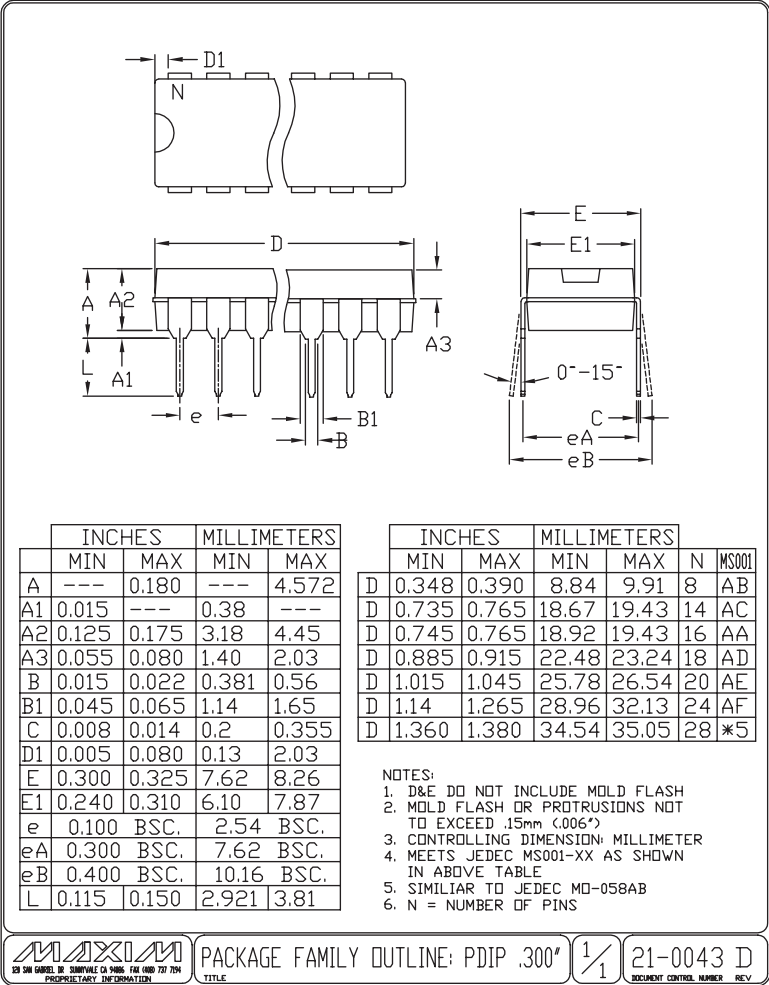
Chip Information

TRANSISTOR COUNT: 1294
PROCESS: BiCMOS

±15kV ESD-Protected, RS-232 Transceivers for Multidrop Applications

Package Information

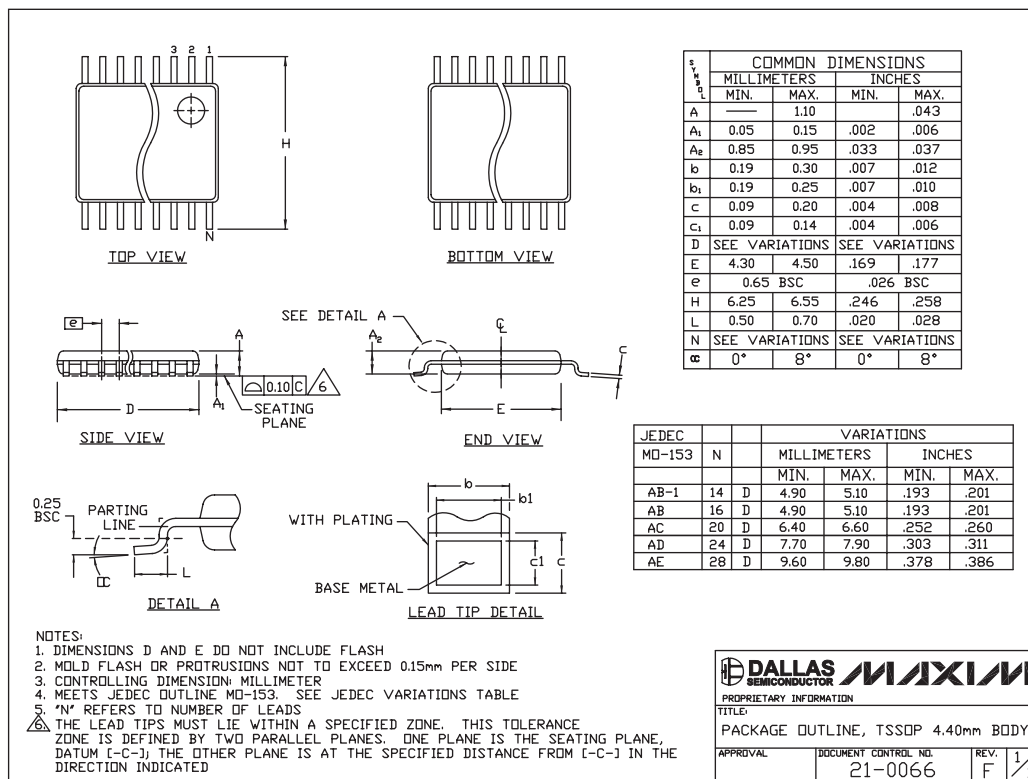
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



±15kV ESD-Protected, RS-232 Transceivers for Multidrop Applications

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



MAX3322E/MAX3323E

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