Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, FB, FBP, FBN, FB1, FB2, ONDC, $\overline{ONP}$, $\overline{ONN}$, $\overline{ON2}$, TGNDA, TGNDB to GND .....-0.3V to +6V
PGND to GND .....±0.3V
LX, V_{DDB} to GND .....-0.3V to +14V
DRVP, DRV1, DRV2, DRVA to GND .....-0.3V to +30V
REF, FREQ, GATE, OCN, OCP, CT, PFLT to GND .....-0.3V to V_{IN} + 0.3V
DRVN to GND .....V_{IN} - 28V to V_{IN} + 0.3V
FBPB, FBNB, OUTB to GND .....-0.3V to V_{DDB} + 0.3V
OUTB Continuous Output Current .....±100mA

MAX1997 Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN
(derate 21.2mW/°C above +70°C) 1702mW
MAX1998 Continuous Power Dissipation (T_A = +70°C)
20-Pin Thin QFN
(derate 20mW/°C above +70°C) 1600mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 3V, V_{DDB} = 10V, $\overline{SHDN}$ = ONDC = FREQ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range			2.7		5.5	V
IN Undervoltage Lockout Threshold	350mV (typ) hysteresis	V_{IN} rising	2.5	2.7	2.9	V
		V_{IN} falling	2.2	2.35	2.5	
IN Quiescent Current (Note 1)	V_{FB} = V_{FBP} = V_{FB1} = V_{FB2} = 1.5V, V_{FBN} = 0 (MAX1997 only)			0.54	1.25	mA
	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = 0 (MAX1998 only)			0.476	1	
IN Shutdown Current	$V_{\overline{SHDN}}$ = 0, V_{IN} = 5.5V			0.1	1	µA
REF Output Voltage	-2µA < I_{REF} < 50µA		1.231	1.250	1.269	V
	-2µA < I_{REF} < 75µA		1.225	1.250	1.275	
Thermal Shutdown				160		°C
OVERCURRENT COMPARATOR						
Input Offset Voltage	V_{OCN} = V_{OCP} = 1.5V to 0.8V × V_{IN}		-5		+5	mV
Input Bias Current	V_{OCN} = V_{OCP} = 0.8V × V_{IN}		-50		+50	nA
OCN, OCP Input Common-Mode Range			1.5		0.8 × V_{IN}	V
FAULT TIMER						
Fault Timer Period	PFLT = GND (MAX1997 only)			21.8		ms
	PFLT unconnected (MAX1997 only)			43.6		
	PFLT = IN, or MAX1998			87.2		
GATE Output Sink Current During Slew	V_{GATE} = 1.5V during turn-on transition		5	10	15	µA
GATE Output Pulldown Resistance	V_{GATE} < 0.5V				200	Ω
GATE Output Pullup Resistance					200	Ω
MAIN STEP-UP REGULATOR						
Output Voltage Range			V_{IN}		13	V
Operating Frequency	FREQ = IN			1.5		MHz
	FREQ unconnected		0.637	0.75	0.863	
	FREQ = GND			0.375		

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 3V, V_{DDB} = 10V, $\overline{SHDN}$ = ONDC = FREQ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Maximum Duty Cycle		80	85	90	%
FB Regulation Voltage	I_{LX} = 200mA	1.229	1.242	1.254	V
FB Fault Trip Level	V_{FB} falling	0.96	1.00	1.04	V
FB Load Regulation	I_{MAIN} = 0 to full load		-1.6		%
FB Line Regulation	V_{IN} = 2.7V to 5.5V		0.2	0.4	%/V
FB Input Bias Current	V_{FB} = 1.5V	-100		+100	nA
LX On-Resistance			250	450	mΩ
LX Leakage Current	V_{LX} = 13V		0.01	20	µA
LX Current Limit		1.6	2.1	2.8	A
LX RMS Current Rating	(Note 2)			1.4	A
Soft-Start Period			4096/f_{OSC}		s
Soft-Start Step Size			V_{REF}/32		V
POSITIVE LINEAR-REGULATOR CONTROLLERS (REG P, REG 1, AND REG 2)					
FB_ Regulation Voltage	I_{DRVP} = 100µA I_{DRV1} = 1350µA (MAX1997 only) I_{DRV2} = 335µA (MAX1997 only)	1.225	1.250	1.275	V
FB_ Fault Trip Level	$V_{FB_}$ falling	0.96	1.00	1.04	V
FB_ Input Bias Current	$V_{FB_}$ = 1.25V	-250		+250	nA
FB_ Effective Load Regulation Error (Transconductance)	V_{DRVP} = 10V, I_{DRVP} = 0.05mA to 1mA V_{DRV1} = 10V, I_{DRV1} = 0.5mA to 5mA (MAX1997 only) V_{DRV2} = 10V, I_{DRV2} = 0.1mA to 2mA (MAX1997 only)		-1.5	-2	%
FB_ Line (IN) Regulation Error	I_{DRVP} = 100µA, 2.7V < V_{IN} < 5.5V I_{DRV1} = 1350µA, 2.7V < V_{IN} < 5.5V (MAX1997 only) I_{DRV2} = 335µA, 2.7V < V_{IN} < 5.5V (MAX1997 only)		1		mV
Bandwidth	(Note 2)	1000			kHz
DRVP Sink Current	$V_{FB_}$ = 1.1V, $V_{DRV_}$ = 10V	2	3.3		mA
DRV1 Sink Current (MAX1997 only)		5	18		
DRV2 Sink Current (MAX1997 only)		5	15		
DRV_ Leakage Current	$V_{FB_}$ = 1.5V, $V_{DRV_}$ = 28V		0.1	10	µA
Soft-Start Period			4096/f_{OSC}		s
Soft-Start Step Size			V_{REF}/32		V
NEGATIVE LINEAR-REGULATOR CONTROLLER (REG N)					
FBN Regulation Voltage	I_{DRVN} = 100µA	95	125	155	mV
FBN Fault Trip Level	V_{FBN} rising	325	370	475	mV
FBN Input Bias Current	V_{FBN} = 0V	-200		+200	nA

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Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 3V, V_{DDB} = 10V, $\overline{SHDN}$ = ONDC = FREQ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FBN Effective Load Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		18	25	mV
FBN Line (IN) Regulation Error	I_{DRVN} = 100µA, 2.7V < V_{IN} < 5.5V		1		mV
Bandwidth	(Note 2)	1000			kHz
DRVN Source Current	V_{FBN} = 200mV, V_{DRVN} = -10V	2	4.2		mA
DRVN Leakage Current	V_{FBN} = -0.1V, V_{DRVN} = -20V		0.1	10	µA
Soft-Start Period			4096/f_{OSC}		s
Soft-Start Step Size			V_{REF}/32		V
VCOM BUFFER (MAX1997 only)					
V_{DDB} Supply Range		4.5		13	V
V_{DDB} Supply Current	V_{FBPB} = V_{FBNB} = 5V, V_{DDB} = 9V		367	900	µA
V_{DDB} Shutdown Current	V_{DDB} = 13V, $\overline{SHDN}$ = ONDC = GND		3.5	13	µA
Input Offset Voltage	V_{FBPB} = 2.5V, no load	-5		+5	mV
Input Bias Current	V_{FBPB} = V_{FBNB} = 1.2V to V_{DDB} - 1.2V			1	µA
Input Offset Current	V_{FBPB} = V_{FBNB} = 1.2V to V_{DDB} - 1.2V	-100		+100	nA
Input Common-Mode Range	V_{DDB} = 4.5V to 13V	1.2		V_{DDB} - 1.2	V
Power-Supply Rejection Ratio	V_{DDB} = 4.5V to 13V, V_{FBPB} = 2.25V	70			dB
Common-Mode Rejection Ratio	V_{FBPB} = V_{FBNB} = 1.2V to V_{DDB} - 1.2V	70			dB
Gain-Bandwidth Product	Small signal		1/6πC_L		Hz
Load-Transient Settling Time	R_L = 25Ω, C_L = 10nF, V_{DRIVE} = 9V, settle to within 10mV (Note 4)		5		µs
Transconductance	Small signal (±1mV overdrive)		0.3		µS
	Large signal (±30mV overdrive)		7.2		
Output Current Drive	±100mV overdrive, V_{OUTB} = 3V or 7V	±150	±300		mA
LOGIC SIGNALS ($\overline{SHDN}$, ONDC)					
Input Low Voltage	100mV typ hysteresis			0.4	V
Input High Voltage		1.6			V
Input Current			0.01	1	µA
CONTROL INPUTS AND OUTPUTS					
$\overline{ONN}$, $\overline{ONP}$, $\overline{ON2}$ Comparator Offset	$V_{\overline{ON_}}$ - V_{CT}, V_{CT} = 1.25V ±50mV	-50		+50	mV
DRVA Sink Current	V_{DRVA} = 10V, V_{CT} = 1.25V, $V_{\overline{ON2}}$ = 2V	5	11		mA
DRVA Off-Leakage	V_{DRVA} = 28V, V_{CT} = 1.25V, $V_{\overline{ON2}}$ = 1V		0.1	10	µA
CT Source Current	V_{CT} = 1V	2.5	5	7.5	µA
CT Discharge Resistance	V_{CT} = 1V		15	100	Ω
FREQ, PFLT Input Low Voltage				1	V
FREQ, PFLT Input Middle Voltage			V_{IN}/2		
FREQ, PFLT Input High Voltage		V_{IN} - 1			V
FREQ, PFLT Input Current	FREQ, PFLT = GND or IN	-50		+50	µA

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, V_{DDB} = 10V, $\overline{SHDN}$ = ONDC = FREQ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range			2.7		5.5	V
IN Undervoltage Lockout Threshold	350mV typ hysteresis	V_{IN} rising	2.5		2.9	V
		V_{IN} falling	2.2		2.5	
IN Quiescent Current (Note 1)	V_{FB} = V_{FBP} = V_{FB1} = V_{FB2} = 1.5V, V_{FBN} = 0 (MAX1997 only)				1.25	mA
	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = 0 (MAX1998 only)				1	
REF Output Voltage	-2µA < I_{REF} < 50µA		1.223		1.270	V
	-2µA < I_{REF} < 75µA		1.218		1.280	
OVERCURRENT COMPARATOR						
Input Offset Voltage	V_{OCN} = V_{OCP} = 1.5V to 0.8V × V_{IN}		-5		+5	mV
Input Bias Current	V_{OCN} = V_{OCP} = 0.8V × V_{IN}		-50		+50	nA
OCN, OCP Input Common-Mode Range			1.5		0.8 × V_{IN}	V
MAIN STEP-UP REGULATOR						
Output Voltage Range			V_{IN}		13	V
Operating Frequency	FREQ = IN		1		2	MHz
	FREQ unconnected		0.563		0.937	
	FREQ = GND		0.25		0.50	
Oscillator Maximum Duty Cycle			78		92	%
FB Regulation Voltage	I_{LX} = 200mA		1.215		1.260	V
FB Fault Trip Level	V_{FB} falling		0.96		1.04	V
FB Input Bias Current	V_{FB} = 1.5V		-100		+100	nA
LX On-Resistance					450	mΩ
LX Current Limit			1.6		2.8	A
POSITIVE LINEAR-REGULATOR CONTROLLERS (REG P, REG 1, AND REG 2)						
FB_ Regulation Voltage	I_{DRVP} = 100µA		1.213		1.288	V
	I_{DRV1} = 1350µA (MAX1997 only)					
	I_{DRV2} = 335µA (MAX1997 only)					
FB_ Fault Trip Level	$V_{FB_}$ falling		0.96		1.04	V
FB_ Effective Load Regulation Error (Transconductance)	V_{DRVP} = 10V, I_{DRVP} = 0.05mA to 1mA				-2.5	%
	V_{DRV1} = 10V, I_{DRV1} = 0.5mA to 5mA (MAX1997 only)					
	V_{DRV2} = 10V, I_{DRV2} = 0.1mA to 2mA (MAX1997 only)					
DRVP Sink Current	$V_{FB_}$ = 1.1V, $V_{DRV_}$ = 10V		1			mA
DRV1 Sink Current (MAX1997 Only)			5			
DRV2 Sink Current (MAX1997 Only)			5			

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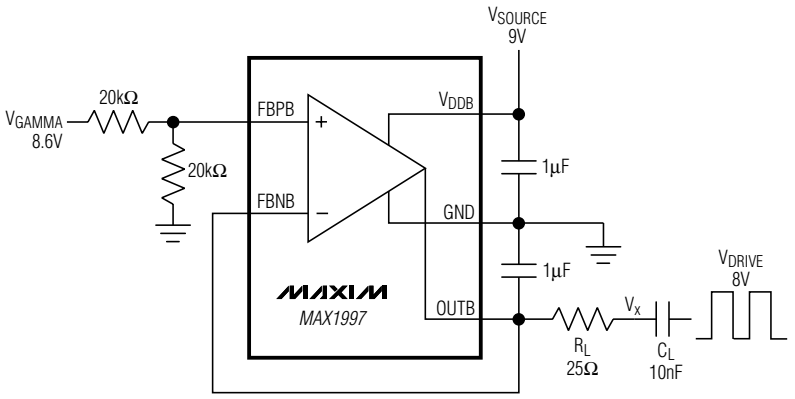
Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{DDB} = 10V, $\overline{SHDN}$ = ONDC = FREQ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
NEGATIVE LINEAR-REGULATOR CONTROLLER (REG N)					
FBN Regulation Voltage	I_{DRVN} = 100µA	95		155	mV
FBN Fault Trip Level	V_{FBN} rising	325		475	mV
FBN Effective Load Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 0.05mA to 5mA			30	mV
DRVN Source Current	V_{FBN} = 200mV, V_{DRVN} = -10V	1			mA
VCOM BUFFER (MAX1997 only)					
V_{DDB} Supply Range		4.5		13	V
V_{DDB} Supply Current	V_{FBPB} = V_{FBNB} = 5V, V_{DDB} = 9V			900	µA
Input Offset Voltage	V_{FBPB} = 2.5V, no load	-5		+5	mV
Input Bias Current	V_{FBPB} = V_{FBNB} = 1.2V to V_{DDB} - 1.2V			1	µA
Input Common-Mode Range	V_{DDB} = 4.5V to 13V	1.2		V_{DDB} - 1.2	V
Out Current Drive	±100mV overdrive, V_{OUTB} = 3V or 7V	±150			mA
LOGIC SIGNALS ($\overline{SHDN}$, ONDC)					
Input Low Voltage	100mV typ hysteresis			0.4	V
Input High Voltage		1.6			V
CONTROL INPUTS AND OUTPUTS					
FREQ, PFLT Input Low Voltage				1	V
FREQ, PFLT Input High Voltage		V_{IN} - 1			V
FREQ, PFLT Input Current	FREQ, PFLT = GND or IN	-50		+50	µA

Note 1: Quiescent current does not include switching losses.
Note 2: Guaranteed by design, not production tested.
Note 3: Specifications to -40°C are guaranteed by design, not production tested.
Note 4: The VCOM buffer load transient settling time is measured with the following circuit:



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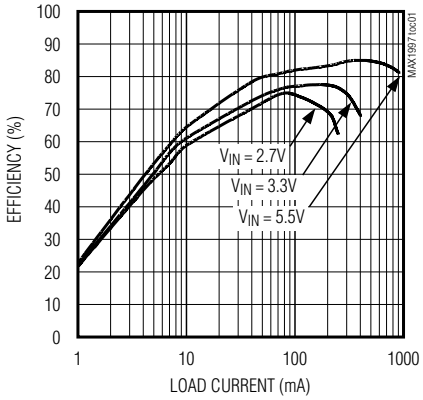
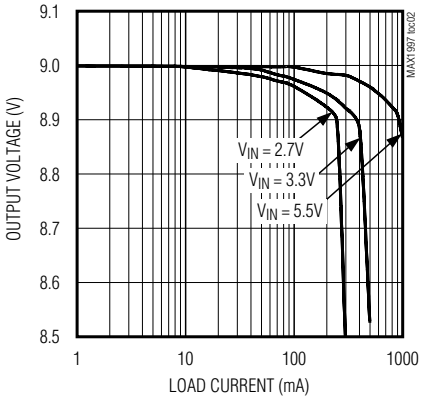
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 3.3V, V_{MAIN} = 9V, V_{G_ON} = 20V, V_{G_OFF} = -7V, V_{LOGIC} = 2.5V, V_{GAMMA} = 8.6V, T_A = +25°C, unless otherwise noted.)

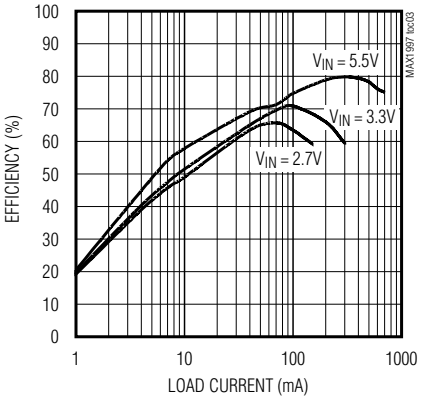
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 9V)



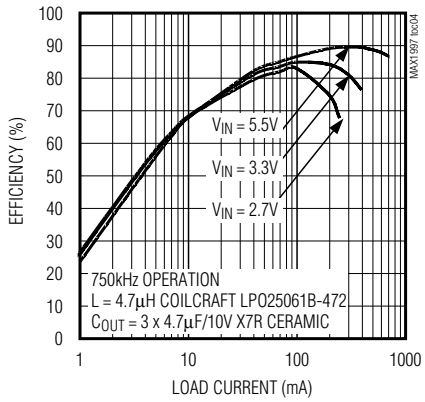
STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (V_{MAIN} = 9V)



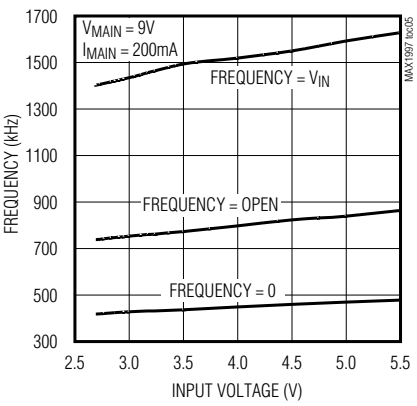
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 13V)



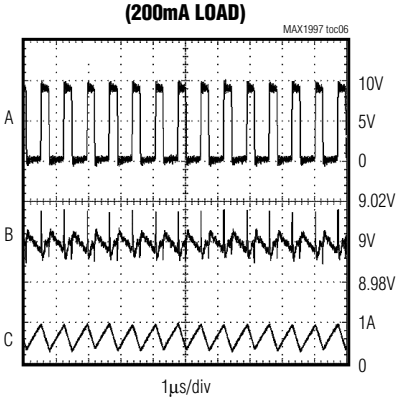
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



STEP-UP REGULATOR SWITCHING FREQUENCY vs. INPUT VOLTAGE

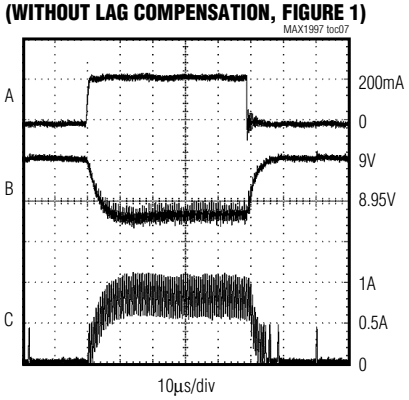


STEP-UP REGULATOR NORMAL OPERATION (200mA LOAD)



A: V_{LX}, 5V/div
B: V_{MAIN} = 9V, 20mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 1A/div

STEP-UP REGULATOR LOAD TRANSIENT RESPONSE (WITHOUT LAG COMPENSATION, FIGURE 1)



A: I_{MAIN} = 0 TO 200mA, 200mA/div
B: V_{MAIN} = 9V, 50mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 500mA/div

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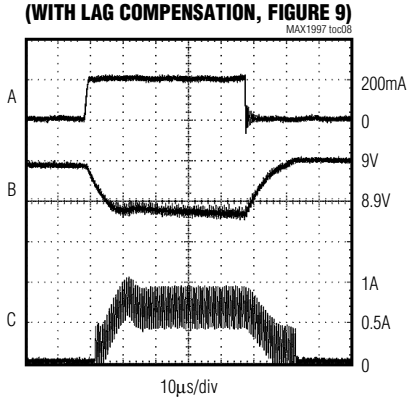
Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

Typical Operating Characteristics (continued)

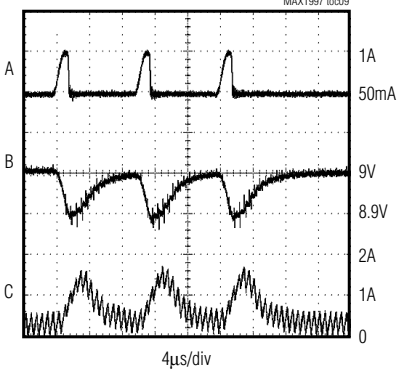
(Circuit of Figure 1, V_{IN} = 3.3V, V_{MAIN} = 9V, V_{G_ON} = 20V, V_{G_OFF} = -7V, V_{LOGIC} = 2.5V, V_{GAMMA} = 8.6V, T_A = +25°C, unless otherwise noted.)

STEP-UP REGULATOR LOAD TRANSIENT RESPONSE (WITH LAG COMPENSATION, FIGURE 9)



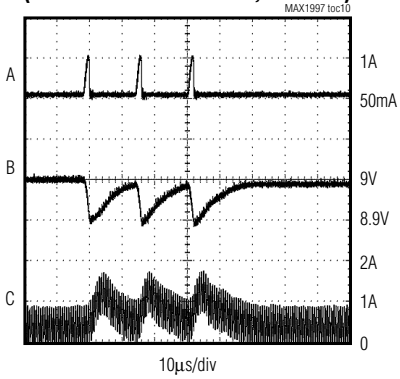
A: I_{MAIN} = 0 TO 200mA, 200mA/div
B: V_{MAIN} = 9V, 50mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 500mA/div
R7 = 76.8kΩ, R8 = 12.1kΩ, R10 = 1.5kΩ, C10 = 470pF

STEP-UP REGULATOR LOAD TRANSIENT RESPONSE (2µs PULSES) (WITHOUT LAG COMPENSATION, FIGURE 1)



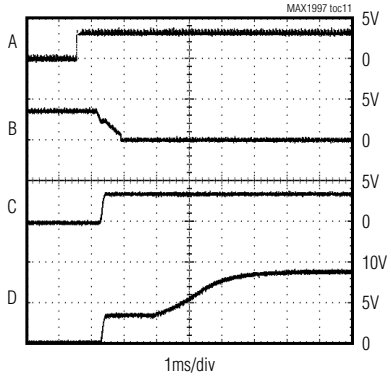
A: I_{MAIN} = 50mA TO 1A, 1A/div
B: V_{MAIN} = 9V, 100mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 1A/div

STEP-UP REGULATOR LOAD TRANSIENT RESPONSE (2µs PULSES) (WITH LAG COMPENSATION, FIGURE 9)



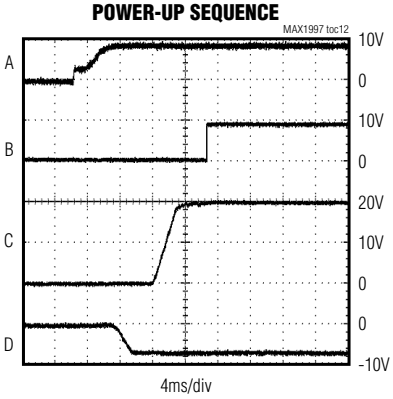
A: I_{MAIN} = 50mA TO 1A, 1A/div
B: V_{MAIN} = 9V, 100mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 1A/div
R7 = 76.8kΩ, R8 = 12.1kΩ, R10 = 1.5kΩ, C10 = 470pF

STEP-UP REGULATOR SOFT-START



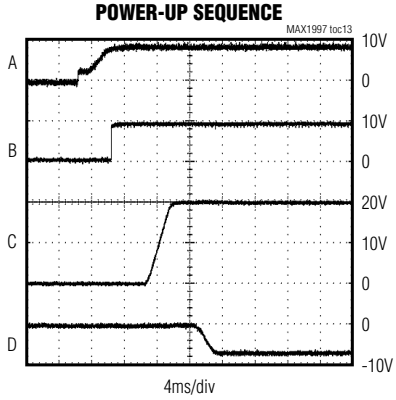
A: $V_{\overline{SHDN}}$, 5V/div
B: V_{GATE}, 5V/div
C: V_{DRAIN}, 5V/div
D: V_{MAIN}, 5V/div

POWER-UP SEQUENCE



A: V_{MAIN}, 10V/div
B: V_{SOURCE}, 10V/div
C: V_{GATE_ON}, 10V/div
D: V_{GATE_OFF}, 10V/div
$V_{\overline{ONN}} < V_{\overline{ONP}} < V_{\overline{ON2}}$

POWER-UP SEQUENCE



A: V_{MAIN}, 10V/div
B: V_{SOURCE}, 10V/div
C: V_{GATE_ON}, 10V/div
D: V_{GATE_OFF}, 10V/div
$V_{\overline{ONN}} > V_{\overline{ONP}} > V_{\overline{ON2}}$

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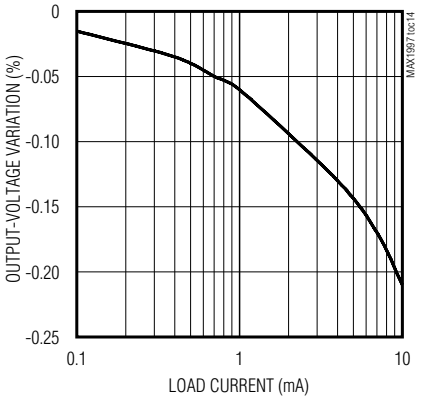
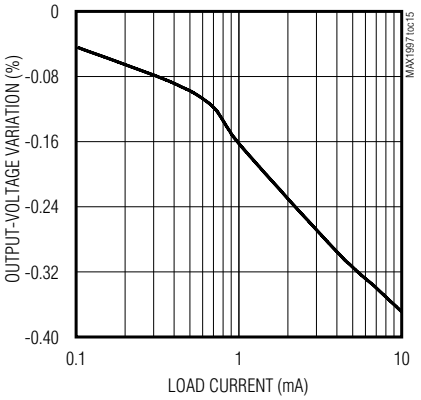
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.3V, V_{MAIN} = 9V, V_{G_ON} = 20V, V_{G_OFF} = -7V, V_{LOGIC} = 2.5V, V_{GAMMA} = 8.6V, T_A = +25°C, unless otherwise noted.)

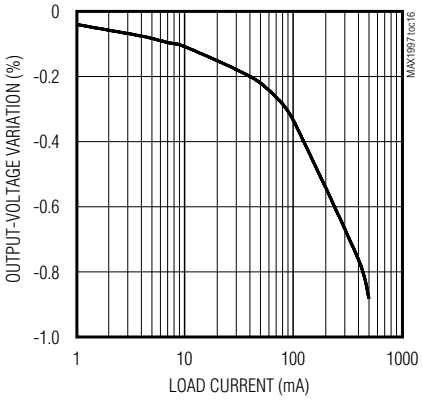
REG P (GATE-ON VOLTAGE) LOAD REGULATION



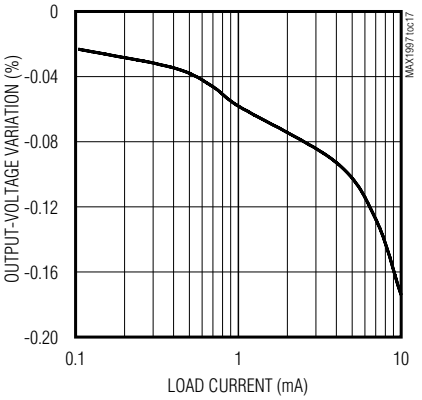
REG N (GATE-OFF VOLTAGE) LOAD REGULATION



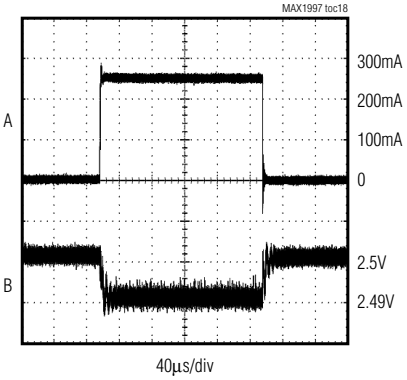
REG 1 (LOGIC SUPPLY) LOAD REGULATION



REG 2 (GAMMA REFERENCE) LOAD REGULATION

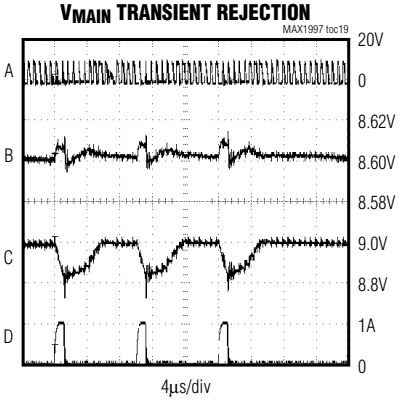


REG 1 (LOGIC SUPPLY) LOAD TRANSIENT RESPONSE



A: LOAD CURRENT, 0 TO 250mA, 100mA/div
B: V_{LOGIC} = 2.5V, 10mV/div, AC-COUPLED

REG 2 (GAMMA REFERENCE) V_{MAIN} TRANSIENT REJECTION



A: V_{LX}, 20V/div
B: V_{GAMMA} = 8.6V, 20mV/div, AC-COUPLED
C: V_{MAIN} = 9V, 200mV/div, AC-COUPLED
D: I_{MAIN} = 0 TO 1A, 1A/div

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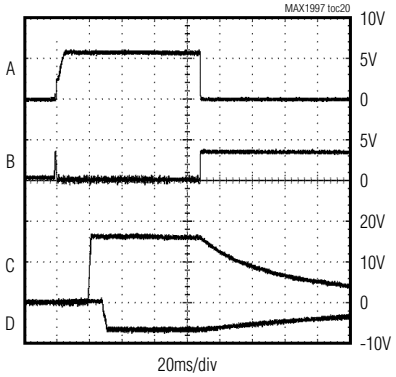
Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

Typical Operating Characteristics (continued)

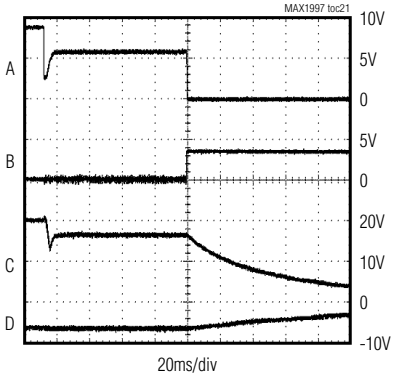
(Circuit of Figure 1, V_{IN} = 3.3V, V_{MAIN} = 9V, V_{G_ON} = 20V, V_{G_OFF} = -7V, V_{LOGIC} = 2.5V, V_{GAMMA} = 8.6V, T_A = +25°C, unless otherwise noted.)

OVERCURRENT PROTECTION RESPONSE TO OVERLOAD DURING STARTUP



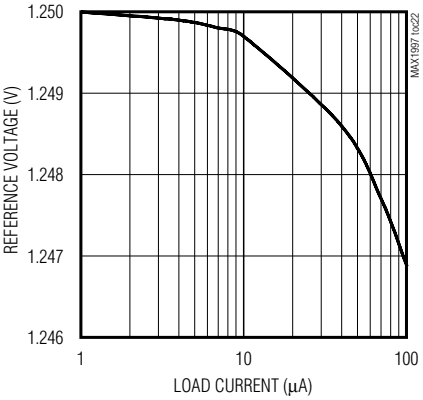
A: V_{MAIN}, 5V/div
B: V_{GATE}, 5V/div
C: V_{G_ON}, 10V/div
D: V_{G_OFF}, 10V/div

OVERCURRENT PROTECTION RESPONSE TO OVERLOAD DURING NORMAL OPERATION

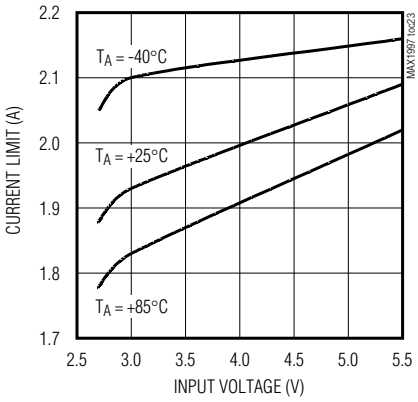


A: V_{MAIN}, 5V/div
B: V_{GATE}, 5V/div
C: V_{G_ON}, 10V/div
D: V_{G_OFF}, 10V/div

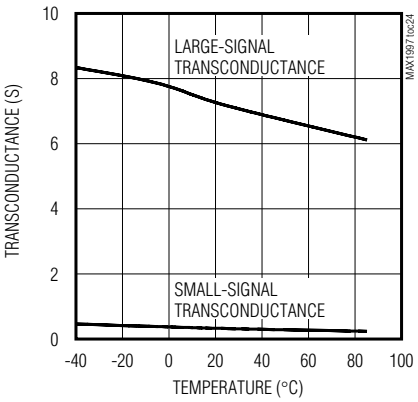
REFERENCE VOLTAGE vs. LOAD CURRENT



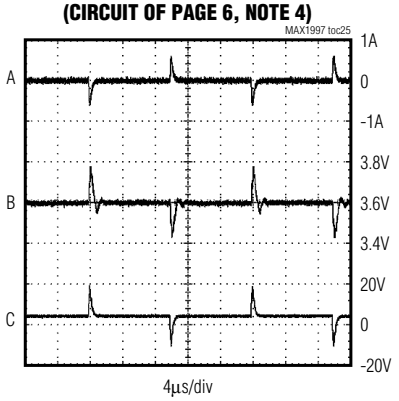
LX CURRENT LIMIT vs. INPUT VOLTAGE



VCOM BUFFER TRANSCONDUCTANCE vs. TEMPERATURE



VCOM LOAD TRANSIENT RESPONSE (CIRCUIT OF PAGE 6, NOTE 4)



A: LOAD CURRENT, 1A/div
B: V_{OUTB} = 3.6V, 200mV/div, AC-COUPLED
C: V_X, 20V/div

Pin Description

PIN		NAME	FUNCTION
MAX1997	MAX1998		
1	—	TGNDB	Internal Connection. Connect this pin to ground. Do not leave this pin floating.
2	1	PGND	Power Ground. PGND is the source of the N-channel power MOSFET. Connect PGND to the star ground at the device's backside pad.
3	—	DRV1	Logic Linear-Regulator (REG 1) Base Drive. Open drain of an internal N-channel MOSFET. Connect DRV1 to the base of an external PNP linear regulator pass transistor. (See the *Pass Transistor Selection* section).

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Pin Description (continued)

PIN		NAME	FUNCTION
MAX1997	MAX1998		
4	—	FB1	Logic Linear-Regulator (REG 1) Feedback Input. FB1 regulates at 1.25V nominal. Connect FB1 to the center tap of a resistive voltage-divider between the REG 1 output and the analog ground (GND) to set the output voltage. Place the resistive voltage-divider close to the pin.
5	2	CT	Sequence Timing Control Input. Connect a capacitor from this pin to GND. This timing capacitor controls the turn-on of REG P, REG N, REG 2, and DRVA. The sequence timing block is enabled, together with the main step-up regulator, when ONDC goes high. Then an internal 5µA current source charges the timing capacitor from 0V to V_{IN}, which sets the turn-on delay. A discharge switch keeps CT at GND when the sequence timing block is disabled. (See the *Power-Up Sequencing and Inrush Current Control* section.)
6	3	$\overline{ONN}$	Gate-Off Linear-Regulator (REG N) Sequence Control Input. REG N is enabled when $\overline{SHDN}$ is high, the gate to the input P-channel MOSFET is low, ONDC is high, and $V_{CT} > V_{\overline{ONN}}$. (See the *Power-Up Sequencing and Inrush Current Control* section.)
7	4	$\overline{ONP}$	Gate-On Linear-Regulator (REG P) Sequence Control Input. REG P is enabled when $\overline{SHDN}$ is high, the gate to the input P-channel MOSFET is low, ONDC is high, and $V_{CT} > V_{\overline{ONP}}$. (See the *Power-Up Sequencing and Inrush Current Control* section.)
8	5	$\overline{ON2}$	Gamma Linear-Regulator (REG 2) Sequence Control Input. REG 2 is enabled when $\overline{SHDN}$ is high, the gate to the input P-channel MOSFET is low, ONDC is high, and $V_{CT} > V_{\overline{ON2}}$. $\overline{ON2}$ also controls the DRVA open-drain output, which is typically used to turn on an N-channel MOSFET between the step-up regulator output and the source driver ICs' supply pins. (See the *Power-Up Sequencing and Inrush Current Control* section.)
9	6	DRVN	Gate-Off Linear-Regulator (REG N) Base Drive. Open drain of an internal P-channel MOSFET. Connect DRVN to the base of an external NPN linear regulator pass transistor. (See the *Pass Transistor Selection* section.)
10	7	FBN	Gate-Off Linear-Regulator (REG N) Feedback Input. FBN regulates to 125mV nominal. Connect FBN to the center tap of a resistive voltage-divider between the REG N output and the reference voltage (REF) to set the output voltage. Place the resistive voltage-divider close to the pin.
11	8	DRVA	Open-Drain Sequence Output. The DRVA open-drain output is controlled by $\overline{ON2}$. DRVA is typically used to turn on an N-channel MOSFET between the step-up regulator output and the source-driver ICs' supply pins. DRVA is high impedance when $\overline{SHDN}$ is high, the gate to the input P-channel MOSFET is low, ONDC is high, and $V_{CT} > V_{\overline{ON2}}$. Otherwise, DRVA connects to ground. (See the *Power-Up Sequencing and Inrush Current Control* section.)
12	9	REF	Internal Reference Bypass Terminal. Connect a 0.22µF ceramic capacitor from REF to the analog ground (GND). External load capability is at least 75µA.
13	10	GND	Analog Ground.
14	—	FBNB	VCOM Buffer Inverting Input. (See the *VCOM Buffer* section.)
15	—	OUTB	VCOM Buffer Output. Requires a minimum 0.47µF ceramic filter capacitor to GND. Place the capacitor as close as possible to OUTB.
16	—	V_{DDB}	VCOM Buffer Supply Input. Bypass to GND with a 0.47µF capacitor as close as possible to the pin.
17	—	FBPB	VCOM Buffer Noninverting Input. (See the *VCOM Buffer* section.)
18	—	FB2	Gamma Linear-Regulator (REG 2) Feedback Input. FBP regulates to 1.25V nominal. Connect FB2 to the center tap of a resistive voltage-divider between the REG 2 output and the analog ground (GND) to set the output voltage. Place the divider close to the pin.

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Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1997	MAX1998		
19	—	DRV2	Gamma Linear-Regulator (REG 2) Base Drive. Open drain of an internal N-channel MOSFET. Connect DRV2 to the base of an external PNP linear regulator pass transistor. (See the *Pass Transistor Selection* section.)
20	11	FB	Main Step-Up Regulator Feedback Input. Connect FB to the center tap of a resistive voltage-divider between the main output (V_{MAIN}) and the analog ground (GND) to set the main step-up regulator output voltage. (See the *Main Step-Up Regulator, Output Voltage Selection* section.) Place the resistive voltage-divider close to the pin.
21	12	FBP	Gate-On Linear-Regulator (REG P) Feedback Input. FBP regulates to 1.25V nominal. Connect FBP to the center tap of a resistive voltage-divider between the REG P output and the analog ground (GND) to set the output voltage. Place the resistive voltage-divider close to the pin.
22	13	DRVP	Gate-On Linear-Regulator (REG P) Base Drive. Open drain of an internal N-channel MOSFET. Connect DRVP to the base of an external PNP linear-regulator pass transistor. (See the *Pass Transistor Selection* section.)
23	14	LX	Switching Node. Drain of the internal N-channel power MOSFET for the main step-up regulator.
24	15	TGNDA	Internal Connection. Connect this pin to ground. Do not leave this pin floating.
25	16	OCN	Overcurrent Comparator Inverting Input. Connect OCN to the center tap of a resistive voltage-divider connected to the drain of the external input protection P-channel MOSFET. (See the *Input Overcurrent Protection* section.) If unused, connect OCN to REF.
26	17	OCP	Overcurrent Comparator Noninverting Input. Connect OCP to the center tap of a resistive voltage-divider connected to the source of the external input protection P-channel MOSFET. The voltage on OCP sets the input overcurrent threshold. (See the *Input Overcurrent Protection* section.) If unused, connect OCP to GND.
27	18	GATE	Gate-Drive Output to the External Input Protection P-Channel MOSFET. (See the *Input Overcurrent Protection* section.) If unused, leave GATE unconnected.
28	—	PFLT	Fault Timer Select Input. Pull PFLT above its logic high threshold ($0.7 \times V_{IN}$) to set the fault delay period to 87ms. Pull PFLT below its logic low threshold ($0.3 \times V_{IN}$) to set the fault delay period to 22ms. Leave PFLT unconnected to set the fault delay period to 44ms. The fault delay period for the MAX1998 is fixed at 87ms.
29	19	IN	Supply Input. The supply voltage powers all the control circuitry. The input voltage range is from 2.7V to 5.5V. Bypass IN to GND with a 0.47µF ceramic capacitor. Place the capacitor within 5mm of IN.
30	—	ONDC	Step-Up Regulator Logic Control Input. The step-up regulator, VCOM buffer, and the sequence timing block are enabled when ONDC is high and disabled when ONDC is low.
31	20	FREQ	Frequency Select Input. Pull FREQ above its logic high threshold ($0.7 \times V_{IN}$) to set the main step-up regulator switching frequency to 1.5MHz. Pull FREQ below its logic low threshold ($0.3 \times V_{IN}$) to set the frequency to 375kHz. Leave FREQ unconnected to set the frequency to 750kHz.
32	—	$\overline{SHDN}$	Active-Low Shutdown Control Input. All the sections of the device are disabled and the GATE pin goes high when $\overline{SHDN}$ is below its 0.4V logic low threshold. Pull $\overline{SHDN}$ above its 1.6V logic high threshold to enable the device. Do not leave $\overline{SHDN}$ unconnected.

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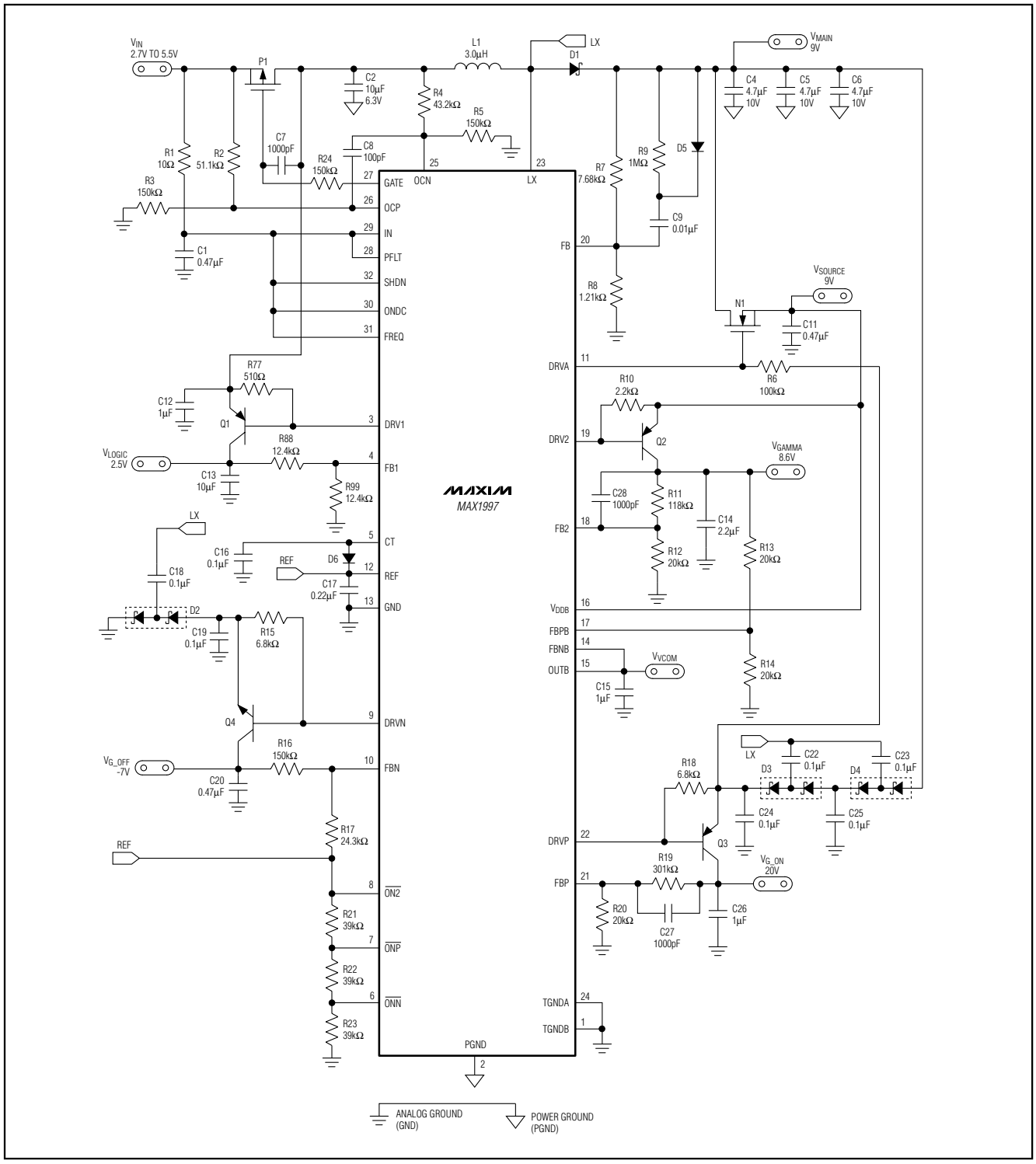

Figure 1. Standard Application Circuit

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Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

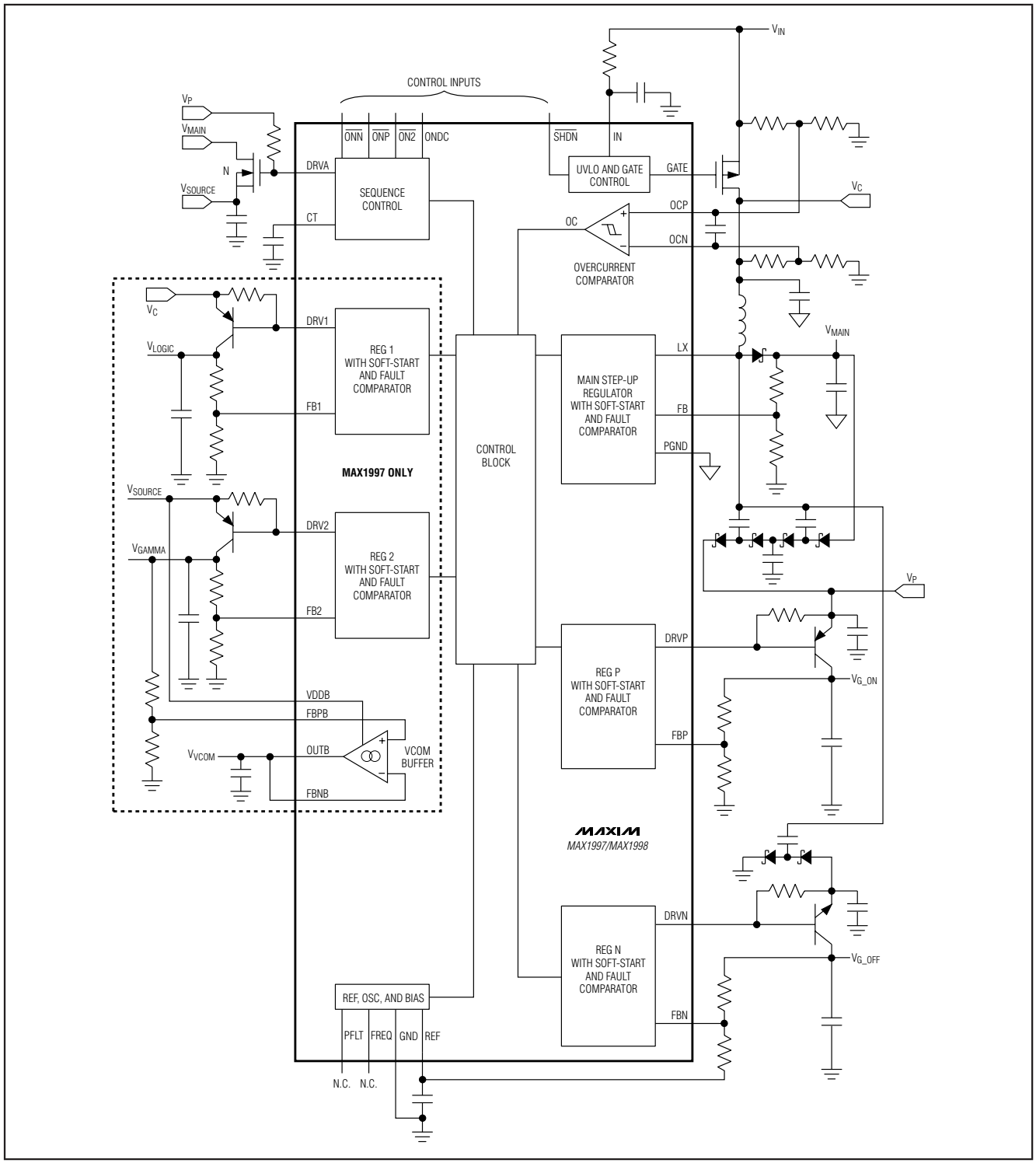

Figure 2. System Functional Diagram

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Table 1. Selected Component List

DESIGNATION	DESCRIPTION
C2, C13	10µF, 6.3V X5R ceramic capacitors (1206), TDK C3216X5R0J106M
C4, C5, C6	4.7µF, 10V X7R ceramic capacitors (1210), Taiyo Yuden LMK352BJ475MF
D1	1.0A, 30V Schottky diode (S-flat), Toshiba CRS02
D2, D3, D4	200mA, 25V dual-series Schottky diodes (SOT23), Fairchild BAT54S
D5, D6	200mA, 75V diode (SOT23), Fairchild MMBD4148
L1	3.0µH, 1.3A inductor, Sumida CLS5D11HP-3R0NC
N1	1.9A, 30V N-channel MOSFET (SuperSOT™-3), Fairchild FDN357P
P1	2.4A, 20V P-channel MOSFET (SuperSOT-3), Fairchild FDN304P
Q1	3A, 25V PNP bipolar transistor (SuperSOT-3), Fairchild FSB749
Q2, Q3	200mA, 40V PNP bipolar transistors (SOT23), Fairchild MMBT3906
Q4	200mA, 40V NPN bipolar transistor (SOT23), Fairchild MMBT3904

SuperSOT is a trademark of Fairchild Semiconductor.

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com

Standard Application Circuit

The standard application circuit (Figure 1) of the MAX1997 is a complete power-supply system for TFT liquid-crystal displays. The circuit generates 9V for source drivers, +20V and -7V for gate drivers, a 2.5V logic supply for the timing controller, a 8.6V gamma reference voltage, and a VCOM buffer. The input voltage range is from 2.7V to 5.5V. Table 1 lists the selected component options and Table 2 lists the component suppliers.

Detailed Description

The MAX1997 and MAX1998 contain a high-performance step-up switching regulator, two low-cost linear-regulator controllers, and multiple levels of protection circuitry. The MAX1997 also includes two additional linear-regulator controllers and a high-current VCOM buffer. Figure 2 shows the MAX1997/MAX1998 system functional diagram. The output voltage of the main step-up regulator (V_{MAIN}) can be set from V_{IN} to 13V with an external resistive voltage-divider. High switching frequency (375kHz/750kHz/1.5MHz) and current-mode control provide fast transient response and allow the use of low-profile inductors and ceramic capacitors.

The low $R_{DS(ON)}$ internal power MOSFET minimizes the external component count and achieves high efficiency using a lossless current-sense architecture.

Two charge pumps take energy from the main step-up regulator's switching node (LX) to generate positive and negative supplies. Additional capacitor and diode stages can be used to generate supply voltages greater than +35V and less than -15V. The positive and negative linear-regulator controllers postregulate the charge-pump supply voltages and allow users to program the power-up sequence as well.

The high-current VCOM buffer of the MAX1997 is ideal for driving the backplane of a TFT LCD panel. It requires only a 0.47µF ceramic output capacitor for stability. The MAX1997's two additional linear-regulator controllers can be used to build the gamma reference and logic supply.

The unique input switch control of the MAX1997/MAX1998 senses the current drawn from the input power supply by monitoring the voltage drop across the input P-channel MOSFET. The protection MOSFET and all regulator outputs latch off if an overcurrent condition lasts for more than the fault timer period.

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Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

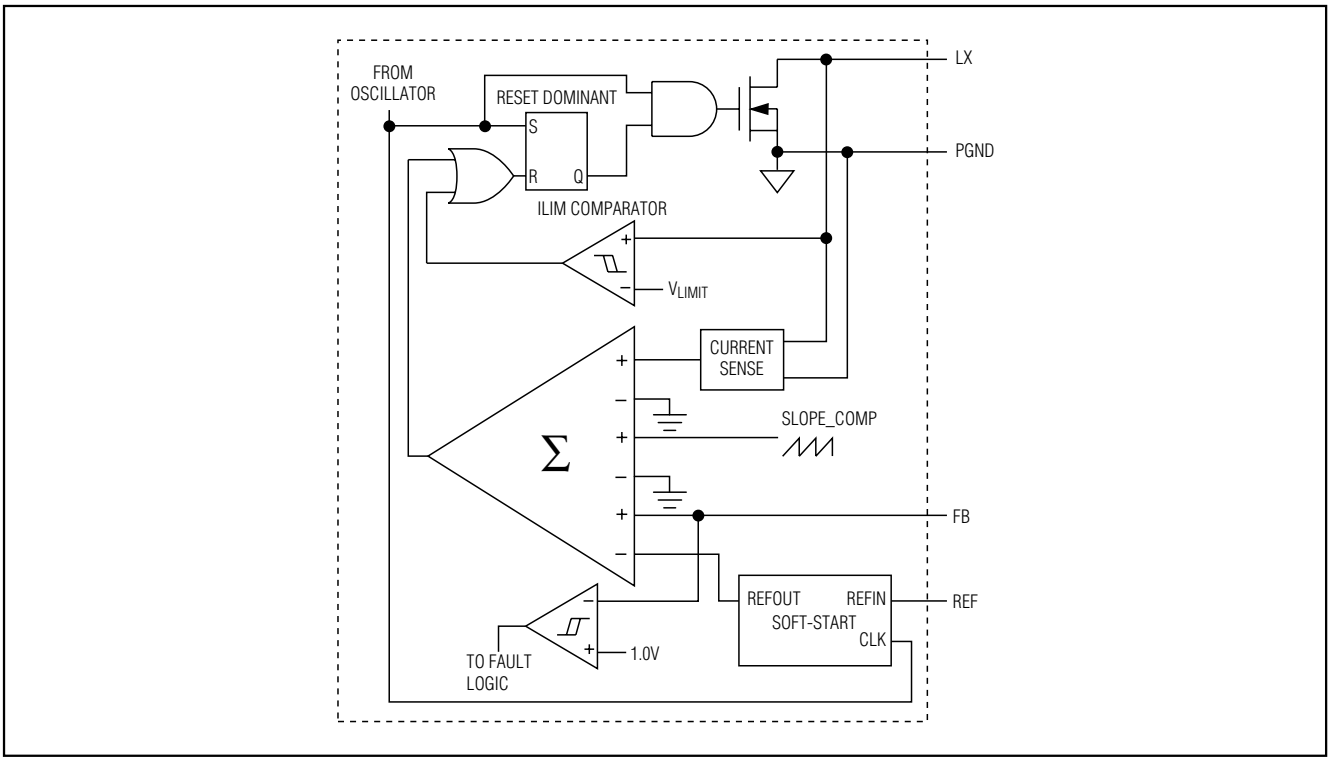

Figure 3. Main Step-Up Converter Functional Diagram

In addition, all outputs are monitored for fault conditions that last longer than the fault timer period. The device goes into a latched shutdown state, if the junction temperature of the device exceeds +160°C.

Main Step-Up Controller

The main step-up regulator switches at up to 1.5MHz, and employs a current-mode control architecture to maximize loop bandwidth and provide fast transient response to pulsed loads found in source drivers for TFT LCD panels. In addition, the high switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET reduces the number of external components. The IC's built-in soft-start function controls the inrush current.

Depending on the input-to-output voltage ratio, the regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the power MOSFET in each switching cycle.

The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

On the rising edge of the internal clock, the controller sets a flip-flop, which turns on the N-channel MOSFET (Figure 3). The input voltage is applied across the inductor. The inductor current ramps up linearly, storing energy in a magnetic field. Once the sum of the feedback voltage, slope-compensation, and current-feedback signals trip the multi-input PWM comparator, the MOSFET turns off, and the flip-flop resets. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

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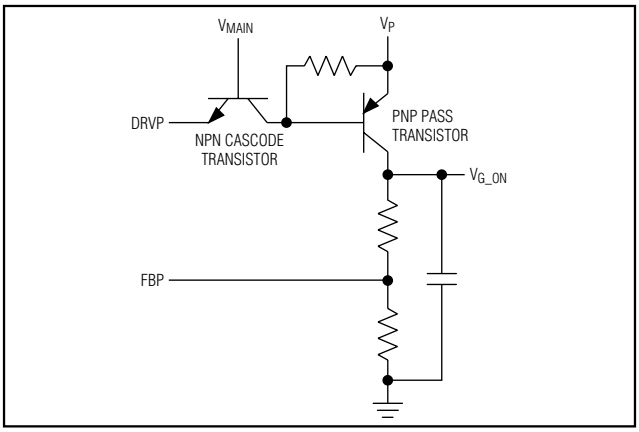

Figure 4. Using Cascode NPN for Output Voltages > 28V

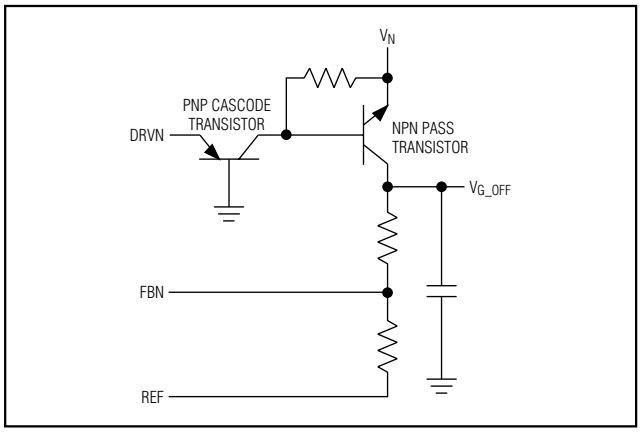

Figure 5. Using Cascode PNP for Output Voltages < VIN - 28V

Positive Linear-Regulator Controller, REG P

The positive linear-regulator controller is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 6.8kΩ base-to-emitter resistor (Figure 1). Its guaranteed base drive sink current is at least 2mA. The regulator is designed to deliver 20mA with an output capacitor of 1µF.

REG P is enabled when $\overline{SHDN}$ is high, the gate to the input P-channel MOSFET is low, ONDC is high, $V_{CT} > V_{\overline{ONP}}$, and the soft-start of the main step-up regulator is complete. (See the *Power-Up Sequencing and Inrush Current Control* section.) Each time it is enabled, the regulator goes through a soft-start routine that ramps up its reference input.

Note that the voltage rating of the DRVP output is 28V. If higher voltages are present, an external cascode NPN transistor should be used with the emitter connected to DRVP, the base to V_{MAIN}, and the collector to the base of the PNP (Figure 4).

REG P is typically used to provide the TFT LCD gate driver's gate-on voltage. A sufficient voltage can be produced using a charge-pump circuit as shown in Figure 1. Use as many stages as necessary to obtain the required output voltage. (See the *Selecting the Number of Charge-Pump Stages* section.)

Negative Linear-Regulator Controller, REG N

The negative linear-regulator controller is an analog gain block with an open-drain P-channel output. It drives an external NPN pass transistor with a 6.8kΩ base-to-emitter resistor (Figure 1). Its guaranteed base drive source current is at least 2mA. The regulator is designed to deliver 20mA with an output capacitor of 0.47µF.

REG N is enabled when $\overline{SHDN}$ is high, the gate to the input P-channel MOSFET is low, ONDC is high, and $V_{CT} > V_{\overline{ONN}}$ (see the *Power-Up Sequencing and Inrush Current Control* section). Each time it is enabled, the regulator goes through a soft-start routine that ramps down its reference input.

Note that the voltage rating of the DRVN output is V_{IN} - 28V. If lower voltages are present, an external cascode PNP transistor should be used with the emitter connected to DRVN, the base to GND, and the collector to the base of the NPN (Figure 5).

REG N is typically used to provide the TFT LCD gate driver's gate-off voltage. A negative voltage can be produced using a charge-pump circuit as shown in Figure 1. Use as many stages as necessary to obtain the required output voltage. (See the *Selecting the Number of Charge-Pump Stages* section.)

Linear-Regulator Controller, REG 1 (MAX1997 Only)

The linear-regulator controller REG 1 is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 510Ω base-to-emitter resistor (Figure 1). Its guaranteed base-drive sink current is at least 5mA. The regulator is designed to deliver 300mA with an output capacitor of 10µF.

REG 1 is enabled when $\overline{SHDN}$ is high and the gate to the input P-channel MOSFET is low. (See the *Power-Up Sequencing and Inrush Current Control* section.) Each time it is enabled, the regulator goes through a soft-start routine that ramps up its reference input. REG 1 is typically used to provide the TFT LCD timing controller's logic supply.

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Quintuple/Triple-Output TFT LCD Power Supplies with Fault Protection and VCOM Buffer

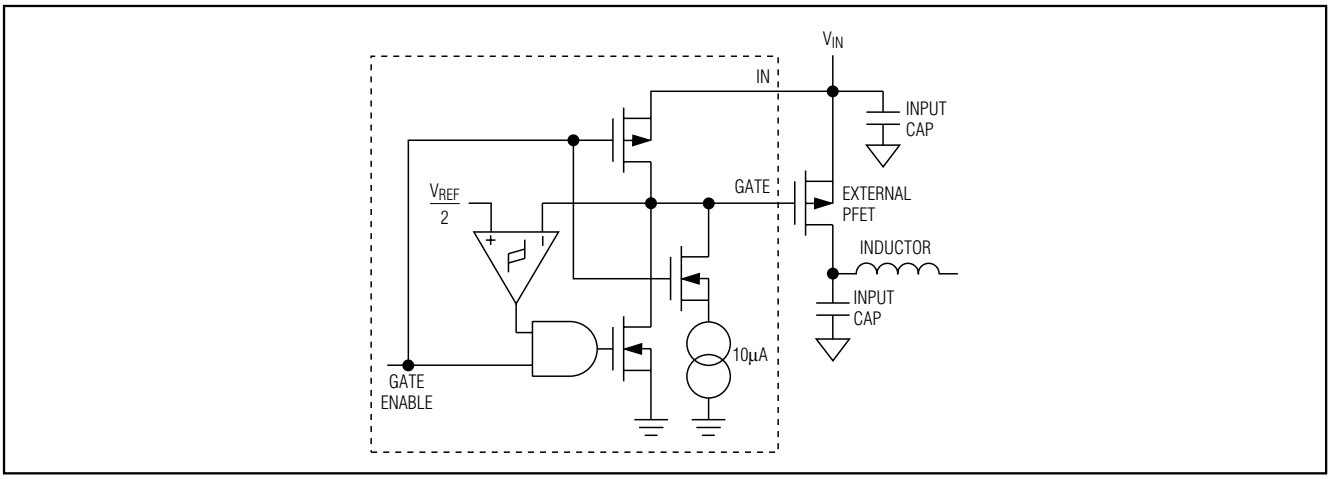

Figure 6. External P-Channel MOSFET Input Switch Control

Linear-Regulator Controller REG 2 (MAX1997 Only)

The linear-regulator controller REG 2 is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 2.2kΩ base-to-emitter resistor (Figure 1). Its guaranteed base drive sink current is at least 5mA. The regulator is designed to deliver 30mA with an output capacitor of 2.2µF.

REG 2 is enabled when $\overline{SHDN}$ is high, the gate to the input P-channel MOSFET is low, ONDC is high, and $V_{CT} > V_{\overline{ON2}}$. (See the *Power-Up Sequencing and Inrush Current Control* section.) Each time it is enabled, the regulator goes through a soft-start routine that ramps up its reference input. REG 2 is typically used to provide the TFT LCD gamma reference voltage.

VCOM Buffer (MAX1997 Only)

The MAX1997 includes a VCOM buffer, which is an operational transconductance amplifier that provides a current output for driving the backplane of a TFT LCD panel. The unity-gain bandwidth of this current-output buffer is:

$$GBW = g_m/C_{OUT}$$

where g_m is the amplifier's transconductance, which is the ratio of the output current to the input voltage. The VCOM buffer requires only a 0.47µF ceramic output capacitor for stability. The bandwidth is inversely proportional to the output capacitance. Thus, large capacitive loads reduce the bandwidth of the buffer output.

In order to improve the transient response time, the amplifier has nonlinear transconductance. The amplifier senses the output current and increases the transconductance as the output current increases. The effect is to provide additional output current when the load demands it.

Undervoltage Lockout (UVLO)

To ensure that the input voltage is high enough for reliable operation, the MAX1997/MAX1998 include an undervoltage lockout (UVLO) circuit. The UVLO threshold at the IN pin is 2.7V (typ) rising and 2.35V (typ) falling. The 350mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, the controller enables the reference block. Once the reference is above 1.05V, an internal 10µA current source pulls the GATE pin low and turns on an external P-channel MOSFET switch (P1, Figure 1) that connects the input supply to the regulator. When the input voltage falls below the UVLO falling threshold, the controller turns off the reference and all the regulator outputs, and pulls GATE high with an internal 100Ω switch to turn off P1 (Figure 6).

Reference Voltage (REF)

The reference output is nominally 1.25V, and can source up to 75µA. (See the *Typical Operating Characteristics*.) Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND.

Oscillator Frequency Control (FREQ)

The internal oscillator frequency is adjustable using the three-level FREQ input. Connect FREQ to ground for 375kHz operation, connect FREQ to V_{IN} for 1.5MHz operation, and leave FREQ unconnected for 750kHz operation. When FREQ is left unconnected, bypass FREQ to ground with a 1000pF to 0.1µF capacitor to prevent switching noise from coupling into the pin's high input impedance. Note that the soft-start period scales with the oscillator frequency. (See the *Soft-Start* section.) The fault timer period does not scale with the oscillator frequency.

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Shutdown (SHDN)

A logic-low signal on the SHDN pin disables all device functions including the reference. During shutdown, the supply current drops to 0.1µA (typ) to maximize battery life. The output capacitance, feedback resistors, and load current determine the rate at which each output voltage decays. A logic-high signal on the SHDN pin activates the MAX1997/MAX1998. (See the *Power-Up Sequencing* section.) Do not leave the SHDN pin floating. Toggling SHDN (below 0.4V) or cycling IN (below 2.2V) clears the fault latch.

Power-Up Sequencing and Inrush Current Control

Once SHDN is pulled high and the input voltage on IN exceeds the rising input UVLO threshold (2.7V typ), the reference turns on. With a 0.22µF REF bypass capacitor, the reference reaches its regulation voltage of 1.25V in approximately 1ms. When the reference voltage is ready, the MAX1997/MAX1998 enable the oscillator and fault detector. After the oscillator is enabled, the controller turns on the external P-channel MOSFET P1 (Figure 1) by pulling GATE low. The GATE is pulled down with a 10µA current source. Add a capacitor from the gate of P1 to its drain to slow down the turn-on rate of the MOSFET, which reduces inrush current.

To guarantee slow turn-on at lower V_{IN}, add a series resistor between the GATE pin and the gate of the external P-channel MOSFET. The typical value of the resistor ranges between 100kΩ and 200kΩ. Once GATE reaches approximately 0.6V, an internal N-channel MOSFET turns on and pulls GATE to ground in order to maximize the enhancement of the external P-channel MOSFET. After P1 fully turns on, REG 1 and the fault counter are enabled.

A logic-high signal on ONDC enables the main step-up regulator and the sequence control block. The sequence control state diagram is shown in Figure 7. The unique sequence control block allows the positive gate-driver voltage (V_{G_ON}), negative gate-driver voltage (V_{G_OFF}), and the source-driver supply voltage (V_{SOURCE}) to be turned on in any order. The capacitor at the CT pin is kept discharged until the main step-up regulator is enabled. An internal 5µA current source starts charging the CT capacitor and the CT voltage ramps linearly up to approximately V_{IN}. REG P, REG N, and REG 2 are enabled when the CT voltage exceeds their associated ON_ control inputs. In addition, the positive linear regulator waits for the completion of the main step-up regulator soft-start. The positive linear regulator is controlled by ONP. The negative linear regulator is controlled by ONN. REG2 and the open-drain output DRVA are controlled by ON2. The DRVA signal can be used to turn on an external N-channel MOSFET (N1, Figure 1), which connects the main step-up regulator output to the source driver's supply pins.

Soft-Start

Each positive regulator (MAIN, REG P, REG 1, and REG 2) includes a 5-bit soft-start DAC whose input is the reference, and whose output is stepped in 32 steps from zero up to the reference voltage. The soft-start DAC of the negative regulator (REG N) steps from the reference down to 125mV in 32 steps. The soft-start duration scales with the switching frequency selected and is 2.73ms for 1.5MHz operation, 5.46ms for 750kHz operation, and 10.92ms for 375kHz operation.

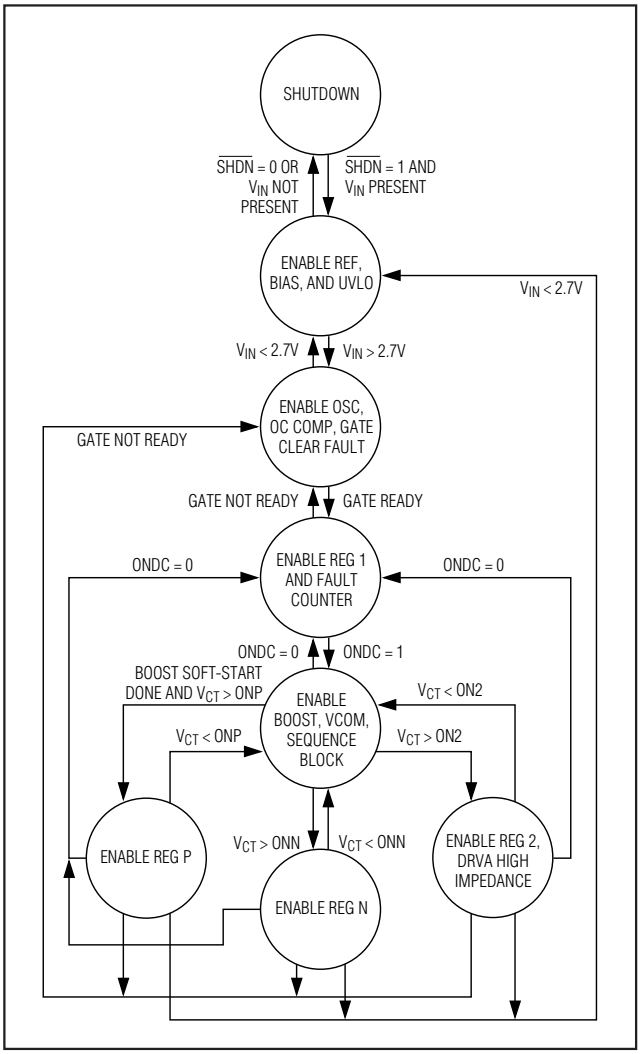

Figure 7. Power-Up Sequence State Diagram

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Table 3. Fault Timer Duration

FREQ PIN	PFLT PIN*	FAULT TIMER DURATION (CLOCK CYCLES)	FAULT TIMER DURATION (ms)
GND	GND	2^{13}	21.8
Unconnected	GND	2^{14}	21.8
IN	GND	2^{15}	21.8
GND	Unconnected	2^{14}	43.6
Unconnected	Unconnected	2^{15}	43.6
IN	Unconnected	2^{16}	43.6
GND	IN**	2^{15}	87.2
Unconnected	IN**	2^{16}	87.2
IN	IN**	2^{17}	87.2

**For MAX1997 only.*
***The MAX1998 has PFLT internally connected high.*

Input Overcurrent Protection

The high-side overcurrent comparator of the MAX1997/MAX1998 provides input overcurrent protection when it is used together with the external P-channel MOSFET switch P1 (Figure 1). Connect resistive voltage-dividers from the source and drain of P1 to GND to set the overcurrent threshold. The center taps of the dividers are connected to the overcurrent comparator inputs (OCN and OCP). See *Setting the Input Overcurrent Threshold* section for information on calculating the resistor values. An overcurrent event activates the fault-protection circuitry. (See the *Fault Protection* section.)

Fault Protection

During steady-state operation, if the output of the main regulator or any of the linear-regulator outputs is below its respective fault detection threshold, or an input overcurrent condition occurs, the MAX1997/MAX1998 activate an internal fault timer (Figure 8). If any condition or the combination of conditions indicates a continuous fault for the fault timer duration (see Table 3), the MAX1997/MAX1998 set the fault latch, shutting down all the outputs except the reference and the oscillator. The fault detection circuit is disabled during the soft-start time of each regulator. Once the fault condition is removed, toggle $\overline{SHDN}$ (below 0.4V) or cycle the input voltage (below 2.2V) to clear the fault latch and reactivate the device.

Thermal Shutdown

The thermal shutdown feature limits total power dissipation in the MAX1997/MAX1998. If the junction temperature T_J exceeds +160°C, a thermal sensor immediately activates the fault protection (Figure 2) and sets the fault latch, which shuts down all the outputs except the reference, allowing the device to cool down. Once the device cools down by at least 15°C, the fault latch can be cleared to reactivate the device. Toggling $\overline{SHDN}$ (below 0.4V) or cycling the input voltage (below 2.2V) clears the fault latch.

Design Procedure

Main Step-Up Regulator

Output Voltage Selection

Set the output voltage by connecting a resistive voltage-divider from the output (V_{MAIN}) to GND with the center tap connected to FB (see Figure 1). Select R8 to be 1.5kΩ or less for optimized transient response. For higher efficiency, increase R8 to 12kΩ and add lag compensation. (See the *Feedback Compensation* section.) Calculate R7 with the following equation:

$$R7 = R8\ [(V_{MAIN} / V_{FB}) - 1]$$

where $V_{FB} = 1.242V - (D \times 20mV)$ and

$D \approx (V_{MAIN} - V_{IN}) / V_{MAIN}$.

For example, if V_{IN} = 3V and D ≈ 0.66, then V_{FB} = 1.229V.

Choosing 1.21kΩ for R8, R7 is 7.65kΩ. Use 7.68kΩ for R7. V_{MAIN} can range from V_{IN} to 13V.

Inductor Selection

The minimum inductance value, peak current rating, series resistance, and size are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. For a switching frequency of 1.5MHz, use values between 1.8µH and 4.7µH. For a switching frequency of 750kHz, use values between 3.3µH and 8.2µH. For a switching frequency of 375kHz, use values between 6.8µH and 15µH.

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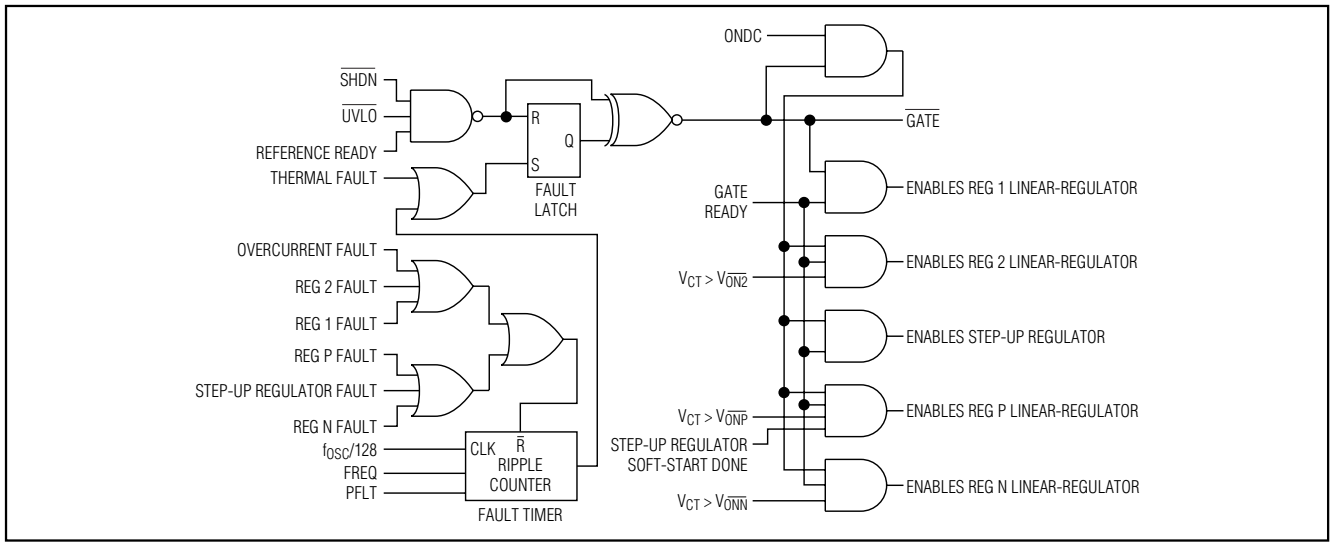

Figure 8. Startup and Fault Protection Logic

The maximum inductor current, input voltage, output voltage, and switching frequency determine the inductor value. To ensure an adequate inductor current-sense signal in the IC, always calculate the inductor value with the maximum guaranteed inductor current even though the actual operating current may be much lower. For the MAX1997/MAX1998, the maximum guaranteed inductor current is the minimum value of the internal LX current limit (1.6A, see the *Electrical Characteristics*). The equations provided here include a constant defined as LIR, which is the ratio of the peak-to-peak inductor current ripple to the average DC inductor current. For a good compromise between the size of the inductor, power loss, and output voltage ripple, select an LIR of 0.3 to 0.5. The inductance value is then given by:

$$L = \left(\frac{V_{IN(TYP)}}{V_{MAIN}}\right)\left(\frac{V_{MAIN} - V_{IN(TYP)}}{I_{L(MAX)} f_{OSC}}\right)\left(\frac{1}{LIR}\right)$$

where f_{OSC} is the oscillator frequency (see *Electrical Characteristics*), and $I_{L(MAX)}$ is 1.6A. Considering the typical application circuit, the typical input voltage is 3.3V, the main output voltage is 9V, and the switching frequency is 1.5MHz. Based on the above equations, the inductance value is 4.3µH for an LIR of 0.2. The inductance value is 1.7µH for an LIR of 0.5. The inductance in the standard application circuit is chosen to be 3.3µH.

The inductor's peak current rating should be higher than the expected peak inductor current throughout the normal operating range. The expected peak inductor current is given by:

$$I_{PEAK} = \left(\frac{I_{MAIN(MAX)} V_{MAIN}}{V_{IN(MIN)}}\right)\left(\frac{1}{\eta}\right) + \left(\frac{1}{2}\right)\left(\frac{V_{IN(MIN)}}{V_{MAIN}}\right)\left(\frac{V_{MAIN} - V_{IN(MIN)}}{L f_{OSC}}\right)$$

where η is the efficiency of the regulator. For most applications, the efficiency is between 75% and 85%.

Under fault conditions, the inductor current may reach the internal LX current limit (see *Electrical Characteristics*). However, soft saturation inductors and the controller's fast current-limit circuitry protect the device from failure during such a fault condition.

The inductor's DC resistance can significantly affect efficiency due to the resistive power loss (P_{LR}), which can be approximated by the following equation:

$$P_{LR} = I_{LAVG}^2 R_L \cong \left(\frac{I_{MAIN} \times V_{MAIN}}{V_{IN}}\right)^2 R_L$$

where I_{LAVG} is the average inductor current and R_L is the inductor's series resistance. For best performance, select inductors with resistance less than the internal N-channel MOSFET's on-resistance (0.25Ω typ). To minimize radiated noise in sensitive applications, use a shielded inductor.

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Output Capacitor

The output capacitor affects the circuit's stability and output-voltage ripple. A 15µF ceramic capacitor works well in most 1.5MHz applications. Depending on the output capacitor chosen, feedback compensation may be required or desirable to increase the loop phase margin or increase the loop bandwidth for transient response. (See the *Feedback Compensation* section.)

The total output-voltage ripple has three components: the inductive ripple caused by the capacitor's equivalent series inductance (ESL), the ohmic ripple due to the capacitor's equivalent series resistance (ESR), and the capacitive ripple caused by the charging and discharging of the output capacitance. Since the ESL is usually very small, the inductive ripple can be neglected:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}, \text{ and}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}} \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}} \right)$$

where I_{PEAK} is the peak inductor current. (See the *Inductor Selection* section.) For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Feedback Compensation

Feedback compensation is not needed for the excellent stability and fast transient response of Figure 1's circuit. However, lead or lag compensation can be useful to compensate for layout issues, or optimize the transient response for various output capacitor or inductor values.

The loop stability of a current-mode step-up regulator can be analyzed by using a small-signal model. In continuous conduction mode, the loop gain transfer function consists of a DC loop gain, a dominant pole, a right-half-plane (RHP) zero, and an ESR zero. In the case of ceramic output capacitors, the ESR zero is at very high frequency and can be ignored. For stable operation, place the dominant pole at a low enough frequency to ensure that the loop gain reaches unity well before the RHP zero, preferably below one-third of the RHP zero frequency f_{Z_RHP}.

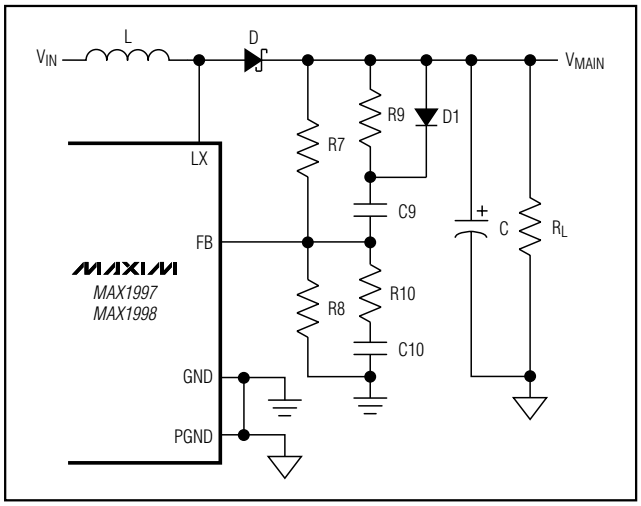

Figure 9. External Compensation

The frequency of the dominant pole is:

$$f_{P_DOMINANT} = \frac{1}{2\pi R_L C}$$

where R_L is the load resistance and C is the output capacitance; the frequency of the RHP zero is:

$$f_{Z_RHP} = (1 - D)^2 \frac{R_L}{2\pi L}$$

where D is the duty cycle and L is the inductance; and the DC gain is given by:

$$A_{DC} = 20 \times \log \left(\frac{R8}{R7 + R8} \times \frac{(1-D)}{R_{CS}} \times R_L \right)$$

where R_{CS} is the 20mΩ internal equivalent current-sense resistor, and R7 and R8 are the feedback divider resistors in Figure 9.

Adding lead compensation (an RC network from V_{MAIN} to FB) increases the loop bandwidth, which can increase the speed of response to transients. Too much speed can destabilize the loop and is not needed or recommended for Figure 1's components.

Lead compensation adds a zero-pole pair, providing gain at higher frequencies and increasing loop bandwidth. The frequencies of the zero and pole for lead compensation depend on the feedback divider resistors and the RC network between V_{MAIN} and FB (Figure 9).

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The frequencies of the zero and pole for the lead compensation are:

$$f_{Z_LEAD} = \frac{1}{2\pi\ (R7+R9)\times C9}$$

$$f_{P_LEAD} = \frac{1}{2\pi\left(R9+\frac{R7\times R8}{R7\times R8}\right)\times C9}$$

At high frequencies, R9 is effectively in parallel with R7, determining the amount of added high-frequency gain. If R9 is very large, there is no added gain and as R9 approaches zero, the added gain approaches the inverse of the feedback divider's attenuation. A typical value for R9 is greater than half of R7. The value of C9 determines the frequency placement of the zero and pole. A typical value of C9 is between 100pF and 10nF. When adding lead compensation, always check the loop stability by monitoring the transient response to a pulsed output load.

Adding lag compensation (an RC network from FB to ground) decreases the loop bandwidth and improves FB noise immunity. Lag compensation slows the transient response but can increase stability margin, which can be needed for particular component choices, a poor layout, or high values of FB divider resistors (R8 greater than 1.5kΩ).

Lag compensation adds a pole-zero pair, attenuating gain at higher frequencies and lowering loop bandwidth. The frequencies of the pole and zero for lag compensation depend on the feedback divider resistors and the RC network between FB and GND (Figure 9).

The frequencies of the pole and zero for the lag compensation are:

$$f_{P_LAG} = \frac{1}{2\pi\left(R10+\frac{R7\times R8}{R7+R8}\right)\times C10}$$

$$f_{Z_LAG} = \frac{1}{2\pi(R10\times C10)}$$

At high frequencies, R10 is effectively in parallel with R8, increasing the divider attenuation ratio. If R10 is very large, the attenuation ratio remains unchanged and as R10 approaches zero, the attenuation ratio approaches infinity. A typical value for R10 is greater than 0.1 times R8. If high-value divider resistors are used, choose R10 < 1.5kΩ for FB noise immunity. The value of C10 determines the frequency placement of the pole and zero. A typical value of C10 is between 100pF and 1000pF.

When adding lag compensation, always check the loop stability by monitoring the transient response to a pulsed output load.

The circuit of Figure 1 works well without compensation. The circuit of Figure 9 uses lag compensation to allow higher value FB divider resistors, at the expense of transient response speed, potentially requiring higher value output capacitors (see *Typical Operating Characteristics*). Using one of these two circuits is recommended.

Using Compensation for Improved Soft-Start

The digital soft-start of the main step-up regulator limits the average input current during startup. If even smoother startup is needed, add a low-frequency lead compensation network (Figure 9). The improved soft-start is active only during startup when the output voltage rises. Positive changes in the output are instantaneously coupled to the FB pin through D1 and feed-forward capacitor C9. This arrangement generates a smoothly rising output voltage. When the output voltage reaches regulation, capacitor C9 charges up through R9 and diode D1 turns off. If desired, C9 and R9 can be chosen also to provide some lead compensation in normal operation. In most applications, lead compensation is not needed, and can be disabled by making R9 large. With R9 much greater than R7, the pole and the zero in the compensation network are very close to one another and cancel out after startup, eliminating the effect of the lead compensation.

Input Capacitor

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the device. A 10µF ceramic capacitor is used in the standard application circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} may be reduced below the values used in the standard applications circuit. Ensure a low-noise supply at the IN pin by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (see R1, C1 in Figure 1).

Rectifier Diode

The MAX1997/MAX1998s' high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 1A Schottky diode complements the internal MOSFET well.

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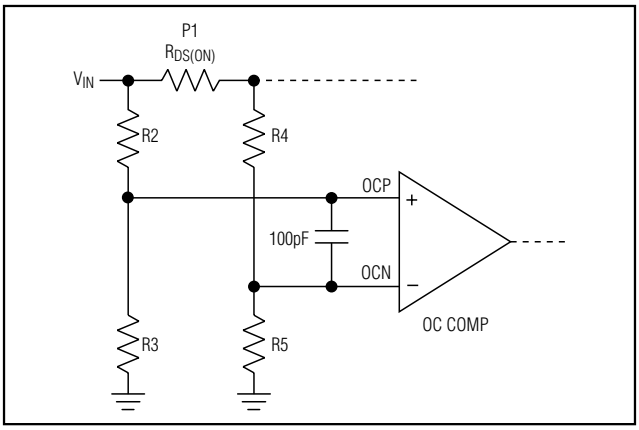

Figure 10. Setting the Overcurrent Threshold

Input P-Channel MOSFET

Select the input P-channel MOSFET based on current rating, voltage rating, gate threshold, and on-resistance. The MOSFET must be able to handle the peak input current (see the *Inductor Selection* section). The drain-to-source voltage rating of the input MOSFET should be higher than the maximum input voltage. Because the MOSFET conducts the full input current, its on-resistance should be low enough for good efficiency. Use a logic-level or low-threshold MOSFET to ensure that the switch is fully enhanced at the lowest input voltage.

Setting the Input Overcurrent Threshold

The high-side comparator of the MAX1997/MAX1998 provides input overcurrent protection when used in conjunction with an external P-channel MOSFET P1. The accuracy of the overcurrent threshold is affected by many factors, including comparator offset, resistor tolerance, input voltage range, and variations in MOSFET $R_{DS(ON)}$. The input overcurrent comparator is only intended to protect against catastrophic failures. This function is similar to an input fuse.

To minimize the impact of the comparator's input offset on the current-sense accuracy, the sense voltage should be close to the upper limit of the comparator's common-mode range (same as the operating range), which extends up to 80% of the input voltage. The resistive voltage divider R4/R5, combined with the on-state resistance of P1, sets the overcurrent threshold. The center of R4/R5 is connected to the inverting input (OCN) as shown in Figure 10.

If the comparator and resistors are ideal, the threshold is at the current where both inputs are equal:

$$V_{IN} \times \frac{R3}{R2+R3} = \left(V_{IN} - I_{L(MAX)} \times R_{DS(MAX)}\right) \times \frac{R5}{R4+R5}$$

$I_{L(MAX)}$ is the average inductor current at maximum load condition and minimum input voltage, and is given by:

$$I_{L(MAX)} = \frac{V_{OUT}}{\eta \times V_{IN(MIN)}} \times I_{LOAD(MAX)}$$

where η is the efficiency of the main step-up regulator.

If the step-up regulator's minimum input voltage is 2.7V, the output voltage is 9V, and the maximum load current is 0.3A. Assuming 80% efficiency, the maximum average inductor current is:

$$I_{L(MAX)} = \frac{9V}{0.8 \times 2.7V} \times 0.3A = 1.25A$$

$R_{DS(MAX)}$ is the maximum on-state drain-to-source resistance of P1. The maximum $R_{DS(ON)}$ at +25°C can be found in the MOSFET manufacturer's data sheet, but that number does not include the MOSFET's temperature coefficient. Since the resistance temperature coefficient is 0.5%/°C, $R_{DS(MAX)}$ can be calculated with the following equation:

$$R_{DS(MAX)} = R_{DS_25C} \times [1 + 0.005 \times (T_J - 25)]$$

where T_J is the actual MOSFET junction temperature in normal operation due to ambient temperature and self-heating caused by power dissipation. As an example, consider the Fairchild FDN304P, which has a maximum $R_{DS(ON)}$ at room temperature of 70mΩ. If the junction temperature is +100°C, the maximum on-state resistance over temperature is:

$$R_{DS(MAX)} = 70m\Omega\,[1 + 0.005 \times (100 - 25)] = 100m\Omega$$

For given R2 and R3 values, the ideal ratio of R4/R5 can be determined:

$$\frac{R4}{R5} = \frac{R2+R3}{R3} \times \frac{V_{IN} - I_{PEAK(MAX)} \times R_{DS(MAX)}}{V_{IN}} - 1$$

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After including the effects of resistor tolerance, comparator offset, and input voltage variation, the minimum input overcurrent threshold equation is:

$$V_{IN(MIN)} \times \frac{R3 \times (1+\varepsilon)}{R2 \times (1+\varepsilon) + R3 \times (1+\varepsilon)} + 5mV = (V_{IN(MIN)} - I_{L(MAX)} \times R_{DS(MAX)}) \times \frac{R5 \times (1+\varepsilon)}{R4 \times (1+\varepsilon) + R5 \times (1+\varepsilon)}$$

where $V_{IN(MIN)}$ is the minimum expected value of the input voltage, ε is the tolerance of the resistors, and 5mV is the worst-case input offset voltage of the comparator. To simplify the equation, define a constant (k) as follows:

$$k = \frac{1+\varepsilon}{1+\varepsilon}$$

The minimum threshold equation becomes:

$$V_{IN(MIN)} \times \frac{R3}{k \times R2 + R3} + 5mV = (V_{IN(MIN)} - I_{L(MAX)} \times R_{DS(MAX)}) \times \frac{k \times R5}{R4 + k \times R5}$$

Solving for R4/R5 yields:

$$\frac{R4}{R5} = k \times \left(\frac{V_{IN(MIN)} - I_{L(MAX)} \times R_{DS(MAX)}}{V_{IN(MIN)} \frac{R3}{R3 + k \times R2} + 5mV} - 1 \right)$$

The R4/R5 ratio guarantees the required minimum level for $I_{L(MAX)}$. The typical overcurrent threshold is given by:

$$I_{TH_TYP} = \frac{V_{IN(TYP)}}{R_{DS(TYP)}} \times \left[1 - \frac{R3 \times (R4+R5)}{R5 \times (R2+R3)} \right]$$

The following example shows how to apply the above equations in the design. If 1% resistors are used, then ε = 0.01. To set V_{OCP} to be around 75% of V_{IN}, select R2 = 51.1kΩ and R3 = 150kΩ. Assume that the minimum input voltage is 2.7V and the typical input voltage is 3.3V, the average inductor current at maximum load is 1.25A, and the maximum $R_{DS(ON)}$ of P1 is 100mΩ:

$$k = \frac{1 - 0.01}{1 + 0.01} = 0.9802$$

$$\frac{R4}{R5} = 0.9802 \times \left(\frac{2.7V - 1.25A \times 0.1\Omega}{2.7V \times \frac{150\Omega}{150\Omega + 0.9802 \times 51.1k\Omega} + 0.005V} - 1 \right) = 0.2637$$

If R5 =150kΩ, then R4 = 39.2kΩ. The typical overcurrent threshold is:

$$I_{TH_TYP} = \frac{3.3V}{0.047\Omega} \times \left[1 - \frac{150\Omega \times (39.2k\Omega + 150\Omega)}{150\Omega \times (51.1k\Omega + 150\Omega)} \right] = 4.15A$$

Charge Pumps

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement. The number of positive charge-pump stages is given by:

$$N_{POS} = \frac{V_{G_ON} + V_{DROPOUT} - V_{MAIN}}{V_{MAIN} - 2 \times V_D}$$

where N_{POS} is the number of positive charge-pump stages, V_{G_ON} is the positive linear-regulator (REG P) output, V_{MAIN} is the main step-up regulator output, V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 2V.

The number of negative charge-pump stages is given by:

$$N_{NEG} = \frac{-V_{G_OFF} + V_{DROPOUT}}{V_{MAIN} - 2 \times V_D}$$

where N_{NEG} is the number of negative charge-pump stages, V_{G_OFF} is the negative linear-regulator (REG N) output, V_{MAIN} is the main step-up regulator output, V_D is the forward-voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 2V.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{MAIN} and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to V_{IN} or another available supply. If the first charge-pump stage is powered from V_{IN}, then the above equations become:

$$N_{POS} = \frac{V_{G_ON} + V_{DROPOUT} - V_{IN}}{V_{MAIN} - 2 \times V_D}$$

$$N_{NEG} = \frac{-V_{G_OFF} + V_{DROPOUT} + V_{IN}}{V_{MAIN} - 2 \times V_D}$$

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Flying Capacitors

Increasing the flying capacitor (C_X) value increases the output current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and the diode impedance limit the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > N \times V_{MAIN}$$

where N is the stage number in which the flying capacitor appears, and V_{MAIN} is the main output voltage. For example, the two-stage positive charge pump in the typical application circuit (Figure 1) where V_{MAIN} = 9V contains two flying capacitors. The flying capacitor in the first stage (C25) requires a voltage rating greater than 9V. The flying capacitor in the second stage (C24) requires a voltage rating greater than 18V.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT} \geq \frac{I_{LOAD}}{2f_{OSC}V_{RIPPLE}}$$

where V_{RIPPLE} is the peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diodes

Use Schottky diodes with a current rating equal to or greater than two times the average charge-pump input current. If the loaded charge-pump output voltage is greater than required, some or all of the Schottky diodes can be replaced with low-cost silicon switching diodes with an equivalent current rating. The charge-pump input current is:

$$I_{CP_IN} = I_{CP_OUT} \times N$$

where N is the number of charge-pump stages.

Linear-Regulator Controllers

Output Voltage Selection

Adjust the positive linear-regulator (REG P) output voltage by connecting a resistive voltage-divider from V_{G_ON} to GND with the center tap connected to FBP (Figure 1). Select R20 in the range of 10kΩ to 30kΩ. Calculate R19 with the following equation:

$$R19 = R20\ [(V_{G_ON} / V_{FBP}) - 1]$$

where V_{FBP} = 1.25V.

The output voltages of linear regulators REG 1 and REG 2 can be similarly adjusted.

Adjust the negative linear-regulator (REG N) output voltage by connecting a resistive voltage-divider from V_{G_OFF} to REF with the center tap connected to FBN (Figure 1). Select R17 in the range of 10kΩ to 30kΩ. Calculate R16 with the following equation:

$$R16 = R17\ [(V_{FBN} - V_{G_OFF}) / (V_{REF} - V_{FBN})]$$

where V_{FBN} = 125mV, V_{REF} = 1.25V. REF can source up to 75µA, using a resistor greater than 17kΩ for R17 leaves at least 10µA for other uses.

Pass Transistor Selection

The pass transistor must meet specifications for current gain (β), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = \left(I_{DRV} - \frac{V_{BE}}{R_{BE}}\right)\beta_{MIN}$$

where I_{DRV} is the minimum guaranteed base drive current, V_{BE} is the base-to-emitter voltage of the transistor, and R_{BE} is the pullup resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the *Stability Requirements* section), so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current can be difficult to stabilize and are not recommended. The transistor's input capacitance and input resistance also create a second pole, which could be low enough to make the output unstable when heavily loaded.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator supports. Alternatively, the package's power dissipation could limit the usable maximum input-to-output voltage differential. The maximum power dissipation capability of the transistor's package and mounting must exceed the actual power dissipation in the device. The power dissipation equals the maximum load current times the maximum input-to-output voltage differential:

$$P = I_{LOAD(MAX)}\ (V_{LDOIN} - V_{LDOOUT}) = I_{LOAD(MAX)}\ V_{CE}$$

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Stability Requirements

The MAX1997/MAX1998 linear-regulator controllers use an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the base-emitter resistor, and the output capacitor determine the loop stability.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V(LDO)} = \left(\frac{4}{V_T}\right)\left[1+\left(\frac{I_{BIAS}h_{FE}}{I_{LOAD}}\right)\right]V_{REF}$$

where V_T is 26mV at room temperature, h_{FE} is the pass transistor's DC current gain, and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). Each of the four linear-regulator controllers is designed for a different maximum output current so they have different output drive currents and different bias currents (I_{BIAS}). Each controller's bias current can be found in the *Electrical Characteristics*. The current listed in the Conditions column for the FB_ Regulation Voltage specification is the individual controller's bias current. The base-to-emitter resistor for each controller should be chosen to set the correct I_{BIAS}:

$$R_{BE} = \frac{V_{BE}}{I_{BIAS}}$$

The output capacitor and the load resistance create the dominant pole in the system. However, the internal amplifier delay, the pass transistor's input capacitance, and the stray capacitance at the feedback node create additional poles in the system, and the output capacitor's ESR generates a zero. For proper operation, use the following steps to ensure the linear regulator stability:

1) First, calculate the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE(LDO)} = \frac{1}{2\pi C_{LDO}R_{LOAD}}$$

where C_{LDO} is the output capacitance of the LDO and R_{LOAD} is the load resistance corresponding to the maximum load current.

The unity gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V(LDO)}f_{POLE(LDO)}$$

2) The pole caused by the internal amplifier delay is at about 1MHz:

$$f_{POLE(AMP)} \cong 1MHz$$

3) Next, calculate the pole set by the transistor's input capacitance, the transistor's input resistance, and the base-to-emitter pullup resistor:

$$f_{POLE(CIN)} = \frac{1}{2\pi CIN(R_{BE} \parallel R_{IN})}$$

Because R_{BE} is much greater than R_{IN}, the above equation can be simplified:

$$f_{POLE(CIN)} \approx \frac{1}{2\pi C_{IN}R_{IN}}$$

$$C_{IN} = \frac{g_m}{2\pi f_T}$$

$$R_{IN} = R_\pi = \frac{h_{FE}}{g_m}$$

where g_m is the transconductance of the pass transistor, and f_T is the transition frequency. Both parameters can be found in the transistor's data sheet. Therefore, the equation can be further simplified:

$$f_{POLE(CIN)} = \frac{f_T}{h_{FE}}$$

4) Next, calculate the pole set by the linear regulator's feedback resistance and the capacitance between FB_ and GND (approximately 5pF including stray capacitance):

$$f_{POLE(FB)_P} = \frac{1}{2\pi C_{FB}(R19 \parallel R20)}$$

$$f_{POLE(FB)_1} = \frac{1}{2\pi C_{FB}(R88 \parallel R99)}$$

$$f_{POLE(FB)_2} = \frac{1}{2\pi C_{FB}(R11 \parallel R12)}$$

and

$$f_{POLE(FB)_N} = \frac{1}{2\pi C_{FB}(R16 \parallel R17)}$$

5) Next, calculate the zero caused by the output capacitor's ESR:

$$f_{ESR_ZERO} = \frac{1}{2\pi C_{LDO}R_{ESR}}$$

where R_{ESR} is the equivalent series resistance of C_{LDO}.

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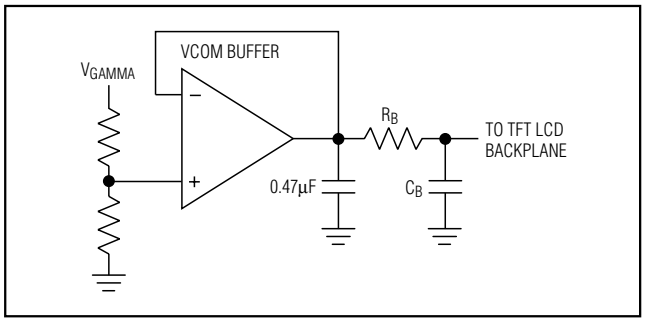

Figure 11. Optimizing VCOM Buffer Drive Current

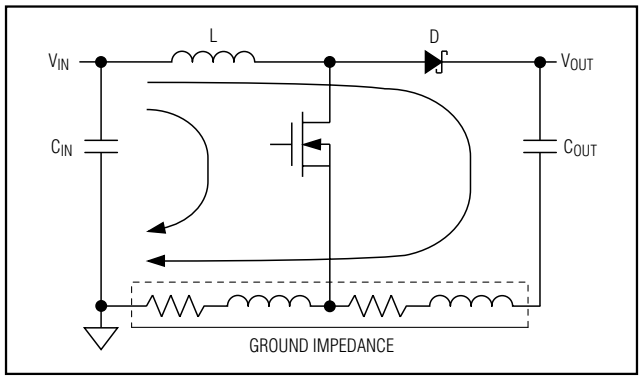

Figure 12. High-Current Loops of Step-Up Regulator

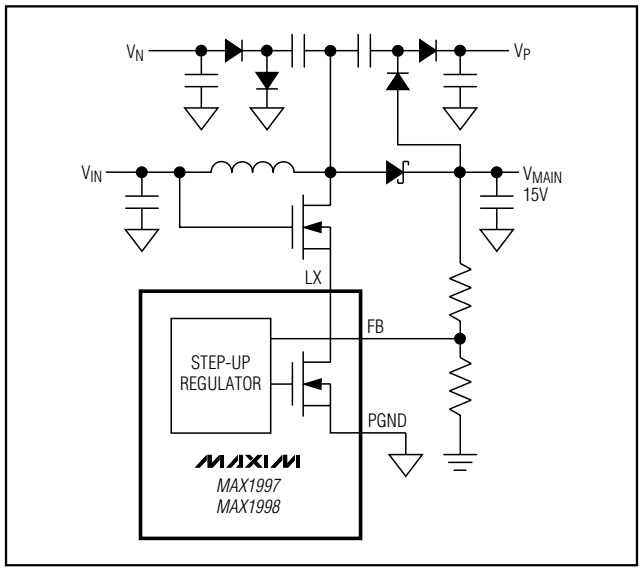

Figure 13. Operation with Output Voltage >13V Using Cascoded MOSFET

6) To ensure stability, choose CLDO large enough so that the crossover occurs well before the poles and zero calculated in steps 2 to 5. The poles in steps 3 and 4 generally occur at several megahertz and using ceramic capacitors ensures the ESR zero occurs at several megahertz as well. Placing the crossover below 500kHz is sufficient to avoid the amplifier-delay pole and generally works well, unless unusual component choices or extra capacitances move the other poles or zero below 1MHz.

A capacitor connected between the regulator output and the feedback node can improve the transient response and reduce the noise coupled into the feedback loop (Figure 1).

If a low-dropout solution is needed, an external P-channel MOS pass transistor can be used for REG 1. However, a PMOS-based linear regulator requires higher output capacitance to stabilize the loop. The high gate capacitance of the P-channel MOSFET lowers $f_{POLE(CIN)}$ and can cause instability. A large output capacitor must be used to reduce the unity-gain bandwidth and ensure that the pole is well above the unity-gain crossover frequency. A ceramic capacitor of at least 30µF is recommended for V_{IN} = 2.7V, V_{OUT} = 2.5V, and I_{LOAD} = 250mA.

VCOM Buffer

Connect the inverting input FBNB directly to the output OUTB to configure the buffer as a voltage follower. Adjust the buffer's output voltage by connecting a voltage-divider from the gamma reference V_{GAMMA} to GND with the center tap connected to the noninverting input FBPB (Figure 1). Select R14 in the 10kΩ to 100kΩ range. Calculate R13 with the following equation:

$$R13 = R14\left[\left(\frac{V_{GAMMA}}{V_{FBPB}}\right) - 1\right]$$

The VCOM buffer is designed to be stable with a 0.47µF capacitor from OUTB to GND. The charge and discharge currents of the VCOM buffer output can be optimized by adding resistor R_B in series with the LCD backplane load and a ceramic capacitor C_B (1µF or larger) in parallel with the backplane load (Figure 11). Start with a 10Ω resistor, then gradually increase the value of R_B, balancing between display quality and buffer power dissipation. Increasing the value of C_B improves the efficiency of the VCOM buffer.

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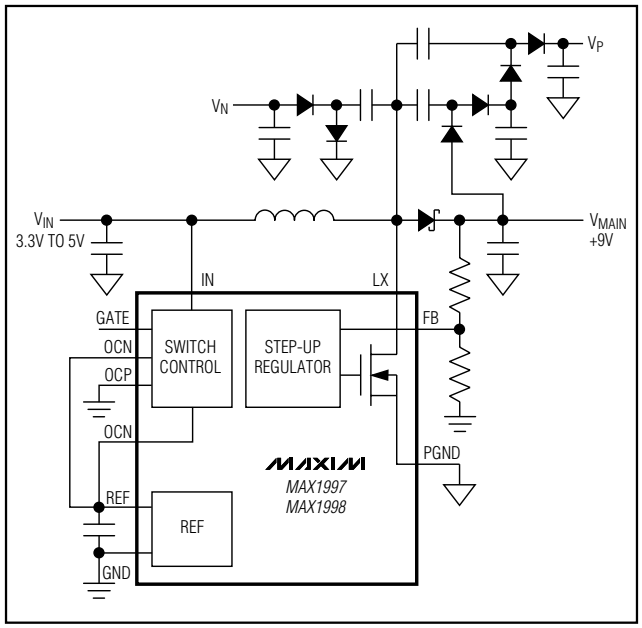

Figure 14. Disabling Input MOSFET Switch

Applications Information

PC Board Layout and Grounding

Careful PC board layout is extremely important for proper operation. Use the following guidelines for good PC board layout:

1) The high-current loops of the main step-up regulators are shown in Figure 12. Minimize the area of these loops by placing the input bypass capacitors, output diode, and output capacitors less than 0.2in (5mm) from the LX and PGND pins. Connect these components with traces as wide as possible. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create islands for the analog ground (GND), power ground (PGND), and linear-regulator ground. Connect all three ground areas (islands) at only one location, which is the backside pad of the device. The REF bypass capacitor and all feedback dividers should be connected to the analog ground island (GND). The step-up regulator's input and output capacitors, and the charge-pump components should be a wide power ground plane. The power ground plane should be connected to the power ground pin (PGND) with a wide trace. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. All the other ground connections, such as the IN pin bypass capacitor and the linear-regulator output capacitors, should be star-connected to the backside of the device with wide traces. Make no other connections between these separate ground planes.
3) Place the IN pin and REF pin bypass capacitors as close to the device as possible.
4) Place all feedback voltage-divider resistors as close to their respective feedback pins as possible. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace parallel to its associated drive trace or near LX or the switching nodes in the charge pumps.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from feedback nodes (FB, FBP, and FBN) and analog ground. Use DC traces as a shield, if necessary. Large ground planes on a multilayer board can provide additional shielding.

Refer to the MAX1997 evaluation kit for an example of proper board layout.

Additional Application Circuits

Operation with Main Output Voltage >13V

The maximum output voltage of the step-up regulator is 13V, which is limited by the absolute maximum rating of the internal power MOSFET. To achieve higher output voltage, an external N-channel MOSFET can be cascoded with the internal FET (Figure 13). Since the gate of the external FET is biased from the input supply, use a logic-level FET to ensure that the FET is fully enhanced at the minimum input voltage. The current rating of the FET needs to be higher than the internal current limit.

Disabling Input MOSFET Switch

If the input protection MOSFET is not needed, disable the input overcurrent comparator by connecting the OCP pin to ground, and the OCN pin to REF. Leave the GATE pin floating (Figure 14).

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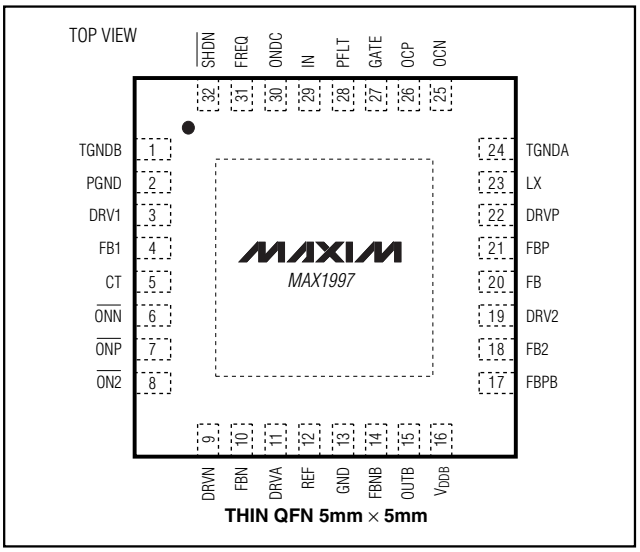
Pin Configurations (continued)



THIN QFN 5mm × 5mm

Chip Information

TRANSISTOR COUNT: 4704

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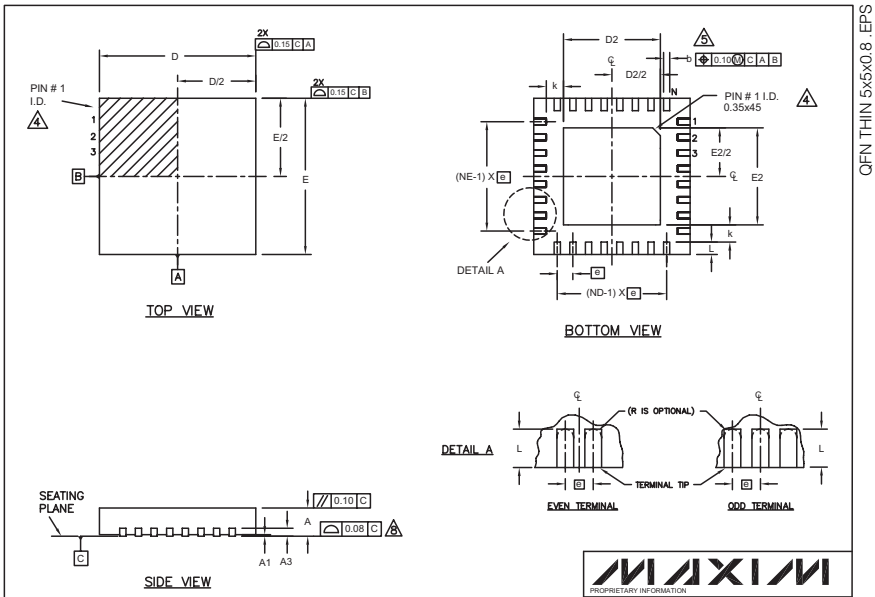
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 5x5x0.8 .EPS



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0140
REV. C
2/2

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