Absolute Maximum Ratings

(All pins referenced to GND)
V_{CC} ..... -0.3V to +6V
$\overline{RESET}$, $\overline{SRESET}$ to GND
Open-Drain ..... -0.3V to +6V
Push-Pull ..... -0.3V to (V_{CC} + 0.3V)
$\overline{MR}$, $\overline{MR1}$, $\overline{MR2}$ ..... -0.3V to +6V
SEL ..... -0.3V to +6V

Input/Output Current (all pins) 20mA
Continuous Power Dissipation (T_A = +70°C) (Multilayer Board)
WLP (derate 10.5mW/°C above +70°C) 840mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 95°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = 1.6V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	$\overline{RESET}$ state guaranteed for $V_{CC} \geq 0.95V$	1.6		5.5	V
V_{CC} Undervoltage Lockout	V_{CCUVLO}			1.25	1.55	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 5V, steady-state condition; $\overline{MR}$, $\overline{MR1}$, $\overline{MR2}$, $\overline{RESET}$, and $\overline{SRESET}$ not asserted		8	10	µA
Supply Current with Oscillator Running	I_{CC2}	V_{CC} = 3V		5	10	µA
V_{CC} Reset Threshold	V_{TH}	V_{CC} falling	-2.5%	V_{TH}	+2.5%	V
V_{CC} Reset Threshold Hysteresis	V_{HYST}			2		%
Reset Threshold Tempco				30		ppm/°C
V_{CC} to $\overline{RESET}$ Output Delay	t_D	V_{CC} falling at 10mV/µs from (V_{TH} + 100mV) to (V_{TH} - 100mV)		10		µs
Reset Timeout Period	t_{RP}	See Table 2	-10	t_{RP}	+10	%
Manual Reset Setup Delay	t_{SU}	Internal timing (see Tables 1a, 1b, 1c)	-10	t_{SU}	+10	%
Debounce Period	t_{DB}		18	20	22	ms

Electrical Characteristics (continued)

(V_{CC} = 1.6V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

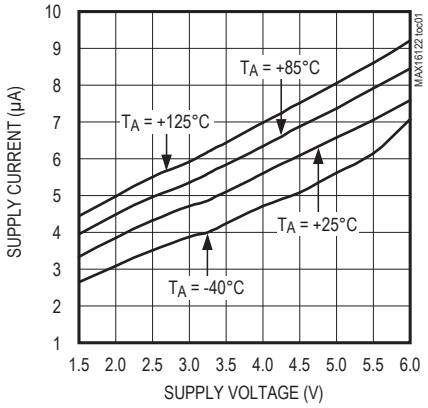
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS ($\overline{RESET}$, $\overline{SRESET}$)						
$\overline{RESET}$, $\overline{SRESET}$ Output Low	V_{OL}	V_{CC} = $V_{TH(MIN)}$, V_{TH} > 4.25V, I_{SINK} = 10mA			0.4	V
		V_{CC} = $V_{TH(MIN)}$, V_{TH} > 2.5V, I_{SINK} = 3.2mA			0.4	V
		V_{CC} = $V_{TH(MIN)}$, V_{TH} > 1.67V, ISINK = 1mA			0.4	V
		V_{CC} = $V_{TH(MIN)}$, V_{TH} > 1V, I_{SINK} = 100µA			0.4	V
		V_{CC} > 0.95V, V_{CC} falling, I_{SINK} = 15µA			0.4	V
$\overline{RESET}$, $\overline{SRESET}$ Output High (Push-Pull Outputs)	V_{OH}	V_{CC} > 0.95V, I_{SOURCE} = 15µA	0.8 x V_{CC}			V
		V_{CC} > 1.2V, I_{SOURCE} = 100µA	0.8 x V_{CC}			V
		V_{CC} > 1.67V, I_{SOURCE} = 150µA	0.8 x V_{CC}			V
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	0.8 x V_{CC}			V
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	0.8 x V_{CC}			V
$\overline{RESET}$, $\overline{SRESET}$ Output Leakage Current (Open-Drain Outputs)					1	µA
MANUAL RESET INPUTS ($\overline{MR}$, $\overline{MR1}$, $\overline{MR2}$)						
$\overline{MR1}$, $\overline{MR2}$, $\overline{MR}$ Input Voltage Low	V_{IL}				0.3 x V_{CC}	V
$\overline{MR1}$, $\overline{MR2}$, $\overline{MR}$ Input Voltage High	V_{IH}		0.7 x V_{CC}			V
Manual Reset Minimum Pulse Width			1			µs
Manual Reset Glitch Rejection				100		ns
Manual Reset to Soft Reset Delay	t_{MRD}			200		ns
$\overline{MR1}$, $\overline{MR2}$, $\overline{MR}$ Internal Pullup Resistance			25	50	80	kΩ
SELECT (SEL) LOGIC INPUT						
SEL Input Low Voltage					0.15 x V_{CC}	V
SEL Input High Voltage			0.85 x V_{CC}			V
SEL Input Leakage			-8		+8	µA

Note 2: All parameters are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

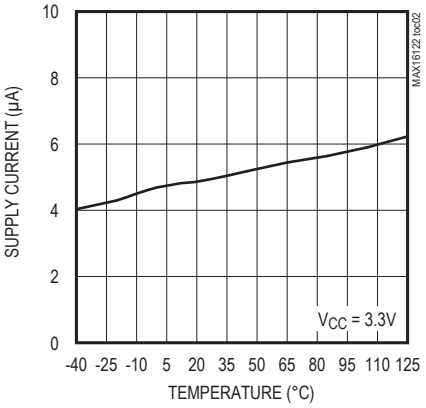
Typical Operating Characteristics

(V_{CC} = 5V, MAX16125WTDB29+, T_A = +25°C, unless otherwise noted.)

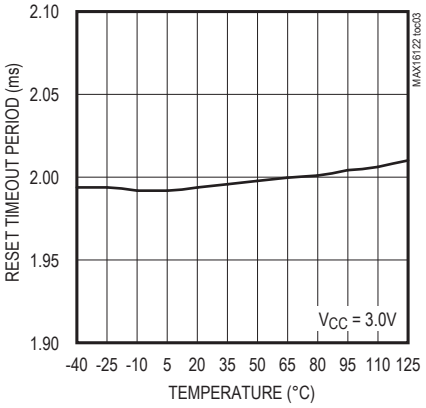
SUPPLY CURRENT vs. SUPPLY VOLTAGE



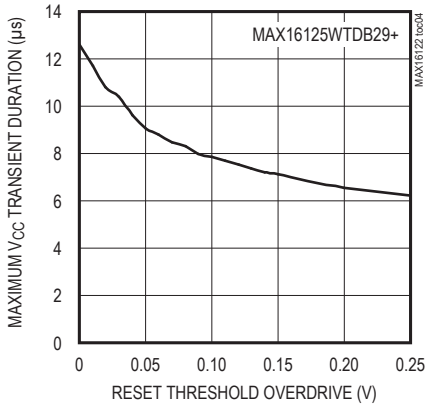
SUPPLY CURRENT vs. TEMPERATURE



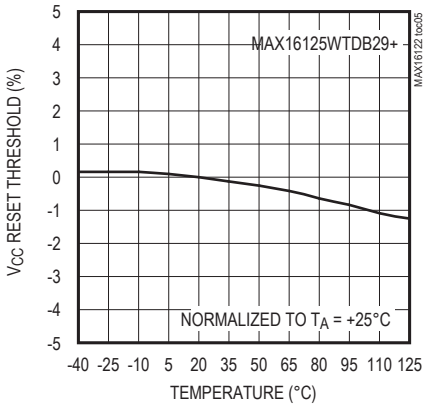
RESET TIMEOUT PERIOD vs. TEMPERATURE



MAXIMUM V_{CC} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



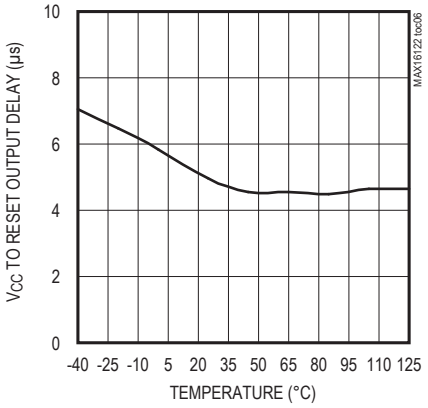
V_{CC} RESET THRESHOLD vs. TEMPERATURE



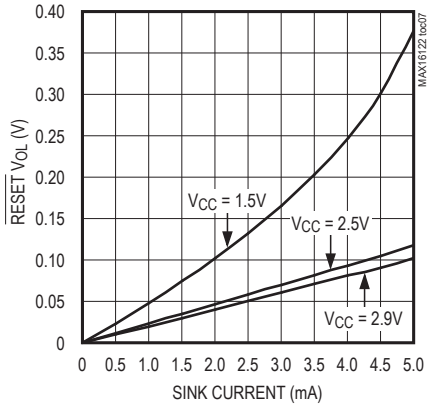
Typical Operating Characteristics (continued)

(V_{CC} = 5V, MAX16125WTDB29+, T_A = +25°C, unless otherwise noted.)

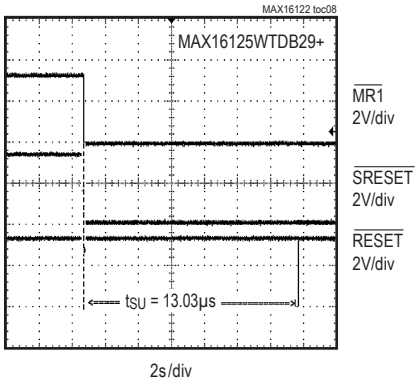
V_{CC} TO RESET OUTPUT DELAY vs. TEMPERATURE



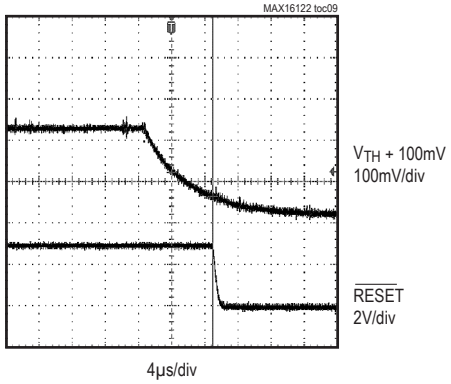
$\overline{RESET}$ OUTPUT-LOW VOLTAGE vs. SINK CURRENT



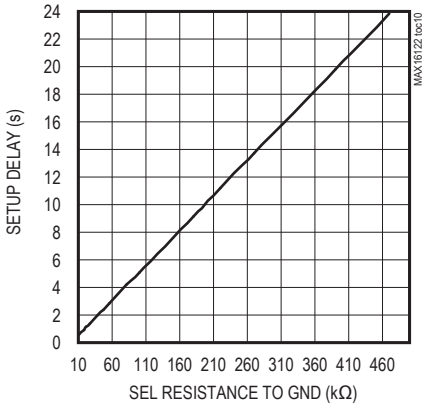
PUSHBUTTON TIMING



V_{CC} TO $\overline{RESET}$ DELAY

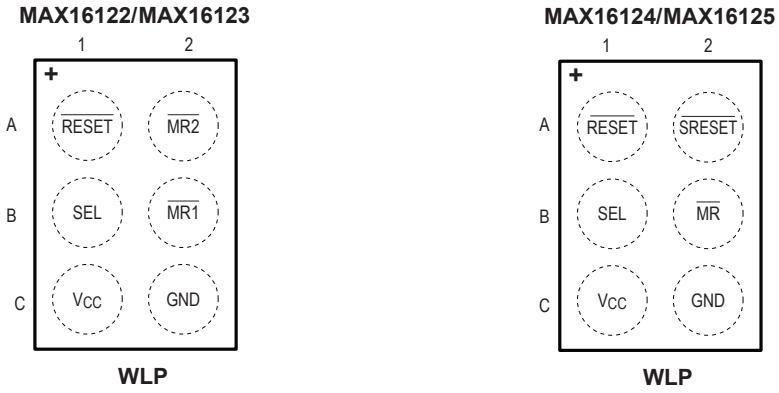


t_{SU} vs. R_{SEL}



Bump Configurations

TOP VIEW
BUMP SIDE DOWN



Bump Description

BUMP		NAME	FUNCTION
MAX16122/ MAX16123	MAX16124/ MAX16125		
A1	A1	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ is either an open-drain or a push-pull output (see the *Selector Guide*). $\overline{\text{RESET}}$ asserts low when V_{CC} drops below the selected threshold and remains low for the V_{CC} reset timeout period after V_{CC} rises above the reset threshold. The $\overline{\text{RESET}}$ one-shot asserts low for the reset timeout period when the manual reset input is asserted longer than the setup delay. The open-drain output requires an external pullup resistor.
—	A2	$\overline{\text{SRESET}}$	Soft Reset Output. $\overline{\text{SRESET}}$ is the debounced version of MR.
B1	B1	SEL	Setup Delay Select Input. Connect SEL to V_{CC}, GND, or leave unconnected to select a desired setup delay (see Table 1a); or connect an external resistor between SEL and GND to select a desired setup delay (E suffix only, see Tables 1a and 1b).
—	B2	$\overline{\text{MR}}$	Manual Reset Input. Internal 50kΩ pullup to V_{CC}. Pull $\overline{\text{MR}}$ low for the setup delay (t_{SU}) to one-shot pulse $\overline{\text{RESET}}$ for the reset timeout period.

Pin Description (continued)

BUMP		NAME	FUNCTION
MAX16122/ MAX16123	MAX16124/ MAX16125		
C1	C1	V_{CC}	Power-Supply Input. V_{CC} provides power to the device and is also a monitored voltage. When V_{CC} drops below the selected threshold, $\overline{RESET}$ asserts low and remains low for the reset timeout period after V_{CC} rises above the threshold. Bypass V_{CC} to GND with a 0.1µF capacitor.
C2	C2	GND	Ground
B2	—	$\overline{MR1}$	Active-Low Manual Reset Input 1. Internal 50kΩ pullup to V_{CC}. Pull both $\overline{MR1}$ and $\overline{MR2}$ low for the setup delay (t_{SU}) to one-shot pulse $\overline{RESET}$ for the reset timeout period.
A2	—	$\overline{MR2}$	Active-Low Manual Reset Input 2. Internal 50kΩ pullup to V_{CC}. Pull the $\overline{MR2}$ and $\overline{MR1}$ low for the setup delay (t_{SU}) to one-shot pulse $\overline{RESET}$ for the reset timeout period.

Detailed Description

The MAX16122–MAX16125 low-current microprocessor reset circuits feature single or dual manual reset inputs with an extended setup period. The devices also feature an internal comparator to monitor 5V, 3.3V, 2.5V, and 1.8V supplies.

When the monitored supply voltage drops below the specified threshold, the active-low $\overline{RESET}$ output asserts low and remains low for the reset timeout period (tRP). The $\overline{RESET}$ output is one-shot pulse asserted for the reset timeout period. For applications that do not require reset timeout period at startup, devices with that configuration are offered. Supply voltage reset threshold is selectable through part suffix, see Table 3.

Connect SEL to GND, V_{CC}, or leave unconnected to select the different setup delays (depending on part suffix, see Table 1a), or connect to an external resistor to set the setup delays (E suffix only, see Table 1b).

The MAX16124/MAX16125 have one manual reset input ($\overline{MR}$), one reset output ($\overline{RESET}$), and one soft reset output ($\overline{SRESET}$). The MAX16122/MAX16123 have two identical manual reset inputs ($\overline{MR1}$ and $\overline{MR2}$) and one reset output ($\overline{RESET}$). A deglitch block is connected to each manual reset input to add a delay to the falling edge with a fixed deglitch period of 20ms (t_{DB}).

Resistor-Adjusted Setup Delay

For the MAX16122–MAX16125 with the E setup delay suffix (MAX1612_WTE_+T), a resistor connected from SEL to GND sets the setup delay. Table 1b shows common resistor values and the resulting setup delays. For resistor values not in the table, use the following formula to compute the setup delay:

$$t_{SU} = \frac{R}{20}$$

where R is the resistor value in kΩ and t_{SU} is the resulting setup delay in seconds. For best results, use resistor values between 10kΩ and 500kΩ.

Reset Output

The reset output is typically connected to the reset input of a microprocessor (µP). A µP's reset input starts or restarts the FP in a known state. The MAX16122–MAX16125 FP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see the *Typical Operating Characteristics*).

The MAX16122/MAX16123 have a reset output $\overline{RESET}$. The MAX16124/MAX16125 have a reset output $\overline{RESET}$ and a soft-reset output $\overline{SRESET}$ which is the debounced "mirror image" of $\overline{MR}$ (see Figure 1a).

All reset outputs are either active-low open-drain or active-low push-pull (see the *Selector Guide*). $\overline{RESET}$ changes from high to low whenever the monitored voltage V_{CC} drops below the reset threshold voltage. Once V_{CC} exceeds its respective reset threshold voltage, $\overline{RESET}$ remains low for the reset timeout period (t_{RP}) and then goes high. $\overline{RESET}$ is one-shot pulsed whenever selected manual reset inputs are asserted longer than the setup delay (t_{SU}). $\overline{RESET}$ stays asserted for the normal reset timeout period.

$\overline{RESET}$ is guaranteed to be in the proper output logic state for $V_{CC} \geq 0.95V$. For applications requiring valid reset logic when V_{CC} is less than 0.95V, see the *Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V (Push-Pull $\overline{RESET}$ Output)* section.

Manual Reset Input

Each device in the MAX16122–MAX16125 family includes at least one manual reset input, which must be held logic-low for an extended setup period (t_{SU}) before the $\overline{RESET}$ output asserts. An internal pullup resistor is connected to each manual reset input. When valid manual reset input conditions/setup periods are met, the $\overline{RESET}$ output is pulsed low for the reset timeout period (see Table 2). Existing front-panel pushbutton switches (i.e., power-on/-off, channel up/down, or mode select) can be used to drive the manual reset inputs. The extended manual reset setup period prevents nuisance system resets during normal front-panel usage or resulting from inadvertent short-term pushbutton closure.

The MAX16124/MAX16125 include a single manual reset input ($\overline{MR}$) and two reset outputs ($\overline{RESET}$ and $\overline{SRESET}$). The MAX16122/MAX16123 include two manual reset inputs ($\overline{MR1}$ and $\overline{MR2}$) and one reset output, $\overline{RESET}$. For dual $\overline{MR1}$ and $\overline{MR2}$ devices, both inputs must be simultaneously pulled low and held for the extended setup period (t_{SU}) before the reset output is pulsed. The dual extended setup provides greater protection from nuisance resets.

The MAX16122–MAX16125 $\overline{RESET}$ output is asserted once for the reset timeout period after each valid manual reset input condition. At least one manual reset input must be released (go high) and then be driven low for the extended setup period before $\overline{RESET}$ asserts again. Internal timing circuitry debounces low-to-high manual reset logic transitions, so no external circuitry is required.

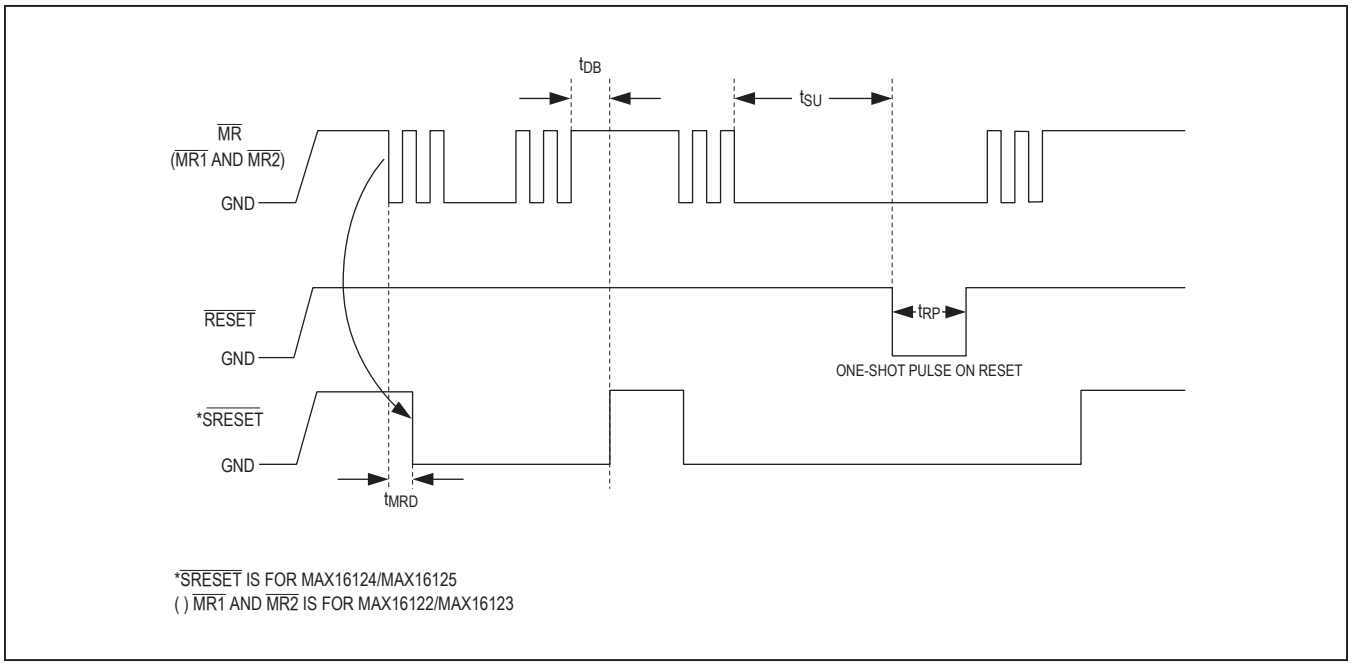


Figure 1a. Reset Timing Diagram

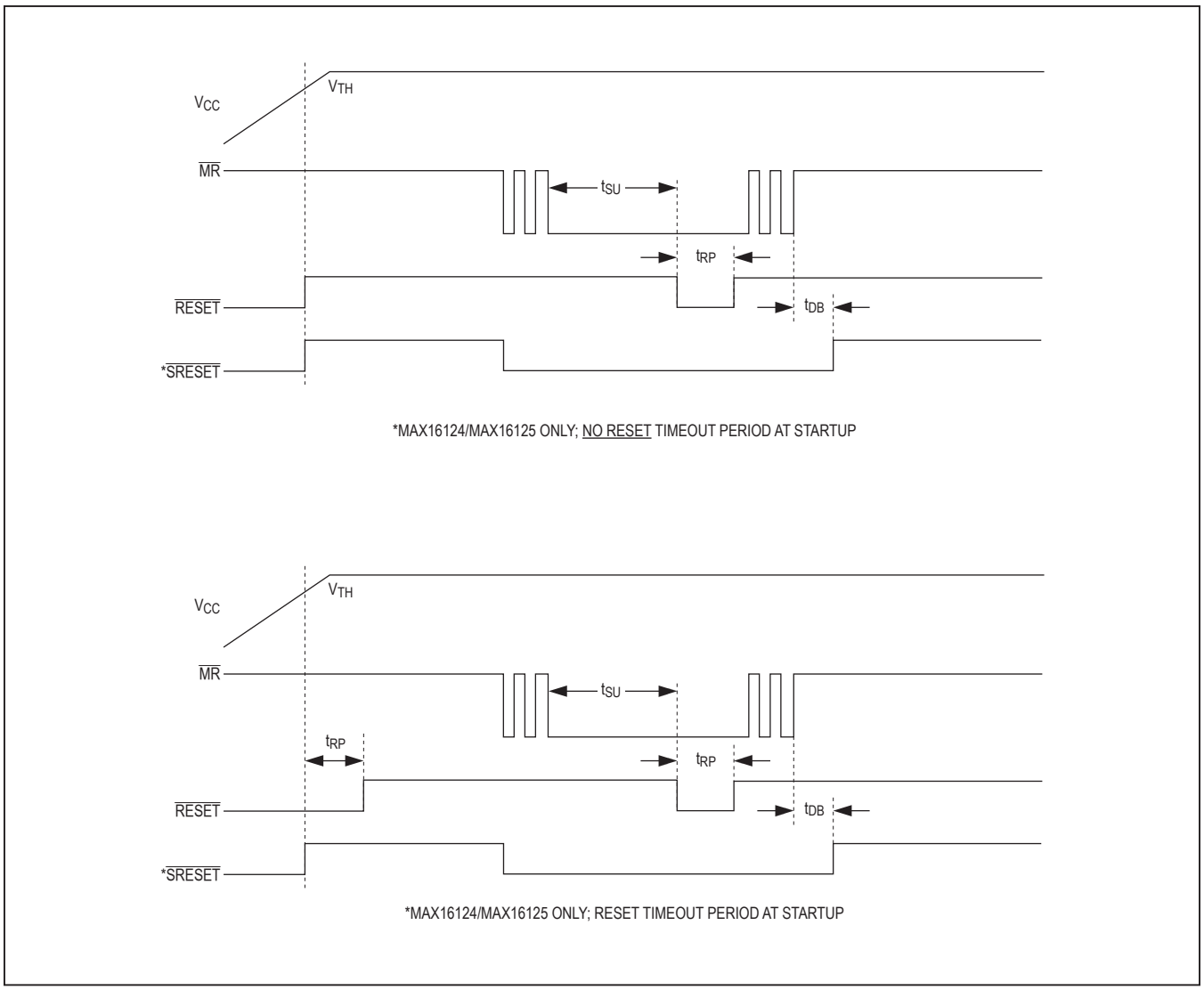


Figure 1b. Timeout Periods at Startup

Supply Voltage Monitor

The MAX16122–MAX16125 have an internal comparator with a programmable trip threshold to monitor the supply voltage. The V_{CC} monitoring thresholds are selectable through the part number suffix (see the *Ordering Information* and Table 3).

Applications Information

Falling V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the MAX16122–MAX16125 are relatively immune to short-duration falling V_{CC} transients (glitches). The *Typical Operating Characteristics* show the Maximum Transient Duration vs. V_{CC} Overdrive graph for which the MAX16122–MAX16125 do not generate a reset pulse. This graph was generated using a falling pulse applied to V_{CC} starting above the actual reset threshold and ending below the threshold by the magnitude indicated (V_{CC} overdrive). The graph indicates the typical maximum pulse width that a falling transient can have without initiating a reset pulse. As the magnitude of the transient increases (go farther below the reset threshold), the maximum allowable pulse width decreases.

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{CC} = 0V (Push-Pull $\overline{\text{RESET}}$ Output)

The MAX16122–MAX16125 guarantee proper operation down to V_{CC} = 0.95V. In applications that require valid reset levels down to V_{CC} = 0V, add a pulldown resistor between $\overline{\text{RESET}}$ and GND for the push-pull outputs (MAX16122/MAX16124). The resistor sinks any stray leakage currents, holding $\overline{\text{RESET}}$ low (Figure 2). The resistor value used is not critical, but it must be small enough not to overload the $\overline{\text{RESET}}$ output when V_{CC} is above the reset threshold. For most applications, use 100kΩ to 1MΩ. This scheme does not work with open-drain outputs of the MAX16123/MAX16125.

Layout and Bypassing

Ensure 0.1µF (minimum) capacitance is connected from V_{CC} to GND.

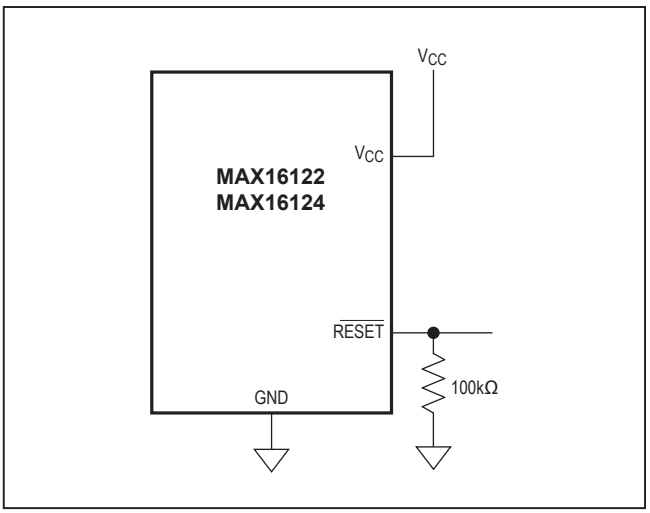
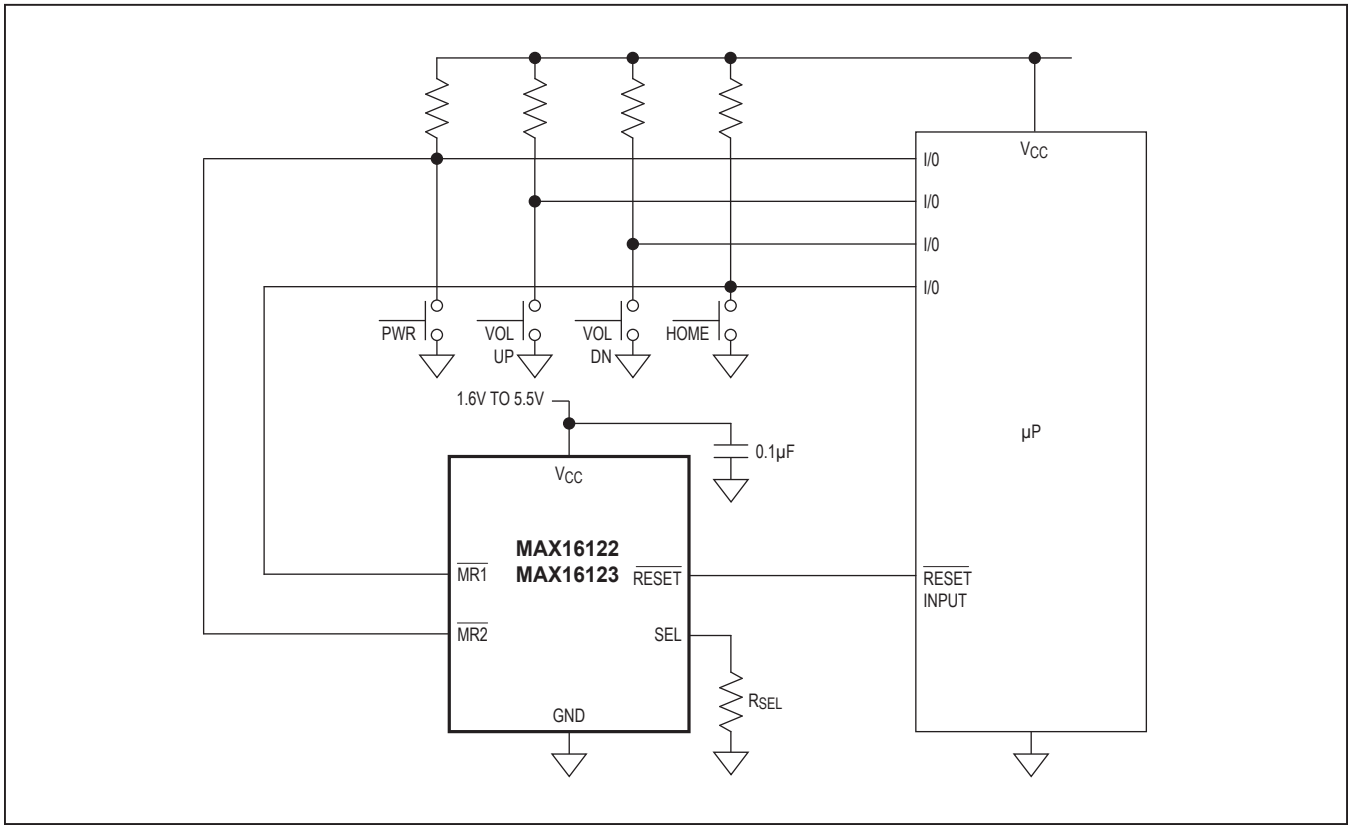
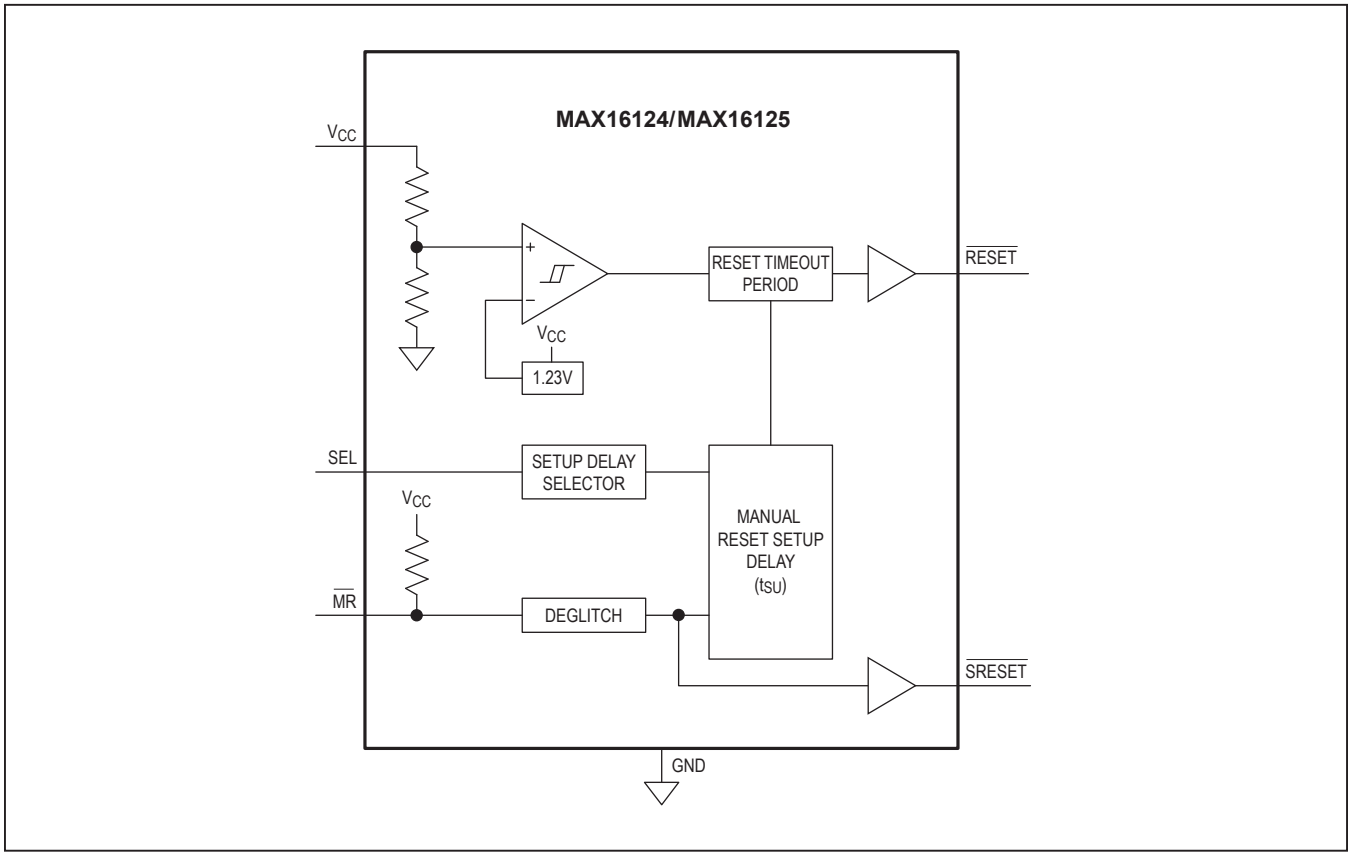


Figure 2. Ensuring $\overline{\text{RESET}}$ Output to V_{CC} = 0V

Typical Operating Circuits (continued)



Functional Diagrams



Functional Diagrams (continued)

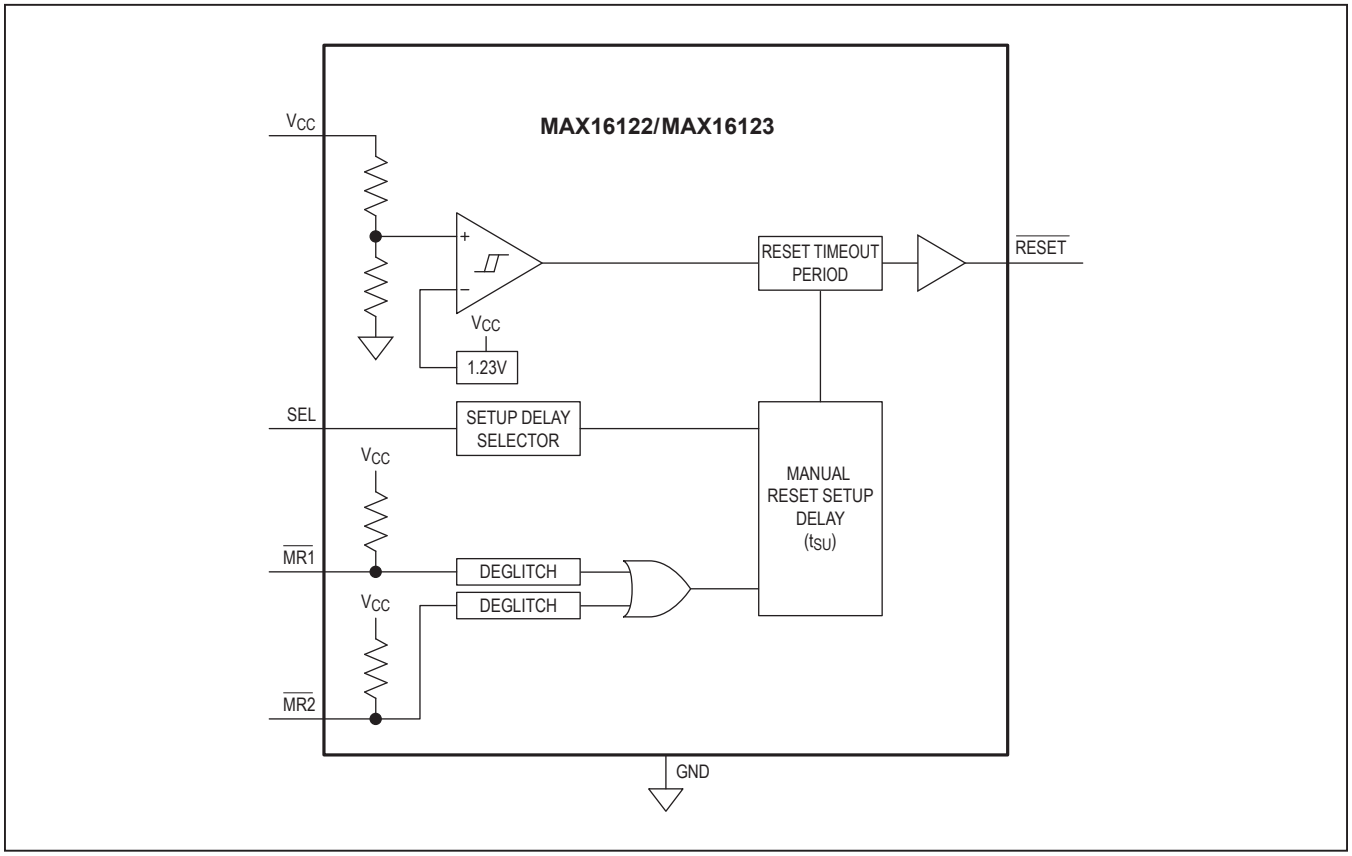


Table 1a. SEL Pin Connection Setup Delays (t_{SU})

PART SUFFIX	SETUP DELAYS (s)		
	SEL = GND	SEL = UNCONNECTED	SEL = V_{CC}
A	0.5	1	2
B	3	4	5
C	6	8	10
D	13	15	17
E	See Table 1b		

Table 1b. Resistor-Adjusted Setup Delays (t_{SU})

RESISTOR (kΩ)	SETUP DELAYS (s)
10	0.5
18	0.9
22	1.1
27	1.35
39	1.95
47	2.35
56	2.8
82	4.1
100	5
180	9
220	11

Table 2. Reset Timeouts (t_{RP})

PART SUFFIX	MINIMUM RESET TIMEOUT (ms)
A	0.9
B	1.8
C	3.6
D	7.2
E	14.4
F	28.8
G	57.6
H	86.4
I	115.2
J	172.8
K	230.4
L	259.2
M	345.6
N	460.8
O	691.2
P	921.6
Q	1843.2
R	3686.4
S	7372.8

Table 3. V_{CC} Reset Threshold Voltage (V_{TH})

SUFFIX	V_{CC} RESET THRESHOLD VOLTAGE (V) (typ)
00	No Monitoring
16	1.58
17	1.67
22	2.19
23	2.32
29	2.93
31	3.08
44	4.38
46	4.63

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16122WT_ _ _ _+T*	-40°C to +125°C	6 WLP
MAX16123WT_ _ _ _+T*	-40°C to +125°C	6 WLP
MAX16124WT_ _ _ _+T*	-40°C to +125°C	6 WLP
MAX16125WT_ _ _ _+T	-40°C to +125°C	6 WLP

Note: *Insert the desired setup delay (A to Q, from Table 1a) into the blank following the letters WT. Insert the letter corresponding to the desired minimum reset timeout period (A to S, from Table 2) into the blank following the setup delay suffix. Insert the two digit number corresponding to the desired nominal reset threshold (from Table 3) into the blanks following the reset timeout suffix.*

+Denotes a lead(Pb)-free/RoHS-compliant package. Devices are available only in lead-free packaging.

T = Tape and reel.

**Future product—Contact factory for availability.*

Selector Guide

PART	DUAL MANUAL RESET INPUT	$\overline{\text{SRESET}}$	SEL	ACTIVE-LOW $\overline{\text{RESET}}$ OUTPUT
MAX16122WT_ _ _ _+T	√	—	√	Push-pull
MAX16123WT_ _ _ _+T	√	—	√	Open-drain
MAX16124WT_ _ _ _+T	—	√	√	Push-Pull
MAX16125WT_ _ _ _+T	—	√	√	Open-drain

Note: *MAX16125WTDB29+T is a standard option. For additional options, please contact factory.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
WLP	W61F0+1	21-0217	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	11/14	No /V OPNs in *Ordering Information*; removed automotive reference from *Applications* section	1
2	4/16	Updated *Electrical Characteristics* table and text	7, 9
3	6/18	Updated *General Description* and *Benefits and Features* sections	1

