Absolute Maximum Ratings

IN to SGND .....-0.3V to +45V
IN to PGND .....-0.3V to +45V
ON/$\overline{OFF}$ to SGND .....-0.3V to (V_{IN} + 0.3V)
OVI, SLOPE, RTCT, SYNC, SS, FB, COMP,
CS to SGND .....-0.3V to (V_{REG5} + 0.3V)
V_{CC} to PGND .....-0.3V to +12V
REG5 to SGND .....-0.3V to +6V
OUT to PGND .....-0.3V to (V_{CC} + 0.3V)
SGND to PGND.....-0.3V to +0.3V
V_{CC} Sink Current (clamped mode) 35mA
OUT Current (< 10µs transient) .....±1.5A

Continuous Power Dissipation* (T_A = +70°C)
16-Pin TSSOP-EP (derate 21.3mW/°C
above +70°C) 1702mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C).....754mW
Operating Junction Temperature Range ..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

**As per JEDEC51 Standard, Multilayer Board.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 16 TSSOP	
Package Code	U16+2
Outline Number	**21-0066**
Land Pattern Number	**90-0117**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	90°C/W
Junction to Case (θ_{JC})	27°C/W
PACKAGE TYPE: 16 TSSOP-EP	
Package Code	U16E+3
Outline Number	**21-0108**
Land Pattern Number	**90-0120**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	38.3°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial.**

Electrical Characteristics

(V_{IN} = 14V, C_{IN} = 0.1µF, C_{VCC} = 0.1µF // 1µF, C_{REG5} = 1µF, $V_{ON/\overline{OFF}}$ = 5V, C_{SS} = 0.01µF, C_{SLOPE} = 100pF, RT = 13.7kΩ, CT = 560pF, V_{SYNC} = V_{OVI} = V_{FB} = V_{CS} = 0V, COMP = unconnected, OUT = unconnected. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to PGND, unless otherwise noted.) (Note 1) (Figure 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Input Supply Range	V_{IN}		4.5		40.0	V
Operating Supply Current	I_Q	V_{IN} = 40V, f_{OSC} = 150kHz		2	3.1	mA
ON/$\overline{OFF}$ CONTROL						
Input-Voltage Threshold	V_{ON}	$V_{ON/\overline{OFF}}$ rising	1.05	1.23	1.40	V
Input-Voltage Hysteresis	$V_{HYST-ON}$			75		mV
Input Bias Current	$I_{B-ON/\overline{OFF}}$	$V_{ON/\overline{OFF}}$ = 40V			0.5	µA
Shutdown Current	I_{SHDN}	$V_{ON/\overline{OFF}}$ = 0V		10	20	µA
INTERNAL 7.4V LDO (V_{CC})						
Output (V_{CC}) Voltage Set Point	V_{VCC}	I_{VCC} = 0 to 20mA (sourcing)	7.15	7.4	7.60	V
Line Regulation		V_{IN} = 8V to 40V		1		mV/V
UVLO Threshold Voltage	$V_{UVLO-VCC}$	V_{CC} rising	3.15	3.5	3.75	V
UVLO Hysteresis	$V_{HYST-UVLO}$			500		mV
Dropout Voltage		V_{IN} = 4.5V, I_{VCC} = 20mA (sourcing)		0.25	0.5	V
Output Current Limit	$I_{VCC-ILIM}$	I_{VCC} sourcing		45		mA
Internal Clamp Voltage	$V_{VCC-CLAMP}$	I_{VCC} = 30mA (sinking)	10.0	10.4	10.8	V
INTERNAL 5V LDO (REG5)						
Output (REG5) Voltage Set Point	V_{REG5}	V_{CC} = 7.5V, I_{REG5} = 0 to 15mA (sourcing)	4.75	4.95	5.05	V
Line Regulation		V_{CC} = 5.5V to 10V		2		mV/V
Dropout Voltage		V_{CC} = 4.5V, I_{REG5} = 15mA (sourcing)		0.25	0.5	V
Output Current Limit	$I_{REG5-ILIM}$	I_{REG5} sourcing		32		mA
OSCILLATOR (RTCT)						
Oscillator Frequency Range	f_{OSC}	f_{OSC} = 2 x f_{OUT} for MAX15004A/B/C/D, f_{OSC} = f_{OUT} for MAX15005A/B/C/D	15		1000	kHz
RTCT Peak Trip Level	$V_{TH,RTCT}$		0.55 x V_{REG5}			V
RTCT Valley Trip Level	$V_{TL,RTCT}$		0.1 x V_{REG5}			V
RTCT Discharge Current	$I_{DIS,RTCT}$	V_{RTCT} = 2V	1.30	1.33	1.36	mA
Oscillator Frequency Accuracy (Note 2)		RT = 13.7kΩ, CT = 4.7nF, f_{OSC} (typ) = 18kHz	-4		+4	%
		RT = 13.7kΩ, CT = 560pF, f_{OSC} (typ) = 150kHz	-4		+4	
		RT = 21kΩ, CT = 100pF, f_{OSC} (typ) = 500kHz	-5		+5	
		RT = 7kΩ, CT = 100pF, f_{OSC} (typ) = 1MHz	-7		+7	
Maximum PWM Duty Cycle (Note 3)	D_{MAX}	MAX15004A/B/C/D			50	%
		MAX15005A/B/C/D RT = 13.7kΩ, CT = 560pF, f_{OSC} (typ) = 150kHz	78.5	80	81.5	
Minimum On-Time	t_{ON-MIN}	V_{IN} = 14V		110	170	ns

Electrical Characteristics (continued)

(V_{IN} = 14V, C_{IN} = 0.1µF, C_{VCC} = 0.1µF // 1µF, C_{REG5} = 1µF, $V_{ON/\overline{OFF}}$ = 5V, C_{SS} = 0.01µF, C_{SLOPE} = 100pF, RT = 13.7kΩ, CT = 560pF, V_{SYNC} = V_{OVI} = V_{FB} = V_{CS} = 0V, COMP = unconnected, OUT = unconnected. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to PGND, unless otherwise noted.) (Note 1) (Figure 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Lock-In Frequency Range (Note 4)		RT = 13.7kΩ, CT = 560pF, f_{OSC} (typ) = 150kHz	102		200	$\%f_{OSC}$
SYNC High-Level Voltage	$V_{IH-SYNC}$		2			V
SYNC Low-Level Voltage	$V_{IL-SYNC}$				0.8	V
SYNC Input Current	I_{SYNC}	V_{SYNC} = 0 to 5V	-0.5		+0.5	µA
SYNC Minimum Input Pulse Width				50		ns
ERROR AMPLIFIER/SOFT-START						
Soft-Start Charging Current	I_{SS}	V_{SS} = 0V	8	15	21	µA
SS Reference Voltage	V_{SS}		1.215	1.228	1.240	V
SS Threshold for HICCUP Enable		V_{SS} rising		1.1		V
FB Regulation Voltage	V_{REF-FB}	COMP = FB, I_{COMP} = -500µA to +500µA	1.215	1.228	1.240	V
FB Input Offset Voltage	V_{OS-FB}	COMP = 0.25V to 4.5V, I_{COMP} = -500µA to +500µA, V_{SS} = 0 to 1.5V	-5		+5	mV
FB Input Current		V_{FB} = 0 to 1.5V	-300		+300	nA
COMP Sink Current	$I_{COMP-SINK}$	V_{FB} = 1.5V, V_{COMP} = 0.25V	3	5.5		mA
COMP Source Current	$I_{COMP-SOURCE}$	V_{FB} = 1V, V_{COMP} = 4.5V	1.3	2.8		mA
COMP High Voltage	$V_{OH-COMP}$	V_{FB} = 1V, I_{COMP} = 1mA (sourcing)	V_{REG5} - 0.5	V_{REG5} - 0.2		V
COMP Low Voltage	$V_{OL-COMP}$	V_{FB} = 1.5V, I_{COMP} = 1mA (sinking)		0.1	0.25	V
Open-Loop Gain	A_{EAMP}			100		dB
Unity-Gain Bandwidth	UGF_{EAMP}			1.6		MHz
Phase Margin	PM_{EAMP}			75		degrees
COMP Positive Slew Rate	SR+			0.5		V/µs
COMP Negative Slew Rate	SR-			-0.5		V/µs
PWM COMPARATOR						
Current-Sense Gain	A_{CS-PWM}	$\Delta V_{COMP}/\Delta V_{CS}$ (Note 5)	2.85	3	3.15	V/V
PWM Propagation Delay to OUT	t_{PD-PWM}	CS = 0.15V, from V_{COMP} falling edge: 3V to 0.5V to OUT falling (excluding leading-edge blanking time)		60		ns
PWM Comparator Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$			50		ns
CURRENT-LIMIT COMPARATOR						
Current-Limit Threshold Voltage	V_{ILIM}		290	305	317	mV
Current-Limit Input Bias Current	I_{B-CS}	OUT= high, 0 ≤ V_{CS} ≤ 0.3V	-2		+2	µA
ILIMIT Propagation Delay to OUT	$t_{PD-ILIM}$	From CS rising above V_{ILIM} (50mV overdrive) to OUT falling (excluding leading-edge blanking time)		60		ns

Electrical Characteristics (continued)

(V_{IN} = 14V, C_{IN} = 0.1µF, C_{VCC} = 0.1µF // 1µF, C_{REG5} = 1µF, $V_{ON/\overline{OFF}}$ = 5V, C_{SS} = 0.01µF, C_{SLOPE} = 100pF, RT = 13.7kΩ, CT = 560pF, V_{SYNC} = V_{OVI} = V_{FB} = V_{CS} = 0V, COMP = unconnected, OUT = unconnected. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to PGND, unless otherwise noted.) (Note 1) (Figure 5)

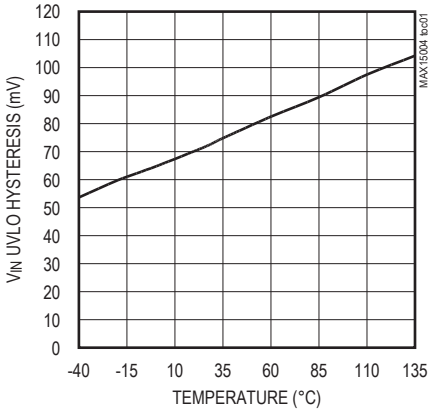
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ILIM Comparator Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$			50		ns
Number of Consecutive ILIMIT Events to HICCUP				7		
HICCUP Timeout				512		Clock periods
SLOPE COMPENSATION (Note 6)						
Slope Capacitor Charging Current	I_{SLOPE}	V_{SLOPE} = 100mV	9.8	10.5	11.2	µA
Slope Compensation		C_{SLOPE} = 100pF		25		mV/µs
Slope Compensation Tolerance (Note 2)		C_{SLOPE} = 100pF	-4		+4	%
Slope Compensation Range		C_{SLOPE} = 22pF		110		mV/µs
		C_{SLOPE} = 1000pF		2.5		
OUTPUT DRIVER						
Driver Output Impedance	R_{OUT-N}	V_{CC} = 8V (applied externally), I_{OUT} = 100mA (sinking)		1.7	3.5	Ω
	R_{OUT-P}	V_{CC} = 8V (applied externally), I_{OUT} = 100mA (sourcing)		3	5	
Driver Peak Output Current	$I_{OUT-PEAK}$	C_{OUT} = 10nF, sinking		1000		mA
		C_{OUT} = 10nF, sourcing		750		
OVERVOLTAGE COMPARATOR						
Overvoltage Comparator Input Threshold	V_{OV-TH}	V_{OVI} rising	1.20	1.228	1.26	V
Overvoltage Comparator Hysteresis	$V_{OV-HYST}$			125		mV
Overvoltage Comparator Delay	TD_{OVI}	From OVI rising above 1.228V to OUT falling, with 50mV overdrive		1.6		µs
OVI Input Current	I_{OVI}	V_{OVI} = 0 to 5V	-0.5		+0.5	µA
THERMAL SHUTDOWN						
Shutdown Temperature	T_{SHDN}	Temperature rising		160		°C
Thermal Hysteresis	T_{HYST}			15		°C

Note 1: 100% production tested at +125°C. Limits over the temperature range are guaranteed by design.
Note 2: Guaranteed by design; not production tested.
Note 3: For the MAX15005A/B/C/D, D_{MAX} depends upon the value of RT. See Figure 3b and the *Oscillator Frequency/External Synchronization* section.
Note 4: The external SYNC pulse triggers the discharge of the oscillator ramp. See Figure 2. During external SYNC, D_{MAX} = 50% for the MAX15004A/B/C/D; for the MAX15005A/B/C/D, there is a shift in D_{MAX} with f_{SYNC}/f_{OSC} ratio (see the *Oscillator Frequency/External Synchronization* section).
Note 5: The parameter is measured at the trip point of latch, with 0 ≤ V_{CS} ≤ 0.3V, and FB = COMP.
Note 6: Slope compensation = $(2.5 \times 10^{-9})/C_{SLOPE}$ mV/µs. See the *Applications Information* section.

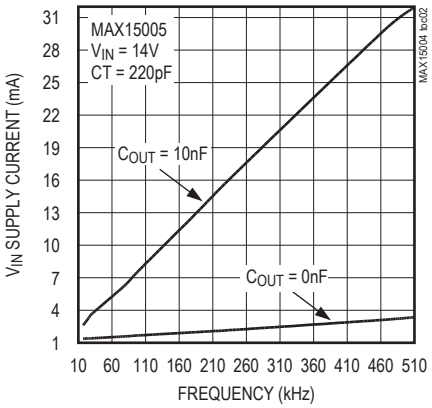
Typical Operating Characteristics

(V_{IN} = 14V, C_{IN} = 0.1µF, C_{VCC} = 0.1µF // 1µF, C_{REG5} = 1µF, $V_{ON/\overline{OFF}}$ = 5V, C_{SS} = 0.01µF, C_{SLOPE} = 100pF, RT = 13.7kΩ, CT = 560pF. T_A = +25°C, unless otherwise noted.)

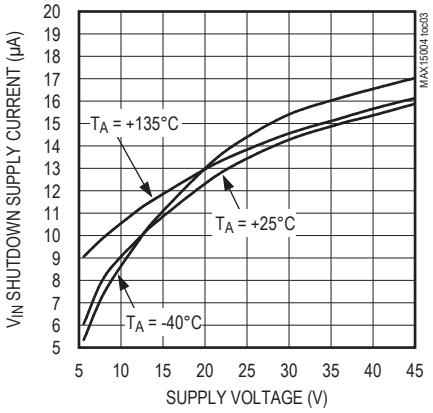
V_{IN} UVLO HYSTERESIS vs. TEMPERATURE



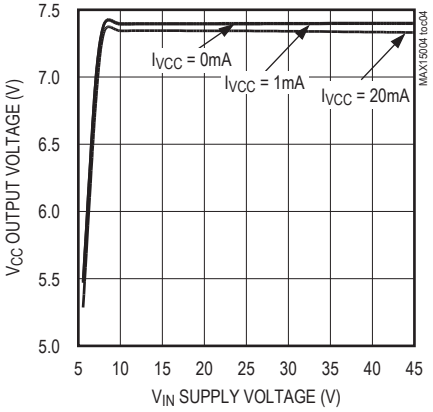
V_{IN} SUPPLY CURRENT (I_{SUPPLY}) vs. OSCILLATOR FREQUENCY (f_{OSC})



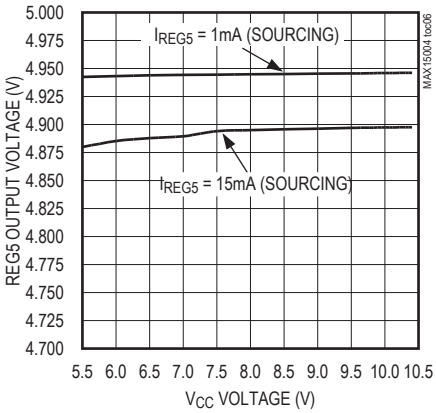
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



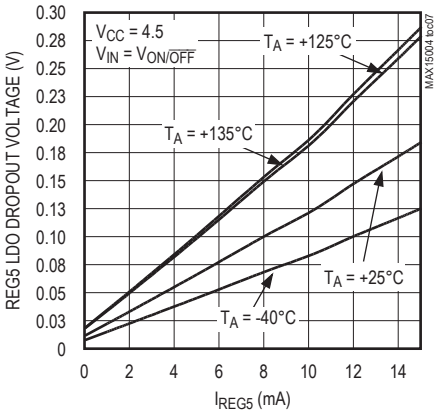
V_{CC} OUTPUT VOLTAGE vs. V_{IN} SUPPLY VOLTAGE



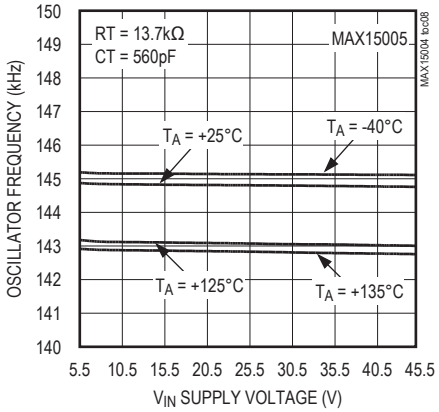
REG5 OUTPUT VOLTAGE vs. V_{CC} VOLTAGE



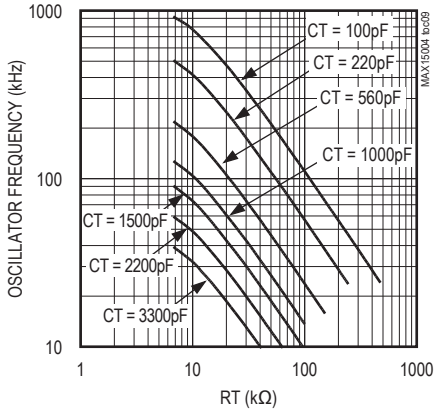
REG5 DROPOUT VOLTAGE vs. I_{REG5}



OSCILLATOR FREQUENCY (f_{OSC}) vs. V_{IN} SUPPLY VOLTAGE



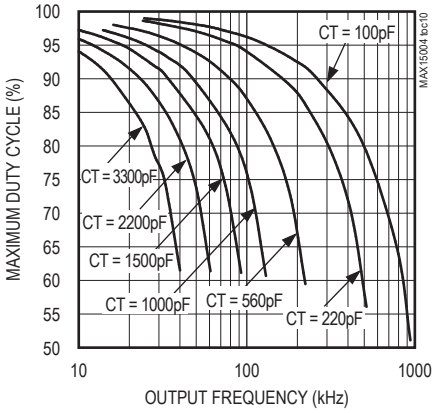
OSCILLATOR FREQUENCY (f_{OSC}) vs. RT/CT



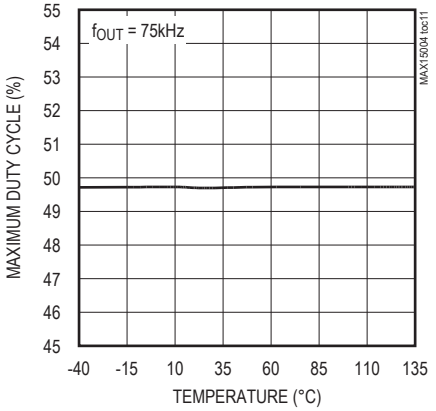
Typical Operating Characteristics (continued)

V_{IN} = 14V, C_{IN} = 0.1µF, C_{VCC} = 0.1µF // 1µF, C_{REG5} = 1µF, $V_{ON/\overline{OFF}}$ = 5V, C_{SS} = 0.01µF, C_{SLOPE} = 100pF, RT = 13.7kΩ, CT = 560pF. T_A = +25°C, unless otherwise noted.)

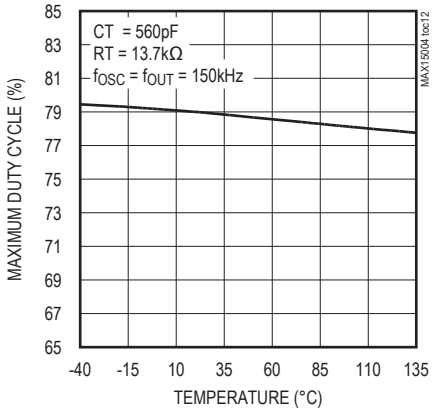
MAX15005 MAXIMUM DUTY CYCLE vs. OUTPUT FREQUENCY (f_{OUT})



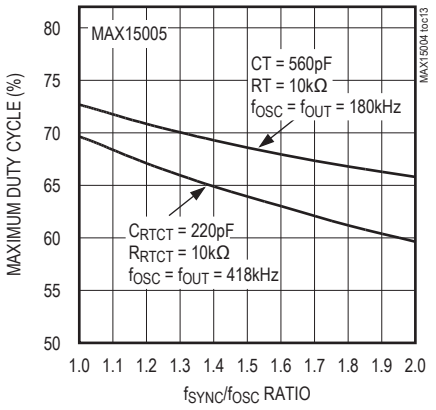
MAX15004 MAXIMUM DUTY CYCLE vs. TEMPERATURE



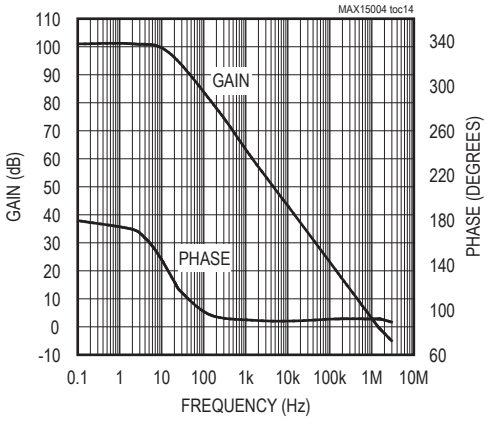
MAX15005 MAXIMUM DUTY CYCLE vs. TEMPERATURE



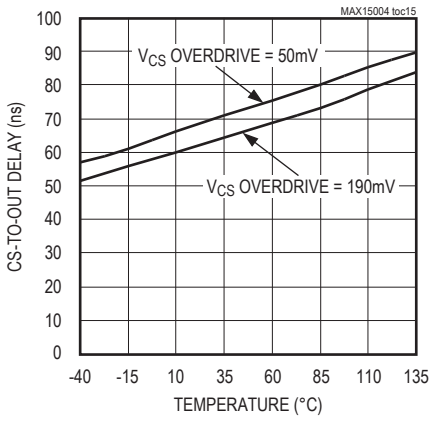
MAXIMUM DUTY CYCLE vs. f_{SYNC}/f_{OSC} RATIO



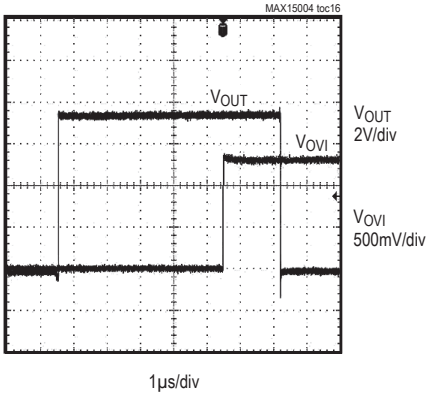
ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



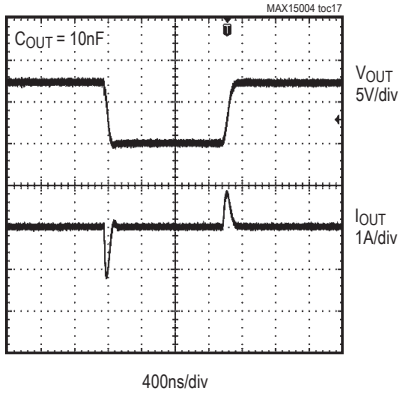
CS-TO-OUT DELAY vs. TEMPERATURE



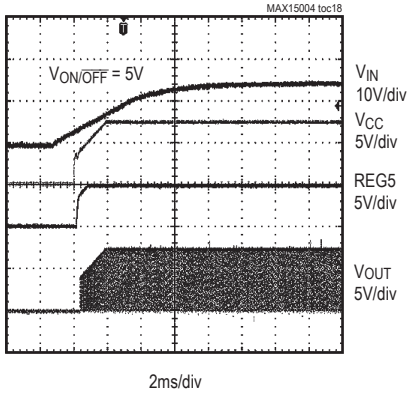
OVI TO OUT DELAY THROUGH OVERVOLTAGE COMPARATOR



DRIVER OUTPUT PEAK SOURCE AND SINK CURRENT



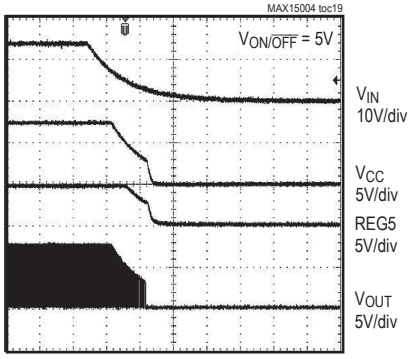
POWER-UP SEQUENCE THROUGH V_{IN}



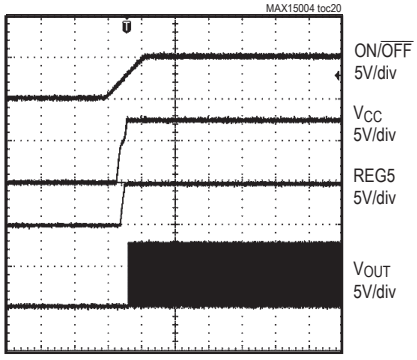
Typical Operating Characteristics (continued)

(V_{IN} = 14V, C_{IN} = 0.1µF, C_{VCC} = 0.1µF // 1µF, C_{REG5} = 1µF, $V_{ON/\overline{OFF}}$ = 5V, C_{SS} = 0.01µF, C_{SLOPE} = 100pF, RT = 13.7kΩ, CT = 560pF. T_A = +25°C, unless otherwise noted.)

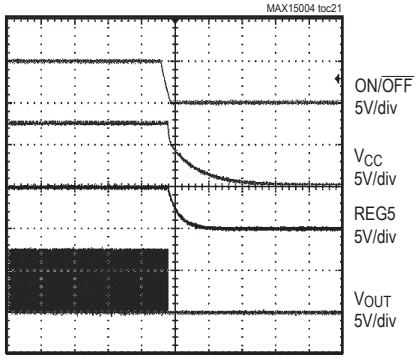
POWER-DOWN SEQUENCE THROUGH V_{IN}



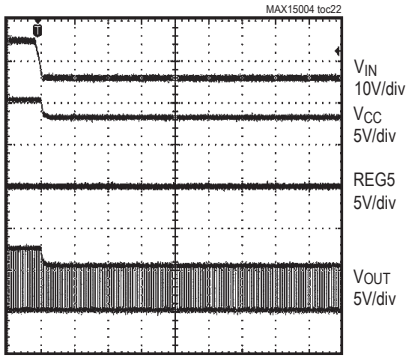
POWER-UP SEQUENCE THROUGH ON/OFF



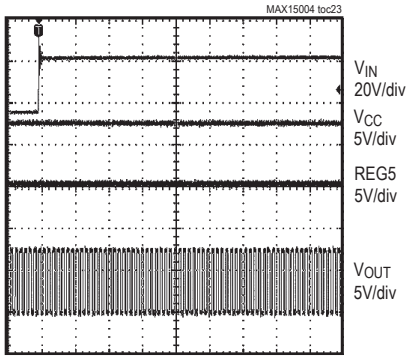
POWER-DOWN SEQUENCE THROUGH ON/OFF



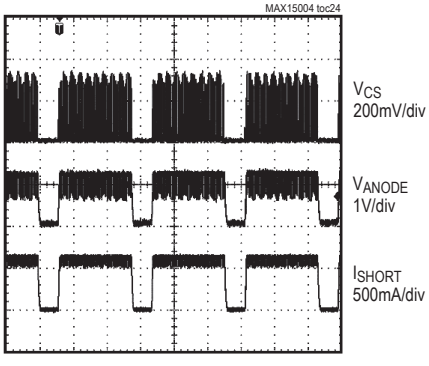
LINE TRANSIENT FOR V_{IN} STEP FROM 14V TO 5.5V



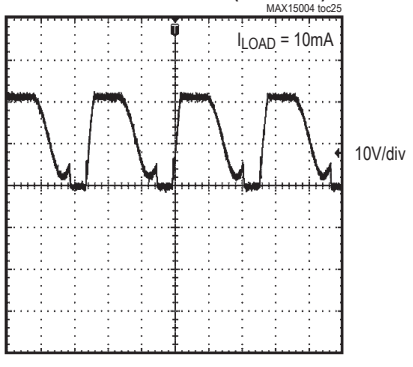
LINE TRANSIENT FOR V_{IN} STEP FROM 14V TO 40V



HICCUP MODE FOR FLYBACK CIRCUIT (FIGURE 7)



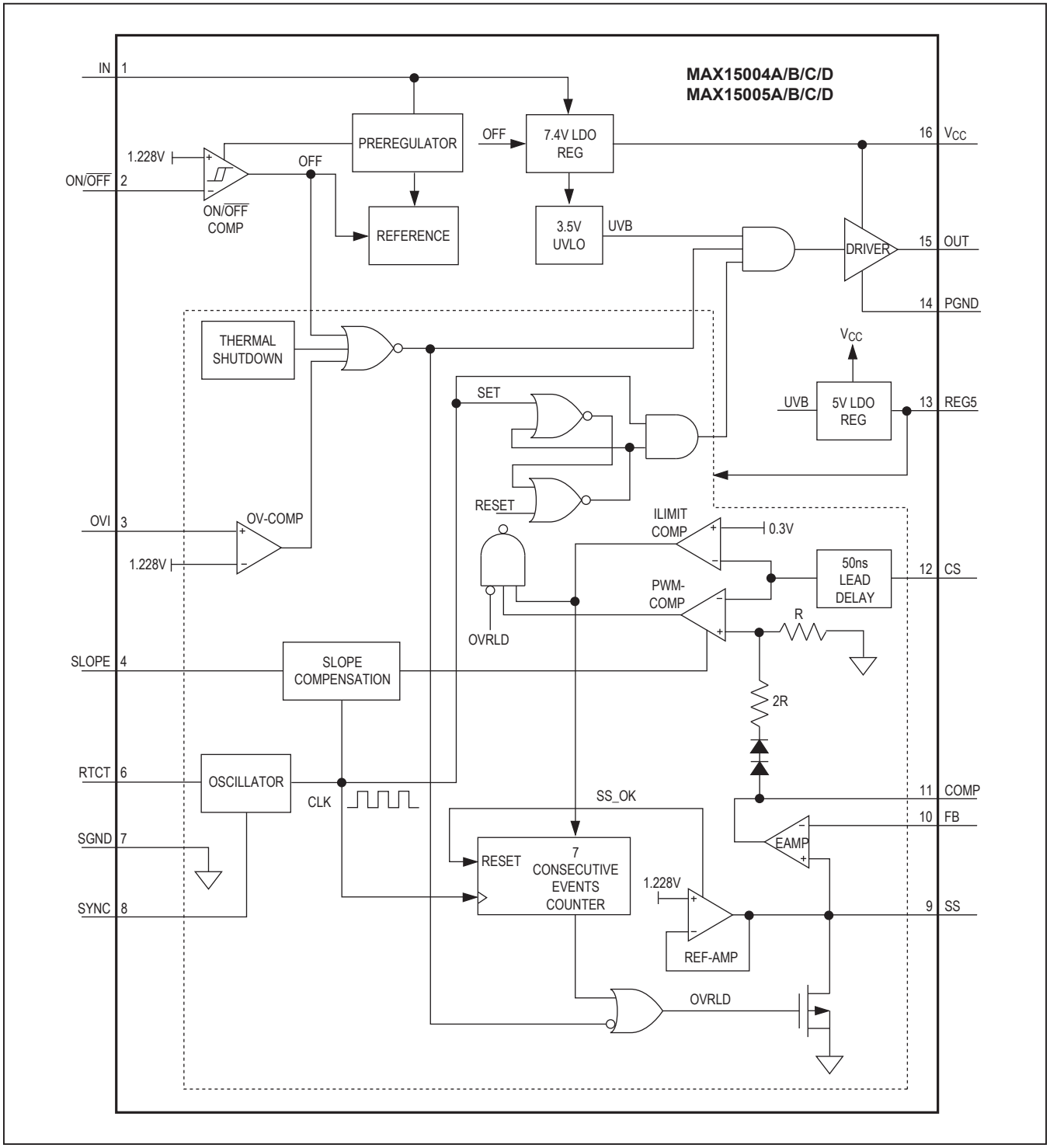
DRAIN WAVEFORM IN FLYBACK CONVERTER (FIGURE 7)



Pin Description

PIN	NAME	FUNCTION
1	IN	Input Power Supply. Bypass IN with a minimum 0.1µF ceramic capacitor to PGND.
2	ON/$\overline{OFF}$	ON/$\overline{OFF}$ Input. Connect ON/$\overline{OFF}$ to IN for always-on operation. To externally program the UVLO threshold of the IN supply, connect a resistive divider between IN, ON/$\overline{OFF}$, and SGND. Pull ON/$\overline{OFF}$ to SGND to disable the controller. To guarantee proper startup using MAX15004A/B or MAX15005A/B, ensure IN voltage is > 6V before asserting ON/OFF signal high. Use MAX15004C/D or MAX15005C/D to ensure proper startup at lower IN voltages.
3	OVI	Overvoltage Comparator Input. Connect a resistive divider between the output of the power supply, OVI, and SGND to set the output overvoltage threshold.
4	SLOPE	Programmable Slope Compensation Capacitor Input. Connect a capacitor (C_{SLOPE}) to SGND to set the amount of slope compensation. Slope compensation = $(2.5 \times 10^{-9})/C_{SLOPE}$ mV/µs with C_{SLOPE} in farads.
5	N.C.	No Connection. Not internally connected.
6	RTCT	Oscillator-Timing Network Input. Connect a resistor from RTCT to REG5 and a capacitor from RTCT to SGND to set the oscillator frequency (see the *Oscillator Frequency/External Synchronization* section).
7	SGND	Signal Ground. Connect SGND to SGND plane.
8	SYNC	External-Clock Synchronization Input. Connect SYNC to SGND when not using an external clock.
9	SS	Soft-Start Capacitor Input. Connect a capacitor from SS to SGND to set the soft-start time interval.
10	FB	Internal Error-Amplifier Inverting Input. The noninverting input is internally connected to SS.
11	COMP	Error-Amplifier Output. Connect the frequency compensation network between FB and COMP.
12	CS	Current-Sense Input. The current-sense signal is compared to a signal proportional to the error-amplifier output voltage.
13	REG5	5V Low-Dropout Regulator Output. Bypass REG5 with a 1µF ceramic capacitor to SGND.
14	PGND	Power Ground. Connect PGND to the power ground plane.
15	OUT	Gate Driver Output. Connect OUT to the gate of the external n-channel MOSFET.
16	V_{CC}	7.4V Low-Dropout Regulator Output—Driver Power Source. Bypass V_{CC} with 0.1µF and 1µF or higher ceramic capacitors to PGND. Do not connect external supply or bootstrap to V_{CC}.
—	EP	Exposed Pad (MAX15004A/C/MAX15005A/C only). Connect EP to the SGND plane to improve thermal performance. Do not use the EP as an electrical connection.

Functional Diagram



Detailed Description

The MAX15004/MAX15005 are high-performance, current-mode PWM controllers for wide input-voltage range isolated/nonisolated power supplies. These controllers are for use as general-purpose boost, flyback, and SEPIC controllers. The input voltage range of 4.5V to 40V makes it ideal in automotive applications such as vacuum fluorescent display (VFD) power supplies. The internal low-dropout regulator (V_{CC} regulator) enables the MAX15004/MAX15005 to operate directly from an automotive battery input. The input voltage can go lower than 4.5V after startup if IN is bootstrapped to a boosted output voltage.

The undervoltage lockout (ON/$\overline{OFF}$) allows the devices to program the input-supply startup voltage and ensures predictable operation during brownout conditions.

The devices contain two internal regulators, V_{CC} and REG5. The V_{CC} regulator output voltage is set at 7.4V and REG5 regulator output voltage at 5V ±2%. The input undervoltage lockout (UVLO) circuit monitors the V_{CC} voltage and turns off the converter when the V_{CC} voltage drops below 3.5V (typ).

An external resistor and capacitor network programs the switching frequency from 15kHz to 500kHz. The MAX15004/MAX15005 provide a SYNC input for synchronization to an external clock. The OUT (FET-driver output) duty cycle for the MAX15004A/B/C/D is 50%. The maximum duty cycle can be set on MAX15005A/B/C/D by selecting the right combination of RT and CT. The RTCT discharge current is trimmed to 2%, allowing accurate setting of the duty cycle for the MAX15005. An internal slope-compensation circuit stabilizes the current loop when operating at higher duty cycles and can be programmed externally.

The MAX15004/MAX15005 include an internal error amplifier with 1% accurate reference to regulate the output in nonisolated topologies using a resistive divider. The internal reference connected to the noninverting input of the error amplifier can be increased in a controlled manner to obtain soft-start. A capacitor connected at SS to ground programs soft-start to reduce inrush current and prevent output overshoot.

The MAX15004/MAX15005 include protection features like hiccup current limit, output overvoltage, and thermal shutdown. The hiccup current-limit circuit reduces the power delivered to the electronics powered by the MAX15004/MAX15005 converter during severe fault conditions. The overvoltage circuit senses the output using the path different from the feedback path to provide meaningful overvoltage protection. During continuous high input operation, the power dissipation into the MAX15004/MAX15005 could exceed its limit. Internal thermal shutdown protection safely turns off the converter when the junction heats up to 160°C.

Current-Mode Control Loop

The advantages of current-mode control overvoltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Secondly, the stability requirements of the current-mode controller are reduced to that of a single-pole system unlike the double pole in voltage-mode control.

The MAX15004/MAX15005 offer peak current-mode control operation to make the power supply easy to design with. The inherent feed-forward characteristic is useful especially in an automotive application where the input voltage changes fast during cold-crank and load dump conditions. While the current-mode architecture offers many advantages, there are some shortcomings. For higher duty-cycle and continuous conduction mode operation where the transformer does not discharge during the off duty cycle, subharmonic oscillations appear. The MAX15004/MAX15005 offer programmable slope compensation using a single capacitor. Another issue is noise due to turn-on of the primary switch that may cause the premature end of the on cycle. The current-limit and PWM comparator inputs have leading-edge blanking. All the shortcomings of the current-mode control are addressed in the MAX15004/MAX15005, making it ideal to design for automotive power conversion applications.

Internal Regulators V_{CC} and REG5

The internal LDO converts the automotive battery voltage input to a 7.4V output voltage (V_{CC}). The V_{CC} output is set at 7.4V and operates in a dropout mode at input voltages below 7.5V. The internal LDO is capable of delivering 20mA current, enough to provide power to internal control circuitry and the gate drive. The regulated V_{CC} keeps the driver output voltage well below the absolute maximum gate voltage rating of the MOSFET especially during the double battery and load dump conditions.

The second 5V LDO regulator from V_{CC} to REG5 provides power to the internal control circuits. This LDO can also be used to source 15mA of external load current.

Bypass V_{CC} and REG5 with a parallel combination of 1µF and 0.1µF low-ESR ceramic capacitors. Additional capacitors (up to 22µF) at V_{CC} can be used although they are not necessary for proper operation of the MAX15004/MAX15005.

Startup Operation/UVLO/ON/$\overline{OFF}$

The MAX15004A/B/MAX15005A/B feature two undervoltage lockouts (UVLO). The internal UVLO monitors the V_{CC}-regulator and turns on the converter once V_{CC} rises above 3.5V. The internal UVLO circuit has about 0.5V hysteresis to avoid chattering during turn-on.

An external undervoltage lockout can be achieved by controlling the voltage at the ON/$\overline{OFF}$ input. The ON/$\overline{OFF}$ input threshold is set at 1.23V (rising) with 75mV hysteresis.

Before any operation can commence, the ON/$\overline{OFF}$ voltage must exceed the 1.23V threshold.

Calculate R1 in Figure 1 by using the following formula:

$$R1 = \left(\frac{V_{ON}}{V_{UVLO}} - 1\right) \times R2$$

where V_{UVLO} is the ON/$\overline{OFF}$'s 1.23V rising threshold, and V_{ON} is the desired input startup voltage. Choose an R2 value in the 100kΩ range. The UVLO circuits keep the PWM comparator, ILIM comparator, oscillator, and output driver shut down to reduce current consumption (see the *Functional Diagram*). The ON/$\overline{OFF}$ input can be used to disable the MAX15004/MAX15005 and reduce the standby current to less than 20µA.

Soft-Start

The MAX15004/MAX15005 are provided with an externally adjustable soft-start function, saving a number of external components. The SS is a 1.228V reference bypass connection for the MAX15004A/B/C/D/MAX15005A/B/C/D and also controls the soft-start period. At startup, after V_{IN} is applied and the UVLO thresholds are reached, the device enters soft-start. During soft-start, 15µA is sourced into the capacitor (C_{SS}) connected from SS to GND causing the reference voltage to ramp up slowly. The HICCUP mode of operation is disabled during soft-start. When V_{SS} reaches 1.228V, the output as well as the HICCUP mode become fully active. Set the soft-start time (t_{SS}) using following equation:

$$t_{SS} = \frac{1.23(V) \times C_{SS}}{15 \times 10^{-6}(A)}$$

where t_{SS} is in seconds and C_{SS} is in farads.

The soft-start programmability is important to control the input inrush current issue and also to avoid the MAX15004/MAX15005 power supply from going into the unintentional hiccup during the startup. The required soft-start time depends on the topology used, current-limit setting, output capacitance, and the load condition.

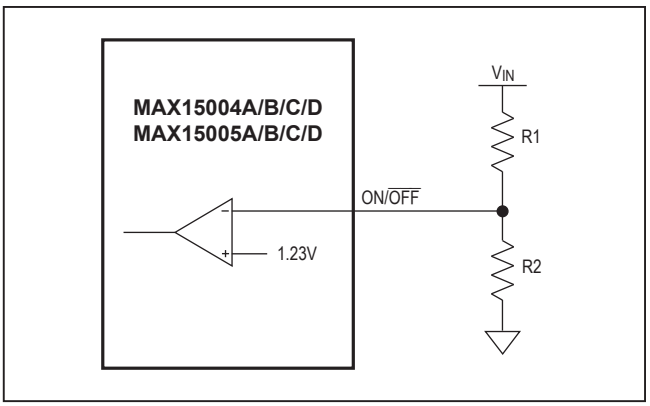


Figure 1. Setting the MAX15004A/B/MAX15005A/B Undervoltage-Lockout Threshold

Oscillator Frequency/External Synchronization

Use an external resistor and capacitor at RTCT to program the MAX15004A/B/C/D/MAX15005A/B/C/D internal oscillator frequency from 15kHz to 1MHz. The MAX15004A/B/C/D output switching frequency is one-half the programmed oscillator frequency with a 50% maximum duty-cycle limit. The MAX15005A/B/C/D output switching frequency is the same as the oscillator frequency. The RC network connected to RTCT controls both the oscillator frequency and the maximum duty cycle. The CT capacitor charges and discharges from (0.1 x V_{REG5}) to (0.55 x V_{REG5}). It charges through RT and discharges through an internal trimmed controlled current sink. The maximum duty cycle is inversely proportional to the discharge time ($t_{DISCHARGE}$). See Figure 3a and Figure 3b for a coarse selection of capacitor values for a given switching frequency and maximum duty cycle and then use the following equations to calculate the resistor value to fine-tune the switching frequency and verify the worst-case maximum duty cycle.

$$t_{CHARGE} = \frac{D_{MAX}}{f_{OSC}}$$

$$RT = \frac{t_{CHARGE}}{0.7 \times CT}$$

$$t_{DISCHARGE} = \frac{2.25(V) \times RT \times CT}{(1.33 \times 10^{-3}(A) \times RT) - 3.375(V)}$$

$$f_{OSC} = \frac{1}{t_{CHARGE} + t_{DISCHARGE}}$$

where f_{OSC} is the oscillator frequency, RT is the resistance connected from RTCT to REG5, and CT is the capacitor connected from RTCT to SGND. For the

most accuracy, CT should include all additional stray capacitance (typically 25pF to 35pF).

The MAX15004A/B/C/D is a 50% maximum duty-cycle part, while the MAX15005A/B/C/D is a 100% maximum duty-cycle part:

$$f_{OUT} = \frac{1}{2} f_{OSC}$$

for the MAX15004A/B/C/D and:

$$f_{OUT} = f_{OSC}$$

for the MAX15005A/B/C/D.

The MAX15004A/B/C/D/MAX15005A/B/C/D can be synchronized using an external clock at the SYNC input. For proper frequency synchronization, SYNC's input frequency must be at least 102% of the programmed internal oscillator frequency. Connect SYNC to SGND when not using an external clock. A rising clock edge on SYNC is interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by RC network connected to RTCT. This maintains output regulation even with intermittent SYNC signals.

n-Channel MOSFET Driver

OUT drives the gate of an external n-channel MOSFET. The driver is powered by the internal regulator (V_{CC}), internally set to approximately 7.4V. The regulated V_{CC} voltage keeps the OUT voltage below the maximum gate voltage rating of the external MOSFET. OUT can source 750mA and sink 1000mA peak current. The average current sourced by OUT depends on the switching frequency and total gate charge of the external MOSFET.

Error Amplifier

The MAX15004A/B/C/D/MAX15005A/B/C/D include an internal error amplifier. The noninverting input of the error amplifier is connected to the internal 1.228V reference and feedback is provided at the inverting input. High 100dB open-loop gain and 1.6MHz unity-gain bandwidth allow good closed-loop bandwidth and transient response.

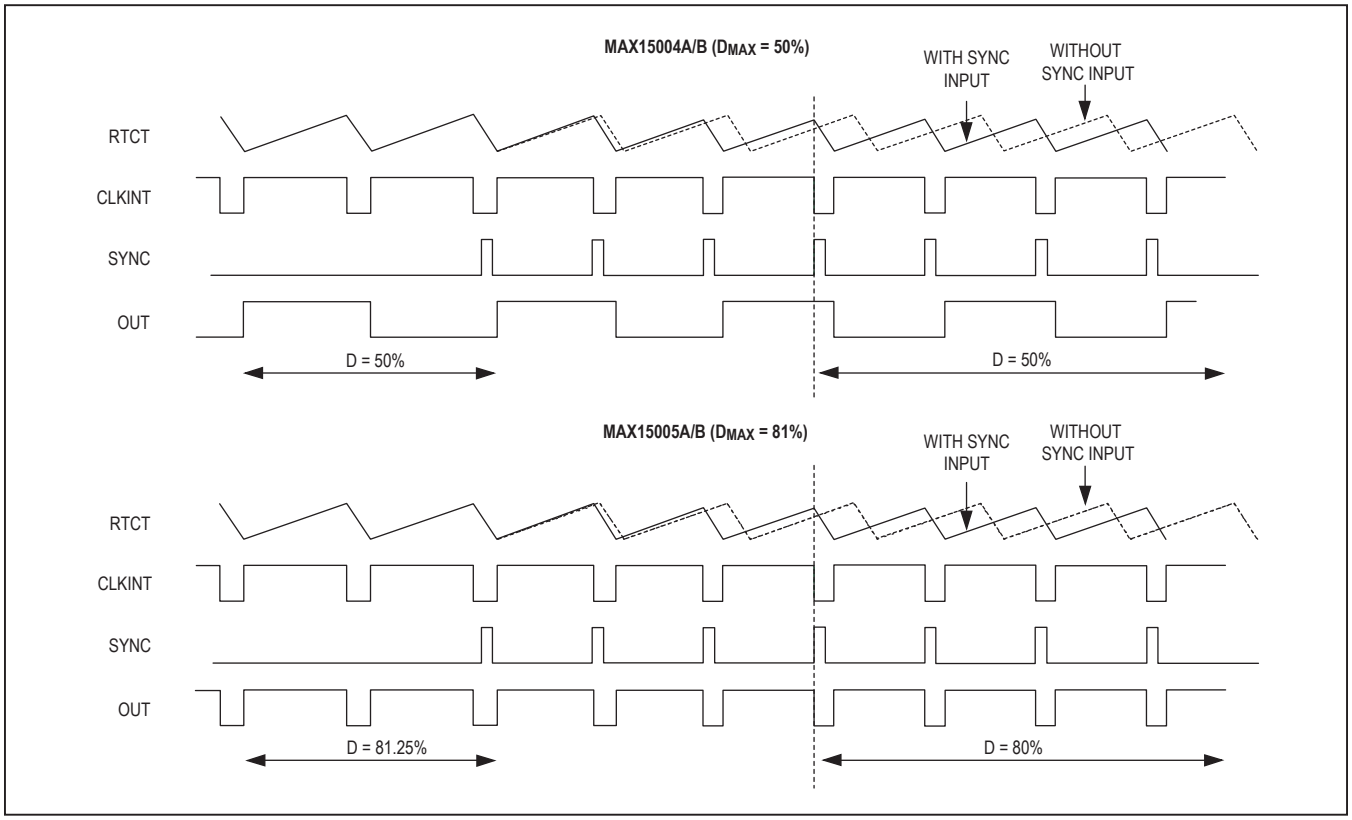


Figure 2. Timing Diagram for Internal Oscillator vs. External SYNC and D_{MAX} Behavior

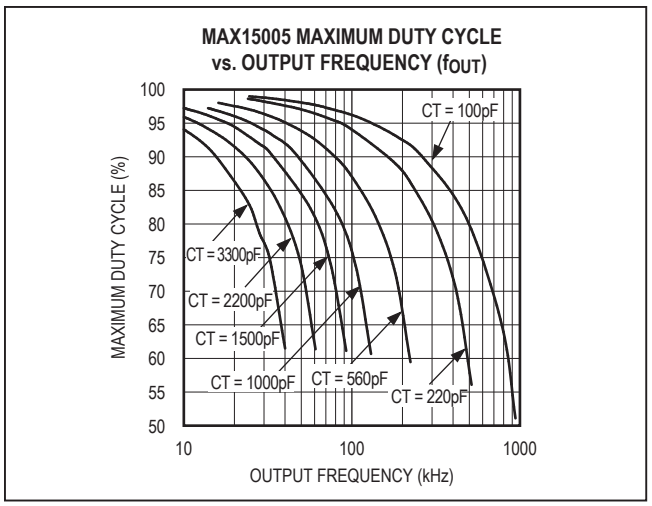


Figure 3a. MAX15005 Maximum Duty Cycle vs. Output Frequency.

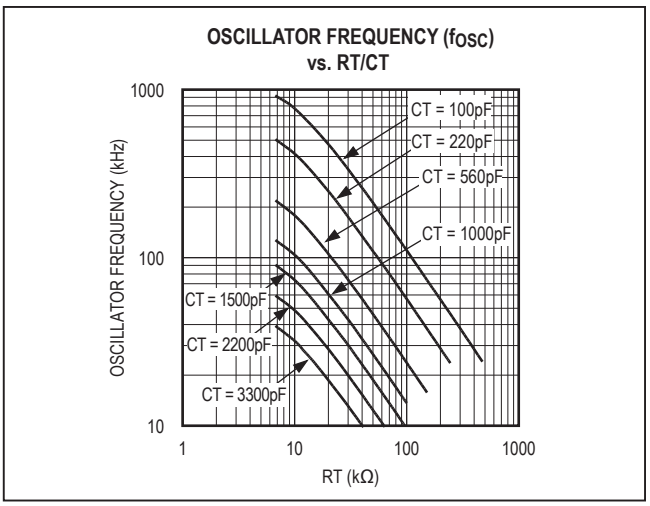


Figure 3b. Oscillator Frequency vs. RT/CT

Moreover, the source and sink current capability of 2mA provides fast error correction during the output load transient. For Figure 5, calculate the power-supply output voltage using the following equation:

$$V_{OUT} = \left(1 + \frac{R_A}{R_B}\right) V_{REF}$$

where V_{REF} = 1.228V. The amplifier's noninverting input is internally connected to a soft-start circuit that gradually increases the reference voltage during startup. This forces the output voltage to come up in an orderly and well-defined manner under all load conditions.

Slope Compensation

The MAX15004A/B/C/D/MAX15005A/B/C/D use an internal ramp generator for slope compensation. The internal ramp signal resets at the beginning of each cycle and slews at the rate programmed by the external capacitor connected to SLOPE. The amount of slope compensation needed depends on the downslope of the current waveform. Adjust the MAX15004A/B/C/D/MAX15005A/B/C/D slew rate up to 110mV/µs using the following equation:

$$\text{Slope compensation}\,(mV/\mu s) = \frac{2.5 \times 10^{-9}(A)}{C_{SLOPE}}$$

where C_{SLOPE} is the external capacitor at SLOPE in farads.

Current Limit

The current-sense resistor (R_{CS}), connected between the source of the MOSFET and ground, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 305mV. The current-sense threshold has 5% accuracy. Set the current-limit threshold 20% higher than the peak switch current at the rated output power and minimum input voltage. Use the following equation to calculate the value of R_S:

$$R_S = V_{CS}/(I_{PK} \times 1.2)$$

where I_{PRI} is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (OUT) quickly terminates the on-cycle. In most cases, a short-time constant RC filter is required to filter out the leading-edge spike on the sense waveform. The amplitude and width of the leading edge depends on the gate capacitance, drain capacitance (including interwinding capacitance), and switching speed (MOSFET turn-on time). Set the RC time constant just long enough to suppress the leading edge. For a given design, measure the leading spike at the highest input and rated output load to determine the value of the RC filter.

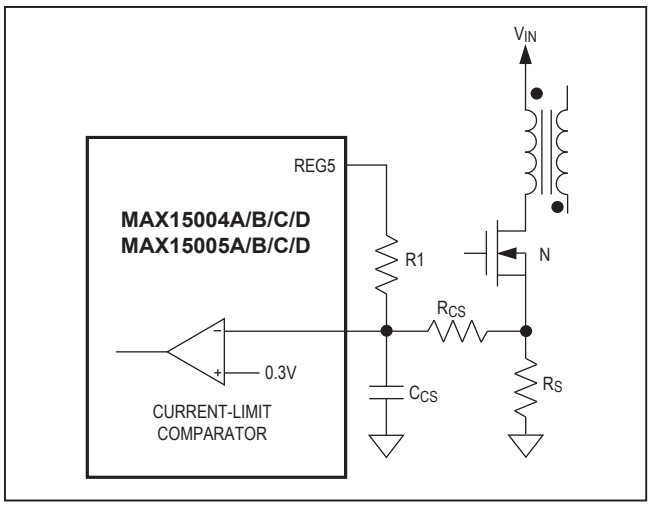


Figure 4. Reducing Current-Sense Threshold

The low 305mV current-limit threshold reduces the power dissipation in the current-sense resistor. The current-limit threshold can be further reduced by adding a DC offset to the CS input from REG5 voltage. Do not reduce the current-limit threshold below 150mV as it may cause noise issues. See Figure 4. For a new value of the current-limit threshold (V_{ILIM_LOW}), calculate the value of R1 using the following equation:

$$R1 = \frac{4.75 \times R_{CS}}{0.290 - V_{ILIM\_LOW}}$$

Applications Information

Boost Converter

The MAX15004A/B/C/D/MAX15005A/B/C/D can be configured for step-up conversion. The boost converter output can be fed back to IN through a Schottky diode (see Figure 5) so the controller can function during low voltage conditions such as cold-crank. Use a Schottky diode (D_{VIN}) in the V_{IN} path to avoid backfeeding the input source. Use the equations in the following sections to calculate inductor (L_{MIN}), input capacitor (C_{IN}), and output capacitor (C_{OUT}) when using the converter in boost operation.

Inductor Selection in Boost Configuration

Using the following equation, calculate the minimum inductor value so that the converter remains in continuous mode operation at minimum output current (I_{OMIN}):

$$L_{MIN} = \frac{V_{IN}^2 \times D \times \eta}{2 \times f_{OUT} \times V_{OUT} \times I_{OMIN}}$$

where:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - V_{DS}}$$

and

$$I_{OMIN} = (0.1 \times I_O) \text{ to } (0.25 \times I_O)$$

The higher value of I_{OMIN} reduces the required inductance; however, it increases the peak and RMS currents in the switching MOSFET and inductor. Use I_{OMIN} from 10% to 25% of the full load current. The V_D is the forward voltage drop of the external Schottky diode, D is the duty cycle, and V_{DS} is the voltage drop across the external switch. Select the inductor with low DC resistance and with a saturation current (I_{SAT}) rating higher than the peak switch current limit of the converter.

Input Capacitor Selection in Boost Configuration

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and maximum ESR using the following equations:

$$C_{IN} = \frac{\Delta I_L \times D}{4 \times f_{OUT} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where :

$$\Delta I_L = \frac{(V_{IN} - V_{DS}) \times D}{L \times f_{OUT}}$$

V_{DS} is the total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR. ΔI_L is peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor

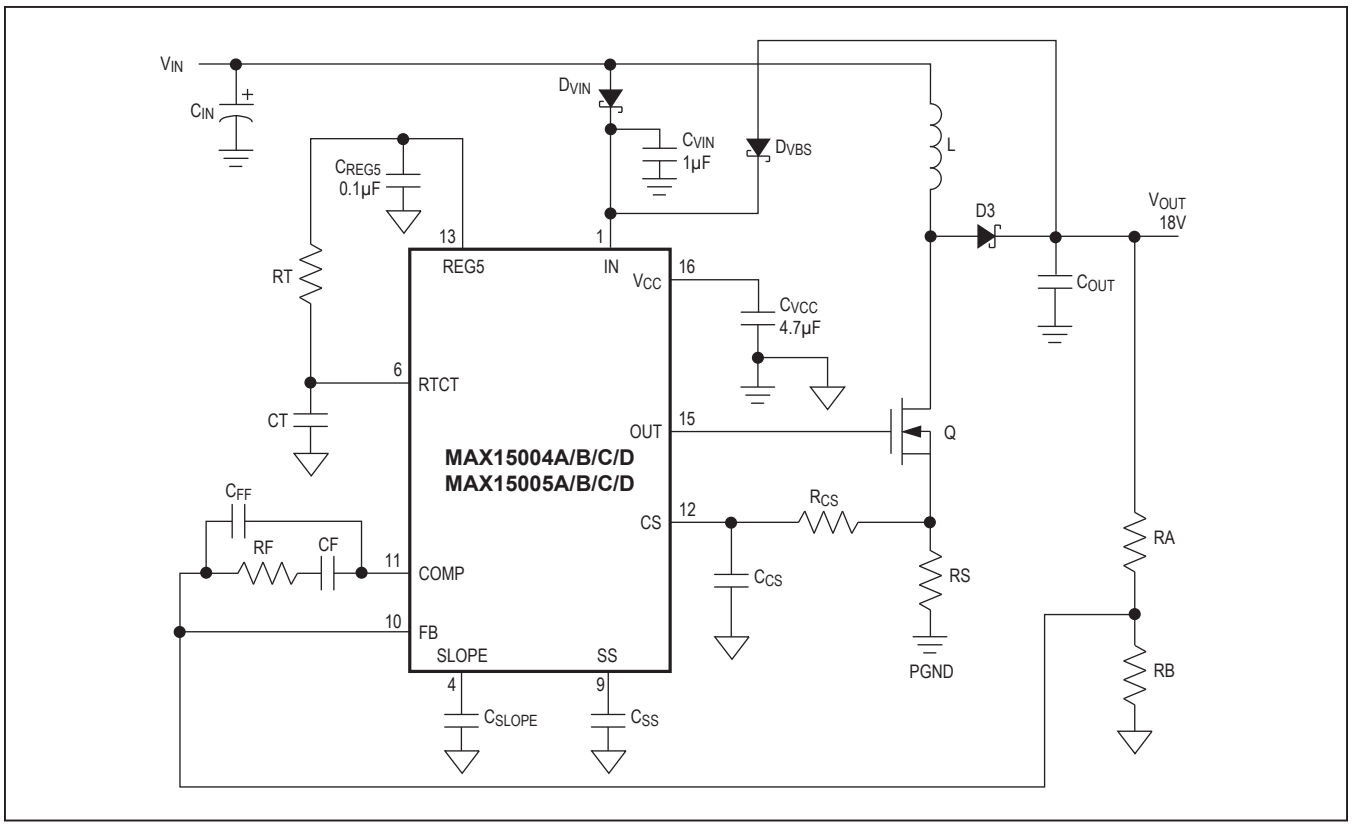


Figure 5. Application Schematic

discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) is equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source especially at high output to input differential. The MAX15004/MAX15005 are provided with a programmable soft-start; however, a large storage capacitor at the input may be necessary to avoid chattering due to finite hysteresis.

Output Capacitor Selection in Boost Configuration

For the boost converter, the output capacitor supplies the load current when the main switch is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop due to the ESR while supporting the load current. Use the following equations to calculate the output capacitor, for a specified output ripple. All ripple values are peak-to-peak.

$$ESR = \frac{\Delta V_{ESR}}{I_O}$$

$$C_{OUT} = \frac{I_O \times D_{MAX}}{\Delta V_Q \times f_{OUT}}$$

I_O is the load current, ΔV_Q is the portion of the ripple due to the capacitor discharge, and ΔV_{ESR} is the contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

Calculating Power Loss in Boost Converter

The MAX15004A/C/MAX15005A/C devices are available in a thermally enhanced package and can dissipate up to 1.7W at +70°C ambient temperature. The total power dissipation in the package must be limited so that the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature; however, Maxim recommends operating the junction at about +125°C for better reliability.

The average supply current ($I_{DRIVE-GATE}$) required by the switch driver is:

$$I_{DRIVE-GATE} = Q_g \times f_{OUT}$$

where Q_g is total gate charge at 7.4V, a number available from MOSFET data sheet.

The supply current in the MAX15004A/B/C/D/MAX15005A/B/C/D is dependent on the switching frequency. See the *Typical Operating Characteristics* to find the supply current I_{SUPPLY} of the MAX15004A/B/C/D/MAX15005A/B/C/D at a given operating frequency. The total power dissipation (P_T) in the device due to supply current (I_{SUPPLY}) and the current required to drive the switch ($I_{DRIVEGATE}$) is calculated using following equation.

$$P_T = V_{INMAX} \times (I_{SUPPLY} + I_{DRIVE-GATE})$$

MOSFET Selection in Boost Converter

The MAX15004A/B/C/D/MAX15005A/B/C/D drive a wide variety of n-channel power MOSFETs. Since V_{CC} limits the OUT output peak gate-drive voltage to no more than 11V, a 12V (max) gate voltage-rated MOSFET can be used without an additional clamp. Best performance, especially at low-input voltages ($5V_{IN}$), is achieved with low-threshold n-channel MOSFETs that specify on-resistance with a gate-source voltage (V_{GS}) of 2.5V or less. When selecting the MOSFET, key parameters can include:

1) Total gate charge (Q_g).
2) Reverse-transfer capacitance or charge (C_{RSS}).
3) On-resistance ($R_{DS(ON)}$).
4) Maximum drain-to-source voltage ($V_{DS(MAX)}$).
5) Maximum gate frequencies threshold voltage ($V_{TH(MAX)}$).

At high switching, dynamic characteristics (parameters 1 and 2 of the above list) that predict switching losses have more impact on efficiency than $R_{DS(ON)}$, which predicts DC losses. Q_g includes all capacitances associated with charging the gate. The $V_{DS(MAX)}$ of the selected MOSFET must be greater than the maximum output voltage setting plus a diode drop. The 10V additional margin is recommended for spikes at the MOSFET drain due to the inductance in the rectifier diode and output capacitor path. In addition, Q_g helps predict the current needed to drive the gate at the selected operating frequency when the internal LDO is driving the MOSFET.

Slope Compensation in Boost Configuration

The MAX15004A/B/MAX15005A/B use an internal ramp generator for slope compensation to stabilize the current loop when operating at duty cycles above 50%. It is advisable to add some slope compensation even at lower than 50% duty cycle to improve the noise immunity. The slope compensations should be optimized because too much slope compensation can turn the converter into the voltage-mode control. The amount of slope compensation required depends on the downslope of the inductor current when the main switch is off. The inductor downslope depends on the input to output voltage differential of the boost converter, inductor value, and the switching frequency. Theoretically, the compensation slope should be equal to 50% of the inductor downslope; however, a little higher than 50% slope is advised.

Use the following equation to calculate the required compensating slope (mc) for the boost converter:

$$mc = \frac{(V_{OUT} - V_{IN}) \times R_S \times 10^{-3}}{2L} (mV/\mu s)$$

The internal ramp signal resets at the beginning of each cycle and slews at the rate programmed by the external capacitor connected to SLOPE. Adjust the MAX15004A/B/C/D/MAX15005A/B/C/D slew rate up to 110mV/µs using the following equation:

$$C_{SLOPE} = \frac{2.5 \times 10^{-9}}{mc(mV/\mu s)}$$

where C_{SLOPE} is the external capacitor at SLOPE in farads.

Flyback Converter

The choice of the conversion topology is the first stage in power-supply design. The topology selection criteria include input voltage range, output voltage, peak currents in the primary and secondary circuits, efficiency, form factor, and cost.

For an output power of less than 50W and a 1:2 input voltage range with small form factor requirements, the flyback topology is the best choice. It uses a minimum of components, thereby reducing cost and form factor.

The flyback converter can be designed to operate either in continuous or discontinuous mode of operation. In discontinuous mode of operation, the transformer core completes its energy transfer during the off-cycle, while in continuous mode of operation, the next cycle begins before the energy transfer is complete. The discontinuous mode of operation is chosen for the present example for the following reasons:

- It maximizes the energy storage in the magnetic component, thereby reducing size.
- Simplifies the dynamic stability compensation design (no right-half plane zero).
- Higher unity-gain bandwidth.

A major disadvantage of discontinuous mode operation is the higher peak-to-average current ratio in the primary and secondary circuits. Higher peak-to-average current means higher RMS current, and therefore, higher loss and lower efficiency. For low-power converters, the advantages of using discontinuous mode easily surpass the possible disadvantages. Moreover, the drive capability of the MAX15004/MAX15005 is good enough to drive a large switching MOSFET. With the presently available MOSFETs, power output of up to 50W is easily achievable with a discontinuous mode flyback topology using the MAX15004/MAX15005 in automotive applications.

Transformer Design

Step-by-step transformer specification design for a discontinuous flyback example is explained below.

Follow the steps below for the discontinuous mode transformer:

Step 1) Calculate the secondary winding inductance for guaranteed core discharge within a minimum off-time.

Step 2) Calculate primary winding inductance for sufficient energy to support the maximum load.

Step 3) Calculate the secondary and bias winding turns ratios.

Step 4) Calculate the RMS current in the primary and estimate the secondary RMS current.

Step 5) Consider proper sequencing of windings and transformer construction for low leakage.

Step 1) As discussed earlier, the core must be discharged during the off-cycle for discontinuous mode operation. The secondary inductance determines the time required to discharge the core. Use the following equations to calculate the secondary inductance:

$$L_S \le \frac{(V_{OUT} + V_D) \times (D_{OFFMIN})^2}{2 \times I_{OUT} \times f_{OUT(MAX)}}$$

$$D_{OFF} = \frac{t_{OFF}}{t_{ON} + t_{OFF}}$$

where:

D_{OFFMIN} = Minimum D_{OFF}

V_D = Secondary diode forward voltage drop

I_{OUT} = Maximum output rated current

Step 2) The rising current in the primary builds the energy stored in the core during on-time, which is then released to deliver the output power during the off-time. Primary inductance is then calculated to store enough energy during the on-time to support the maximum output power.

$$L_P = \frac{V_{INMIN}^2 \times D_{MAX}^2 \times \eta}{2 \times P_{OUT} \times f_{OUT(MAX)}}$$

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

D_{MAX} = Maximum D.

Step 3) Calculate the secondary to primary turns ratio (N_{SP}) and the bias winding to primary turns ratio (N_{BP}) using the following equations:

$$N_{SP} = \frac{N_S}{N_P} = \sqrt{\frac{L_S}{L_P}}$$

and

$$N_{BP} = \frac{N_{BIAS}}{N_P} = \frac{11.7}{V_{OUT} + 0.35}$$

The forward bias drops of the secondary diode and the bias rectifier diode are assumed to be 0.35V and 0.7V, respectively. Refer to the diode manufacturer's data sheet to verify these numbers.

Step 4) The transformer manufacturer needs the RMS current maximum values in the primary, secondary, and bias windings to design the wire diameter for the different windings. Use only wires with a diameter smaller than 28AWG to keep skin effect losses under control. To

achieve the required copper cross-section, multiple wires must be used in parallel. Multifilar windings are common in high-frequency converters. Maximum RMS currents in the primary and secondary occur at 50% duty cycle (minimum input voltage) and maximum output power. Use the following equations to calculate the primary and secondary RMS currents:

$$I_{PRMS} = \frac{P_{OUT}}{0.5 \times D_{MAX} \times \eta \times V_{INMIN}} \times \sqrt{\frac{D_{MAX}}{3}}$$

$$I_{SRMS} = \frac{I_{OUT}}{0.5 \times D_{OFFMAX}} \sqrt{\frac{D_{OFFMAX}}{3}}$$

The bias current for most MAX15004/MAX15005 applications is about 20mA and the selection of wire depends more on convenience than on current capacity.

Step 5) The winding technique and the windings sequence is important to reduce the leakage inductance spike at switch turn-off. For example, interleave the secondary between two primary halves. Keep the bias winding close to the secondary, so that the bias voltage tracks the output voltage.

MOSFET Selection

MOSFET selection criteria include the maximum drain voltage, peak/RMS current in the primary and the maximum-allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage through transformer turns ratio and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case (maximum input voltage and output load) drain voltage.

$$V_{DSMAX} = V_{INMAX} + \left[\frac{N_P}{N_S} \times (V_{OUT} + V_D)\right] + V_{SPIKE}$$

Lower maximum V_{DS} requirement means a shorter channel, lower $R_{DS(ON)}$, lower gate charge, and smaller package. A lower N_P/N_S ratio allows a low V_{DSMAX} specification and keeps the leakage inductance spike under control. A resistor/diode/capacitor snubber network can be also used to suppress the leakage inductance spike.

The DC losses in the MOSFET can be calculated using the value for the primary RMS maximum current. Switching losses in the MOSFET depend on the operating frequency, total gate charge, and the transition loss during turn-off. There are no transition losses during turn-on since the primary current starts from zero in the discontinuous conduction mode. MOSFET derating may be necessary to avoid damage during system turn-on and any other fault conditions. Use the following equation to estimate the power dissipation due to the power MOSFET:

$$P_{MOS} = (1.4 \times R_{DSON} \times I^2_{PRMS}) + (Q_g \times V_{IN} \times f_{OUTMAX}) + \left(\frac{V_{INMAX} \times I_{PK} \times t_{OFF} \times f_{OUTMAX}}{4}\right) + \frac{C_{DS} \times V_{DS}{}^2 \times f_{OUTMAX}}{2}$$

where:

Q_g = Total gate charge of the MOSFET (C) at 7.4V

V_{IN} = Input voltage (V)

t_{OFF} = Turn-off time (s)

C_{DS} = Drain-to-source capacitance (F)

Output Filter Design

The output capacitance requirements for the flyback converter depend on the peak-to-peak ripple acceptable at the load. The output capacitor supports the load current during the switch on-time. During the off-cycle, the transformer secondary discharges the core replenishing the lost charge and simultaneously supplies the load current. The output ripple is the sum of the voltage drop due to charge loss during the switch on-time and the ESR of the output capacitor. The high switching frequency of the MAX15004/MAX15005 reduces the capacitance requirement.

An additional small LC filter may be necessary to suppress the remaining low-energy high-frequency spikes. The LC filter also helps attenuate the switching frequency ripple. Care must be taken to avoid any compensation problems due to the insertion of the additional LC filter. Design the LC filter with a corner frequency at more than a decade higher than the estimated closed-loop, unity-gain bandwidth to minimize its effect on the phase margin. Use 1µF to 10µF low-ESR ceramic capacitors and calculate the inductance using following equation:

$$L \le \frac{1}{4 \times 10^3 \times f_C{}^2 \times C}$$

where f_C = estimated converter closed-loop unity-gain frequency.

SEPIC Converter

The MAX15004A/B/C/D/MAX15005A/B/C/D can be configured for SEPIC conversion when the output voltage must be lower and higher than the input voltage when the input voltage varies through the operating range. The duty-cycle equation:

$$\frac{V_O}{V_{IN}} = \frac{D}{1-D}$$

indicates that the output voltage is lower than the input for a duty cycle lower than 0.5 while V_{OUT} is higher than the input at a duty cycle higher than 0.5. The inherent advantage of the SEPIC topology over the boost converter is a complete isolation of the output from the source during a fault at the output. The SEPIC converter output can be fed back to IN through a Schottky diode (see Figure 6) so the controller can function during low voltage conditions such as cold-crank. Use a Schottky diode (D_{VIN}) in the V_{IN} path to avoid backfeeding the input source.

The SEPIC converter design includes sizing of inductors, a MOSFET, series capacitance, and the rectifier diode. The inductance is determined by the allowable ripple current through all the components mentioned above. Lower ripple current means lower peak and RMS currents and lower losses. The higher inductance value needed for a lower ripple current means a larger-sized inductor, which is a more expensive solution. The inductors (L1 and L2) can be independent, however, winding them on the same core reduces the ripple currents.

Calculate the maximum duty cycle using the following equation and choose the RT and CT values accordingly for a given switching frequency (see the *Oscillator Frequency/External Synchronization* section).

$$D_{MAX} = \left[\frac{V_{OUT} + V_D}{V_{IN-MIN} + V_{OUT} + V_D - (V_{DS} + V_{CS})}\right]$$

where V_D is the forward voltage of the Schottky diode, V_{CS} (0.305V) is the current-sense threshold of the MAX15004/MAX15005, and V_{DS} is the voltage drop across the switching MOSFET during the on-time.

Inductor Selection in SEPIC Converter

Use the following equations to calculate the inductance values. Assume both L1 and L2 are equal and that the inductor ripple current (ΔI_L) is equal to 20% of the input current at nominal input voltage to calculate the inductance value.

$$L = L_1 = L2 = \left[\frac{V_{IN-MIN} \times D_{MAX}}{2 \times f_{OUT} \times \Delta I_L}\right]$$

$$\Delta I_L = \left[\frac{0.2 \times I_{OUT-MAX} \times D_{MAX}}{(1-D_{MAX}) \times \eta}\right]$$

where f_{OUT} is the converter switching frequency and η is the targeted system efficiency. Use the coupled inductors MSD-series from Coilcraft or PF0553-series from Pulse Engineering, Inc. Make sure the inductor saturating current rating (I_{SAT}) is 30% higher than the peak inductor current calculated using the following equation. Use the current-sense resistor calculated based on the I_{LPK} value from the equation below (see the *Current Limit* section).

$$I_{LPK} = \left[\frac{I_{OUT-MAX} \times D_{MAX}}{(1-D_{MAX}) \times \eta} + I_{OUT-MAX} + \Delta I_L\right]$$

MOSFET, Diode, and Series Capacitor Selection in a SEPIC Converter

For the SEPIC configuration, choose an n-channel MOSFET with a V_{DS} rating at least 20% higher than the sum of the output and input voltages. When operating at a high switching frequency, the gate charge and switching losses become significant. Use low gate-charge MOSFETs. The RMS current of the MOSFET is:

$$I_{MOS-RMS}(A) = \sqrt{\left[(I_{LPK})^2 + (I_{LDC})^2 + (I_{LPK} \times I_{LDC})\right] \times \frac{D_{MAX}}{3}}$$

where $I_{LDC} = (I_{LPK} - \Delta I_L)$.

Use Schottky diodes for higher conversion efficiency. The reverse voltage rating of the Schottky diode must be higher than the sum of the maximum input voltage (V_{IN-MAX}) and the output voltage. Since the average current flowing through the diode is equal to the output current, choose the diode with forward current rating of $I_{OUT-MAX}$. The

current sense (R_{CS}) can be calculated using the current-limit threshold (0.305V) of MAX15004/MAX15005 and I_{LPK}. Use a diode with a forward current rating more than the maximum output current limit if the SEPIC converter needs to be output short-circuit protected.

$$R_{CS} = \frac{0.305}{I_{LPK}}$$

Select R_{CS} 20% below the value calculated above. Calculate the output current limit using the following equation:

$$I_{OUT-LIM} = \left[\frac{D}{(1-D)} \times (I_{LPK} - \Delta I_L)\right]$$

where D is the duty cycle at the highest input voltage (V_{IN-MAX}).

The series capacitor should be chosen for minimum ripple voltage (ΔV_{CP}) across the capacitor. We recommend using a maximum ripple ΔV_{CP} to be 5% of the minimum input voltage (V_{IN-MIN}) when operating at the minimum input voltage. The multilayer ceramic capacitor X5R and X7R series are recommended due to their high ripple current capability and low ESR. Use the following equation to calculate the series capacitor CP value.

$$CP = \left[\frac{I_{OUT-MAX} \times D_{MAX}}{\Delta V_{CP} \times f_{OUT}}\right]$$

where ΔV_{CP} is 0.05 x V_{IN-MIN}.

For a further discussion of SEPIC converters, go to **http://pdfserv.maximintegrated.com/en/an/AN1051.pdf**.

Power Dissipation

The MAX15004/MAX15005 maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the device package, PCB copper area, other thermal mass, and airflow.

Calculate the temperature rise of the die using following equation:

$$T_J = T_C + (P_T \times \theta_{JC})$$

or:

$$T_J = T_A + (P_T \times \theta_{JA})$$

where θ_{JC} is the junction-to-case thermal impedance (3°C/W) of the 16-pin TSSOP-EP package and P_T is power dissipated in the device. Solder the exposed pad of the package to a large copper area to spread heat through the board surface, minimizing the case-to-ambient thermal impedance. Measure the temperature of the copper area near the device (T_C) at worst-case condition of power dissipation and use 3°C/W as θ_{JC} thermal impedance. The case-to-ambient thermal impedance (θ_{JA}) is dependent on how well the heat is transferred from the PCB to the ambient. Use a large copper area to keep the PCB temperature low. The θ_{JA} is 38°C/W for TSSOP-16-EP and 90°C/W for TSSOP-16 package with the condition specified by the JEDEC51 standard for a multilayer board.

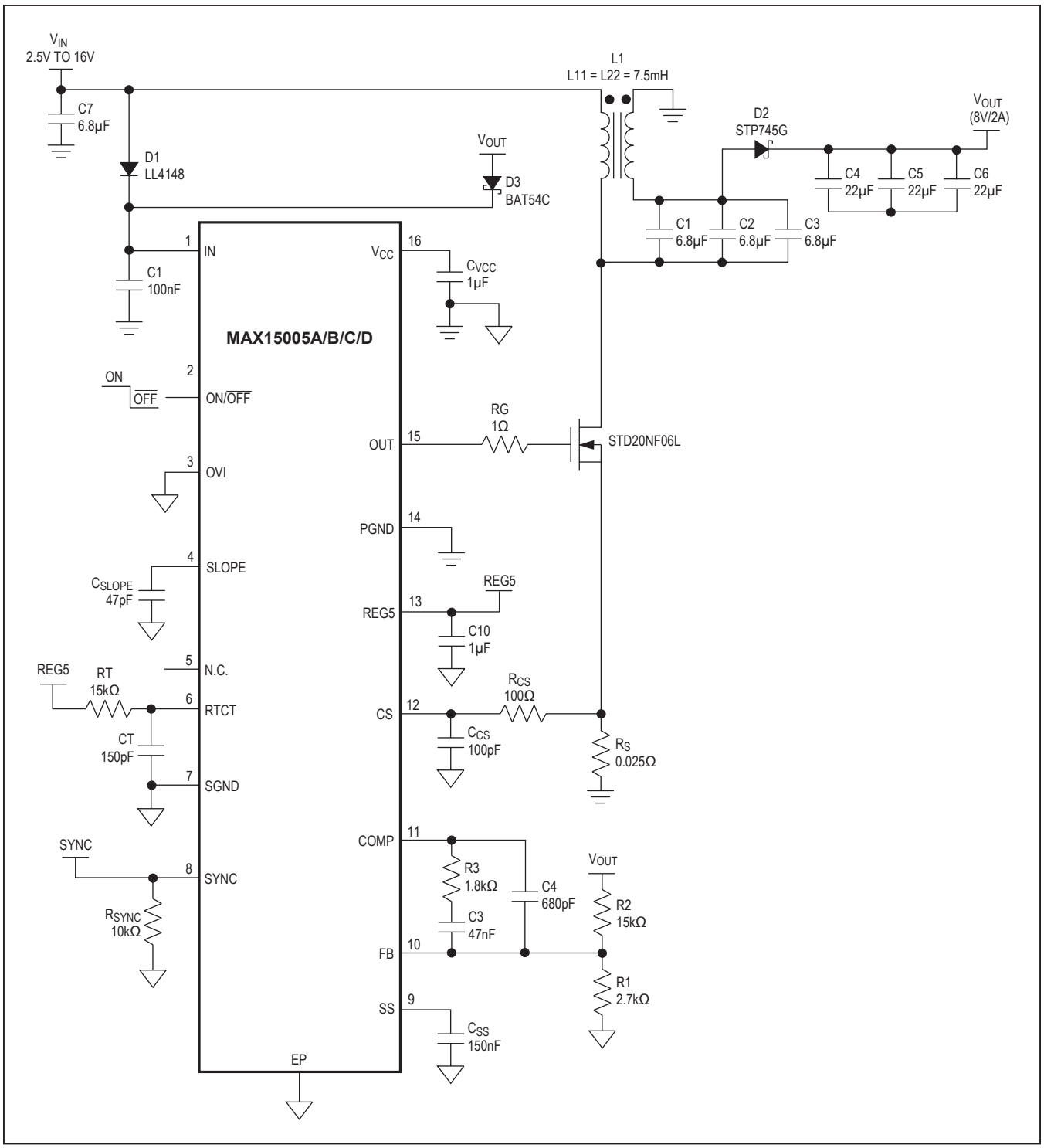


Figure 6. SEPIC Application Circuit

Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET connected to the device drain presents a dv/dt source; therefore, minimize the surface area of the heatsink as much as possible. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use a ground plane for best results.

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Refer to the MAX15005 EV kit data sheet for a specific layout example. Use a multilayer board whenever possible for better noise immunity. Follow these guidelines for good PCB layout:

1) Use a large copper plane under the package and solder it to the exposed pad. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose this copper area on the top and bottom side of the PCB.
2) Do not connect the connection from SGND (pin 7) to the EP copper plane underneath the IC. Use midlayer-1 as an SGND plane when using a multilayer board.
3) Isolate the power components and high-current path from the sensitive analog circuitry.
4) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
5) Connect SGND and PGND together close to the device at the return terminal of V_{CC} bypass capacitor. Do not connect them together anywhere else.
6) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
7) Ensure that the feedback connection to FB is short and direct.
8) Route high-speed switching nodes away from the sensitive analog areas. Use an internal PCB layer for SGND as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors.
9) Connect SYNC pin to SGND when not used.

Typical Operating Circuits

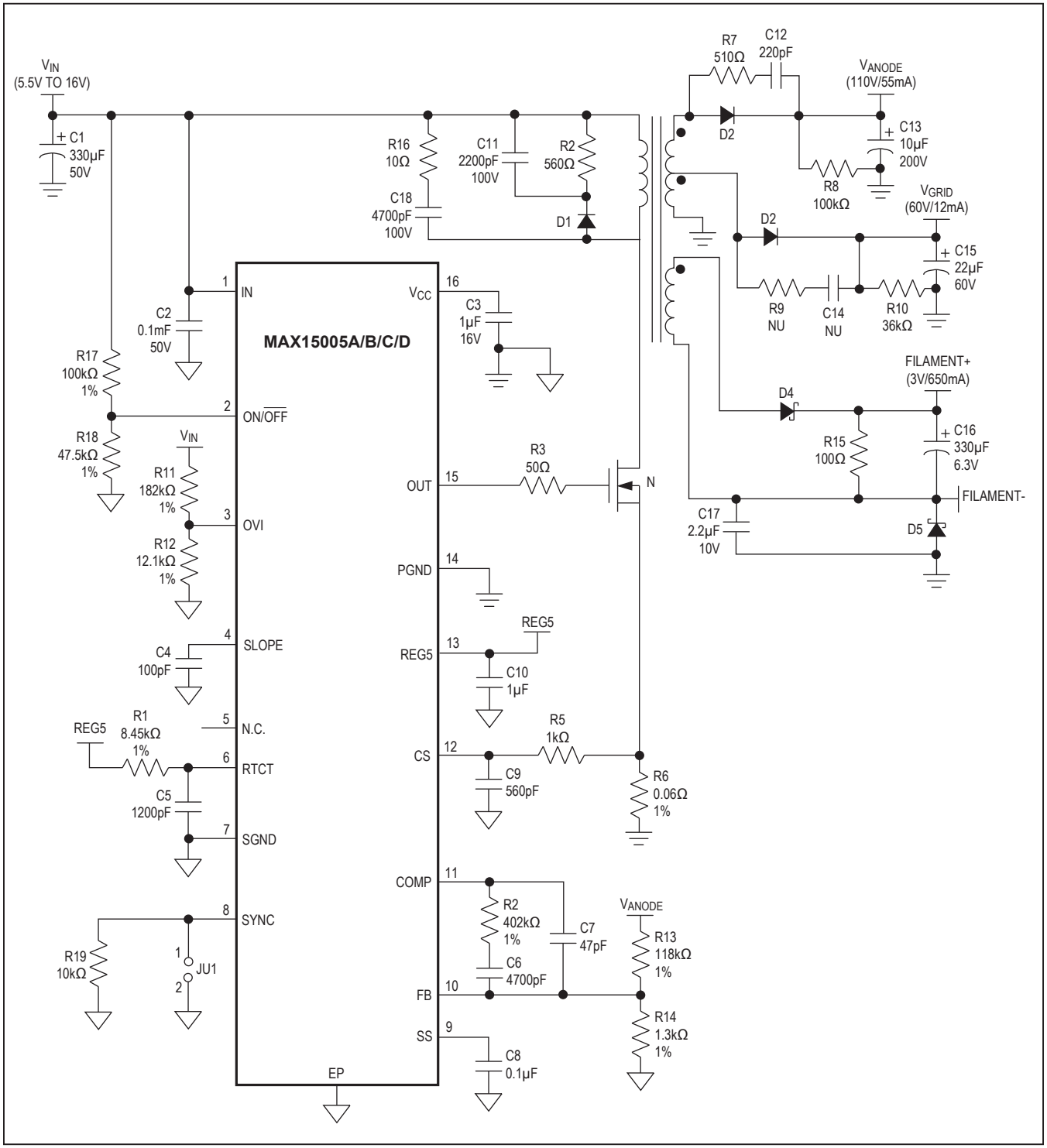


Figure 7. VFD Flyback Application Circuit

Typical Operating Circuits (continued)

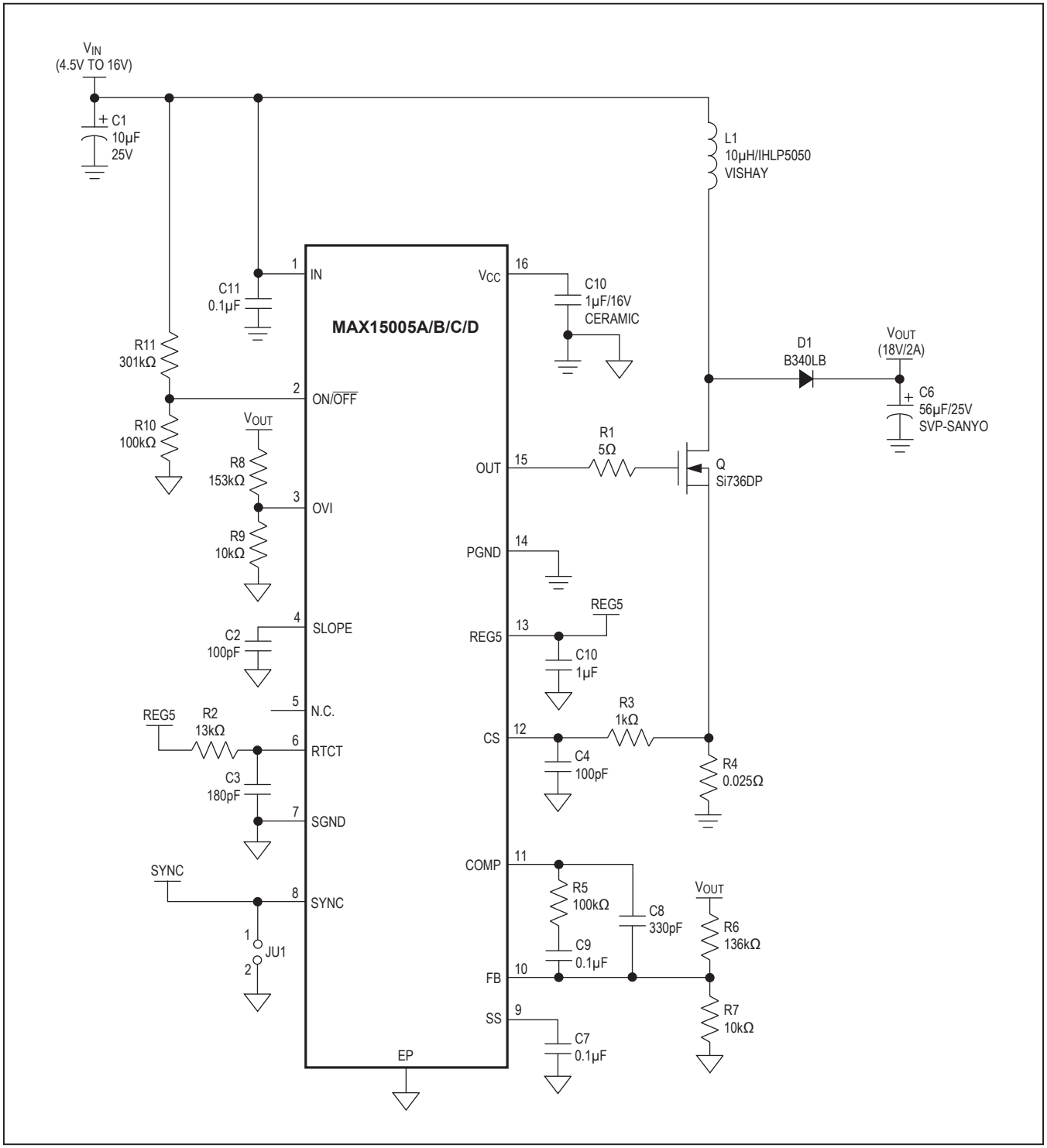
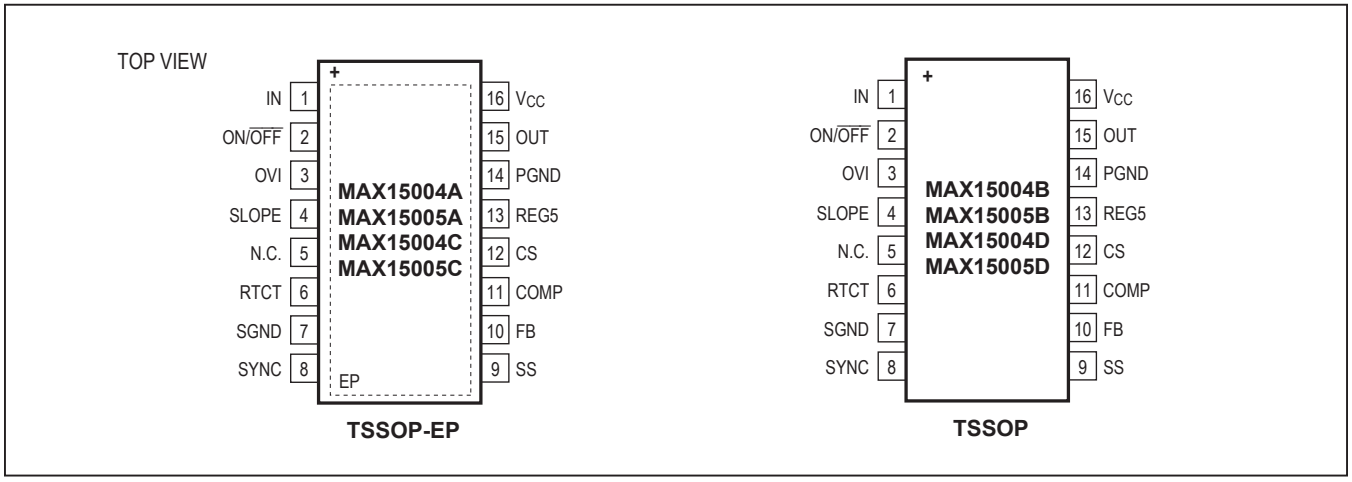


Figure 8. Boost Application Circuit

Pin Configurations



Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/07	Initial release	—
1	11/07	Updated *Features*, revised equations on pages 13, 20, and 21, revised Figure 8 with correct MOSFET, and updated package outline	1, 13, 20, 21, 25, 28
2	12/10	Added MAX15005BAUE/V+ automotive part, updated *Features*, updated *Package Information*, style edits	1–5, 9, 13, 21, 25–29
3	1/11	Added MAX15004AAUE/V+, MAX15004BAUE/V+, MAX15005AAUE/V+ automotive parts to the *Ordering Information*	1
4	1/15	Updated *Benefits and Features* section	1
5	9/15	Miscellaneous updates	1, 6, 9–11, 14–16, 18, 20–22
6	12/15	Deleted last sentence in the *Startup Operation/UVLO/ON/$\overline{OFF}$* section	12
7	2/17	Corrected f_{OSC} formula and moved section to page 12	13
8	1/20	Added part number to header on all pages, updated part number in *General Description*, *Benefits and Features*, *Ordering Information*, *Electrical Characteristics* table and *Notes*, updated *Pin Description* table, *Functional Diagram*, *Detailed Description* section, *Soft-Start* section, *Oscillator Frequency/External Synchronization* section, *Error Amplifier* section, *Slope Compensation* section,and *Boost Converter* section, updated Figure 1, Figure 4, Figure 5, *Calculating Power Loss in Boost Converter* section, *MOSFET Selection in Boost Converter* section, *Slope Compensation in Boost Configuration* section, and *SEPIC Converter* section, updated Figure 6, Figure 7, Figure 8, and Pin Configuration figures	1, 3, 5, 9–17, 20, 22, 24–26
9	2/20	Moved Package Information to page 2 and added thermal characteristics	2, 26