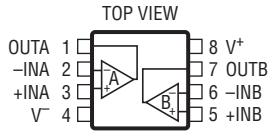
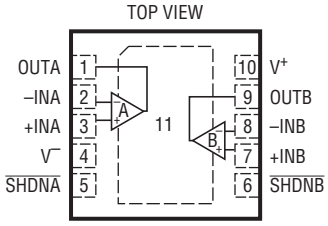
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 6V
Input Voltage ..... V^- to V^+
Input Current ..... ±10mA
$\overline{SHDNA}$/$\overline{SHDNB}$ Voltage ..... V^- to V^+
Output Short-Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range (Note 3)
LTC6084C/LTC6085C ..... –40°C to 85°C
LTC6084H/LTC6085H ..... –40°C to 125°C
Specified Temperature Range (Note 4)
LTC6084C/LTC6085C ..... 0°C to 70°C
LTC6084H/LTC6085H ..... –40°C to 125°
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MS8, GN Only ..... 300°C

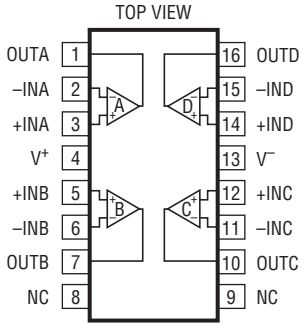
PIN CONFIGURATION



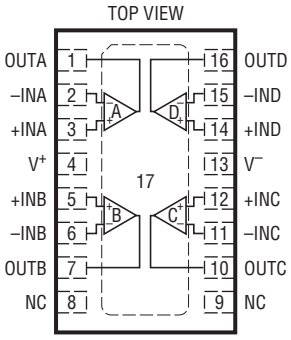
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 200°C/W



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS V^-, MUST BE SOLDERED TO PCB



GN PACKAGE
16-LEAD PLASTIC SSOP NARROW
T_{JMAX} = 150°C, θ_{JA} = 110°C/W



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6084CMS8#PBF	LTC6084CMS8#TRPBF	LTDNG	8-Lead Plastic MSOP	0°C to 70°C
LTC6084HMS8#PBF	LTC6084HMS8#TRPBF	LTDNG	8-Lead Plastic MSOP	–40°C to 125°C
LTC6084CDD#PBF	LTC6084CDD#TRPBF	LDNH	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC6084HDD#PBF	LTC6084HDD#TRPBF	LDNH	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6085CGN#PBF	LTC6085CGN#TRPBF	6085	16-Lead Plastic SSOP	0°C to 70°C
LTC6085HGN#PBF	LTC6085HGN#TRPBF	6085	16-Lead Plastic SSOP	–40°C to 125°C
LTC6085CDHC#PBF	LTC6085CDHC#TRPBF	6085	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC6085HDHC#PBF	LTC6085HDHC#TRPBF	6085	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
V_{OS}	Offset Voltage (Note 5)	LTC6084MS8, LTC6085GN			300	750		300	750	µV
		LTC6084DD, LTC6085DHC			300	1100		300	1100	µV
		LTC6084MS8, LTC6085GN	●			900			1100	µV
		LTC6084DD, LTC6085DHC	●			1350			1600	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)		●		2	5		2	5	µV/°C
I_B	Input Bias Current (Notes 5, 7)	Guaranteed by 5V Test			1			1		pA
			●			40			750	pA
I_{OS}	Input Offset Current (Notes 5, 7)	Guaranteed by 5V Test			0.5			0.5		pA
			●			30			150	pA
e_n	Input Noise Voltage Density	f = 1kHz			31			31		$nV/\sqrt{Hz}$
		f = 10kHz			27			27		$nV/\sqrt{Hz}$
	Input Noise Voltage	0.1Hz to 10Hz			3			3		μV_{P-P}
i_n	Input Noise Current Density (Note 8)				0.56			0.56		$fA/\sqrt{Hz}$
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{IN}	Input Capacitance	f = 100kHz								
	Differential Mode				5			5		pF
	Common Mode				9			9		pF
CMRR	Common Mode Rejection Ratio	$0 \le V_{CM} \le 2.5V$		64	80		64	80		dB
			●	63			61			dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 5.5V		94	115		94	115		dB
			●	91			89			dB
V_{OUT}	Output Voltage, High, (Referred to V^+)	No Load	●		0.5	5		0.5	10	mV
		I_{SOURCE} = 1mA	●		39	85		39	100	mV
		I_{SOURCE} = 5mA	●		220	460		220		mV
	Output Voltage, Low, (Referred to V^-)	No Load	●		0.5	5		0.5	10	mV
		I_{SINK} = 1mA	●		36	85		36	100	mV
		I_{SINK} = 5mA	●		200	460		200		mV
A_{VOL}	Large-Signal Voltage Gain	R_{LOAD} = 10k, $0.4V \le V_{OUT} \le 2.1V$		400	2000		400	2000		V/mV
			●	200			150			V/mV

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
I_{SC}	Output Short-Circuit Current	Source and Sink	 ●	7.7 6	12.5		7.7 4.5	12.5		mA mA
SR	Slew Rate	A_V = 1			0.5			0.5		V/µs
GBW	Gain Bandwidth Product (f_{TEST} = 10kHz)	R_{LOAD} = 50k, V_{CM} = 1.25V	 ●	0.9 0.7	1.5		0.9 0.6	1.5		MHz
Φ_0	Phase Margin	R_L = 10k, C_L = 150pF, A_V = 1			45			45		Deg
t_S	Settling Time 0.1%	V_{STEP} = 1V, A_V = 1			6			6		µs
I_S	Supply Current (Per Amplifier)	No Load	 ●		110	130 140		110	130 145	µA µA
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\overline{SHDNx}} \le 0.5V$	●		0.2	0.3		0.2	0.5	µA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.5		5.5	2.5		5.5	V
	Channel Separation	f_S = 10kHz			–120			–120		dB
	Shutdown Logic	$\overline{SHDNx}$ High $\overline{SHDNx}$ Low		1.8		 0.5	1.8		 0.5	V V
t_{ON}	Turn On Time	$V_{\overline{SHDNx}}$ = 0.5V to 1.8V			7			7		µs
t_{OFF}	Turn Off Time	$V_{\overline{SHDNx}}$ = 1.8V to 0.5V			1			1		µs
	Leakage of $\overline{SHDN}$ Pin	$V_{\overline{SHDNx}}$ = 0V	●		0.2	0.3		0.2	0.5	µA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
V_{OS}	Offset Voltage (Note 5)	LTC6084MS8, LTC6085GN LTC6084DD, LTC6085DHC LTC6084MS8, LTC6085GN LTC6084DD, LTC6085DHC	 ● ●		300 300	750 1100 900 1350		300 300	750 1100 1100 1600	µV µV µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)		●		2	5		2	5	µV/°C
I_B	Input Bias Current (Notes 5, 7)		 ●		1	 40		1	 750	pA pA
I_{OS}	Input Offset Current (Notes 5, 7)		 ●		0.5	 30		0.5	 150	pA pA
e_n	Input Noise Voltage Density	f = 1kHz f = 10kHz			31 27			31 27		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Input Noise Voltage	0.1Hz to 10Hz			3			3		μV_{P-P}
i_n	Input Noise Current Density (Note 8)				0.56			0.56		$fA/\sqrt{Hz}$
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{IN}	Input Capacitance Differential Mode Common Mode	f = 100kHz			 5 9			 5 9		 pF pF

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 5V, V^- = 0V, V_{CM} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX MIN	C SUFFIX TYP	C SUFFIX MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
CMRR	Common Mode Rejection Ratio	$0 \le V_{CM} \le 5V$	 ●	70 68	84		70 66	84		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 5.5V	 ●	94 91	115		94 89	115		dB dB
V_{OUT}	Output Voltage, High, (Referred to V^+)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 5mA	● ● ●		0.5 39 220	5 85 460		0.5 39 220	10 100	mV mV mV
	Output Voltage, Low, (Referred to V^-)	No Load I_{SINK} = 1mA I_{SINK} = 5mA	● ● ●		0.5 36 200	5 85 460		0.5 36 200	10 100	mV mV mV
A_{VOL}	Large-Signal Voltage Gain	R_{LOAD} = 10k, 0.5V ≤ V_{OUT} ≤ 4.5V	 ●	1000 400	5000		1000 300	5000		V/mV V/mV
I_{SC}	Output Short-Circuit Current	Source and Sink	 ●	7.7 6	12.5		7.7 4.5	12.5		mA mA
SR	Slew Rate	A_V = 1			0.5			0.5		V/µs
GBW	Gain Bandwidth Product (f_{TEST} = 10kHz)	R_{LOAD} = 50k, V_{CM} = 2.5V	 ●	0.9 0.7	1.5		0.9 0.6	1.5		MHz
Φ_0	Phase Margin	R_L = 10k, C_L = 150pF, A_V = 1			45			45		Deg
t_S	Settling Time 0.1%	V_{STEP} = 1V, A_V = 1			5			5		µs
I_S	Supply Current (Per Amplifier)	No Load	 ●		110	130 140		110	130 145	µA µA
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\overline{SHDNx}} \le 1.2V$	●		1.1	1.8		1.1	2	µA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.5		5.5	2.5		5.5	V
	Channel Separation	f_S = 10kHz			–120			–120		dB
	Shutdown Logic	$\overline{SHDNx}$ High $\overline{SHDNx}$ Low		3.5		 1.2	3.5		 1.2	V V
t_{ON}	Turn On Time	$V_{\overline{SHDNx}}$ = 1.2V to 3.5V			7			7		µs
t_{OFF}	Turn Off Time	$V_{\overline{SHDNx}}$ = 3.5V to 1.2V			1			1		µs
	Leakage of $\overline{SHDN}$ Pin	$V_{\overline{SHDNx}}$ = 0V	●		0.5	0.9		0.5	1.2	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and the total output current.

Note 3: The LTC6084C/LTC6085C are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6084H/LTC6085H are guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 4: The LTC6084C/LTC6085C are guaranteed to meet specified performance from 0°C to 70°C. The LTC6084C/LTC6085C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LTC6084H/LTC6085H are guaranteed to meet specified performance from –40°C to 125°C.

Note 5: ESD (Electrostatic Discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6084/LTC6085; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 6: This parameter is not 100% tested.

Note 7: This specification is limited by high speed automated test capability. See Typical Performance Characteristic curves for actual performance.

Note 8: Current noise is calculated from $i_n = \sqrt{2qI_B}$, where $q = 1.6 \cdot 10^{-19}$ coulombs.

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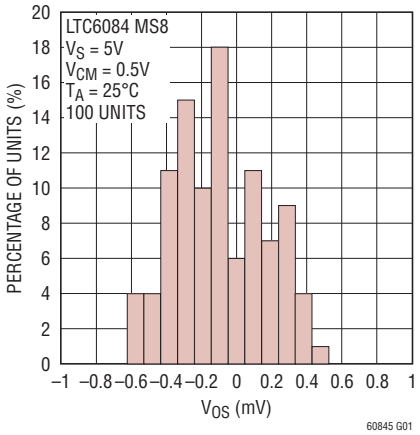
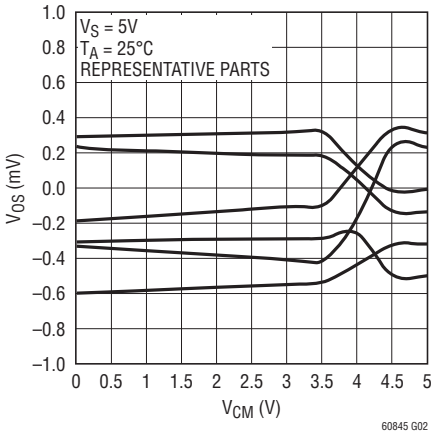
TYPICAL PERFORMANCE CHARACTERISTICS

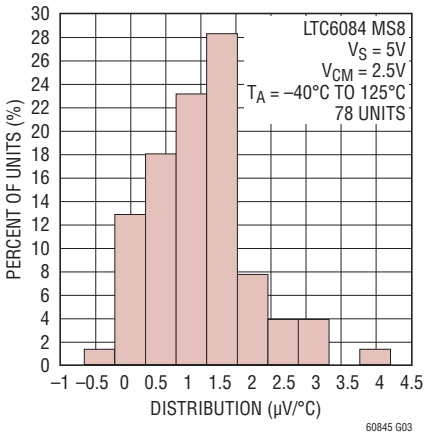
V_{OS} Distribution



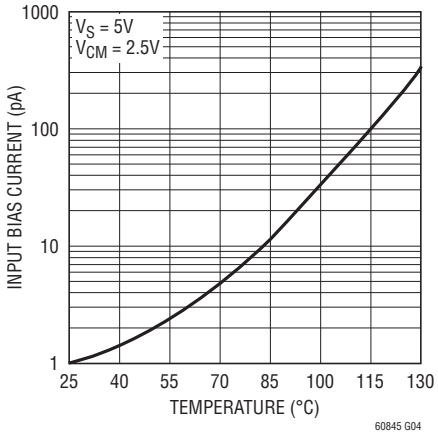
V_{OS} vs V_{CM}



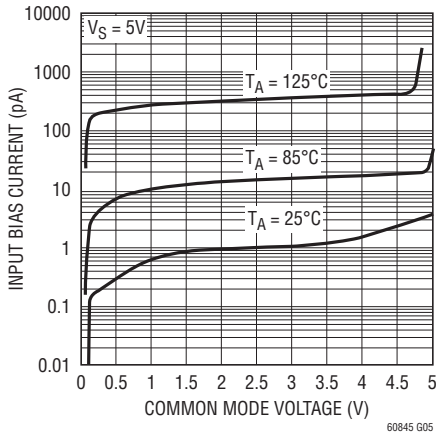
V_{OS} Drift Distribution



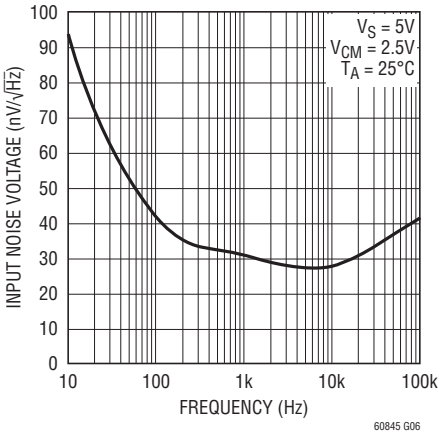
Input Bias vs Temperature



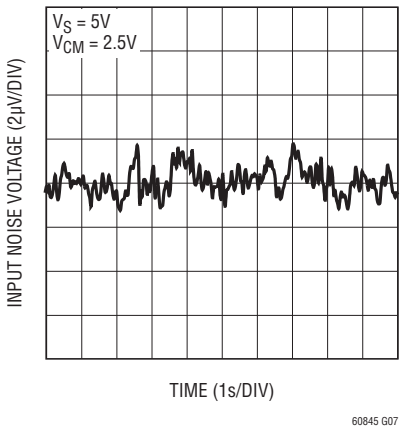
Input Bias Current vs Common Mode Voltage



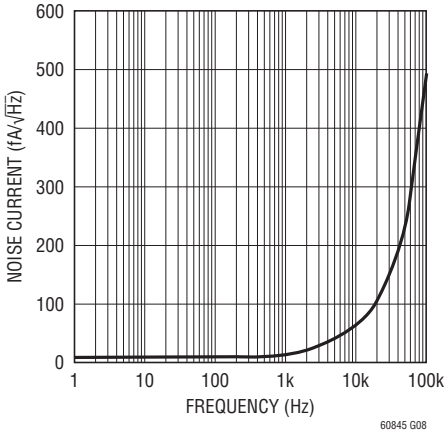
Input Noise Voltage vs Frequency



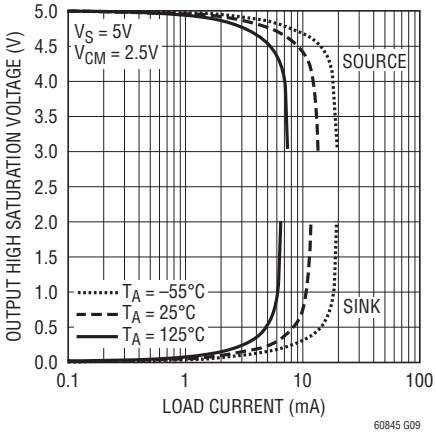
0.1Hz to 10Hz Output Voltage Noise



Input Noise Current vs Frequency



Output Saturation Voltage vs Load Current (Output High)



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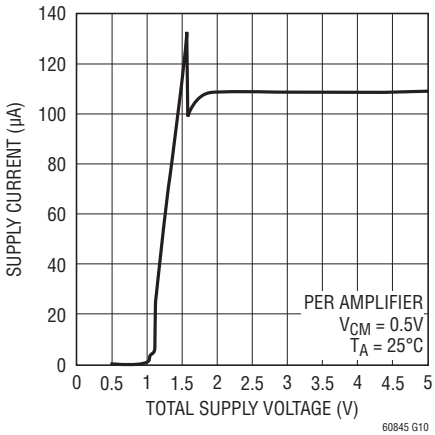
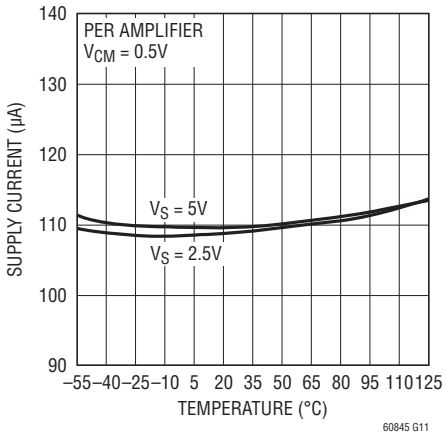
TYPICAL PERFORMANCE CHARACTERISTICS

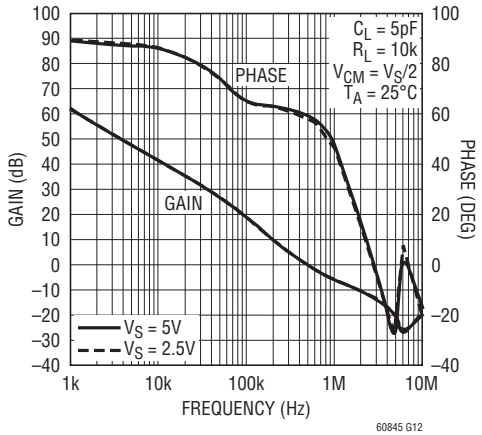
Supply Current vs Supply Voltage



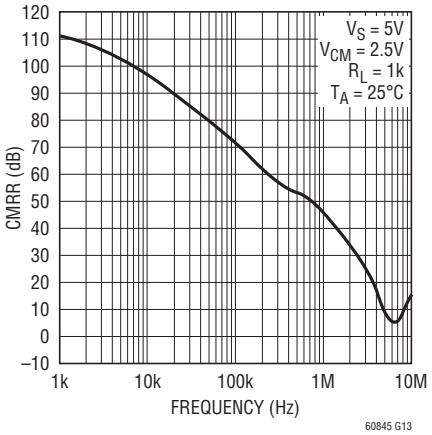
Supply Current vs Temperature



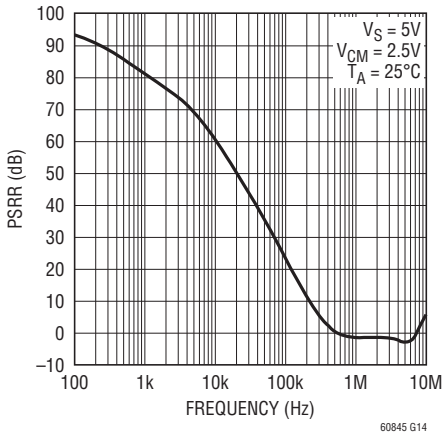
Open-Loop Gain vs Frequency



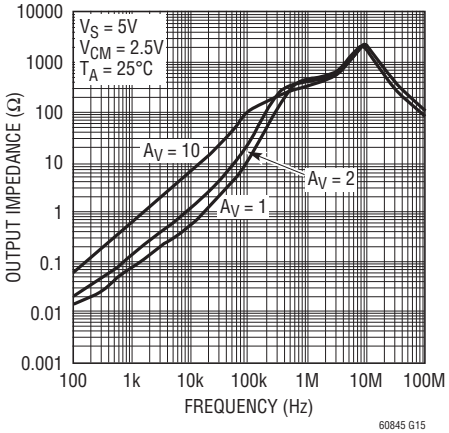
CMRR vs Frequency



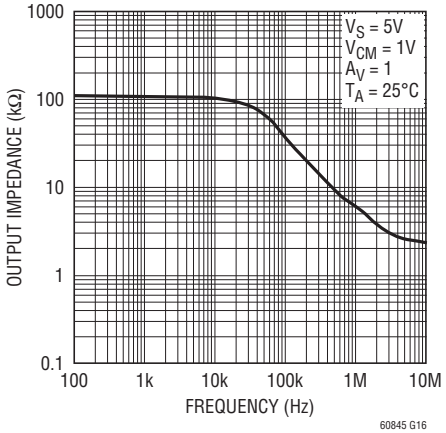
PSRR vs Frequency



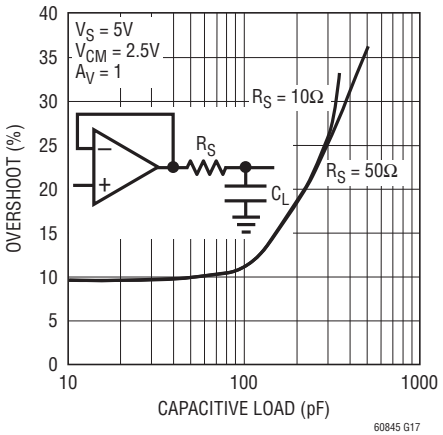
Output Impedance vs Frequency



Disabled Output Impedance vs Frequency



Capacitive Load Handling



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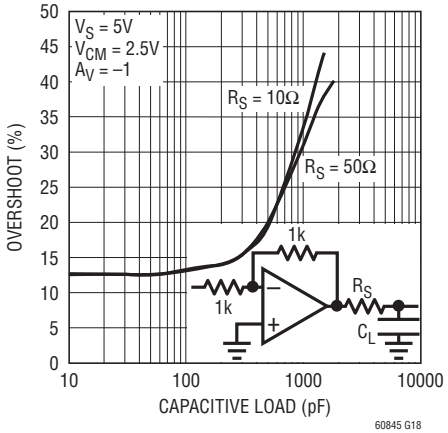
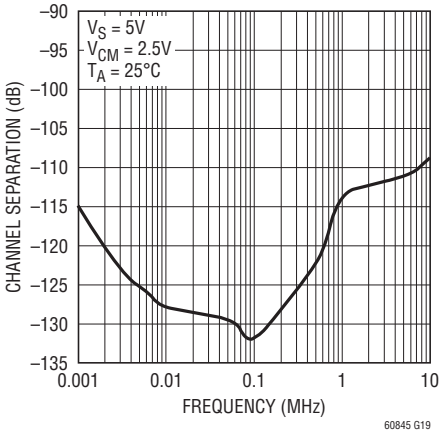
TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling



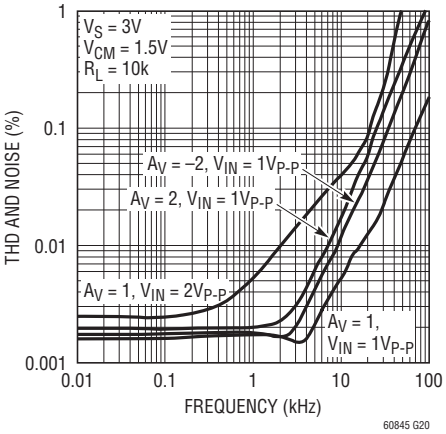
60845 G18

Channel Separation vs Frequency



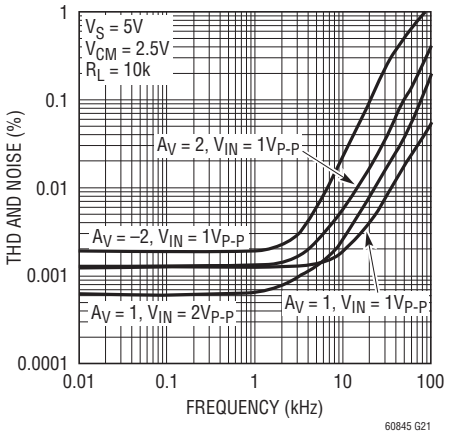
60845 G19

Total Harmonic Distortion and Noise vs Frequency



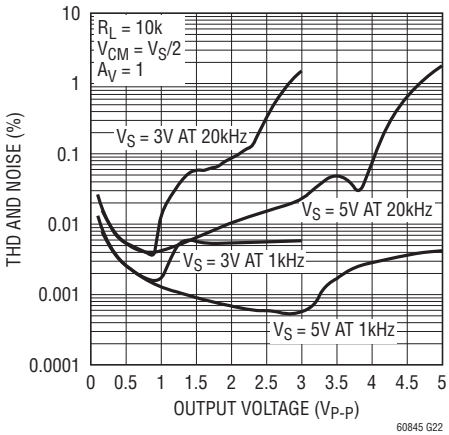
60845 G20

Total Harmonic Distortion and Noise vs Frequency



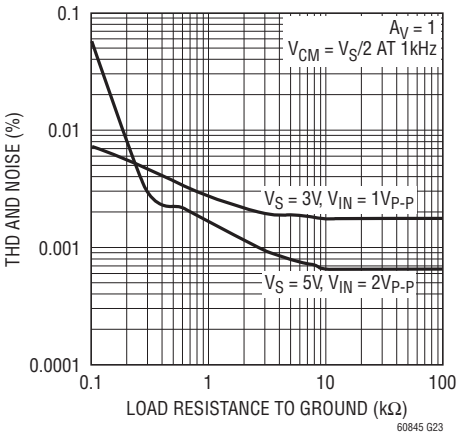
60845 G21

Total Harmonic Distortion and Noise vs Output Voltage



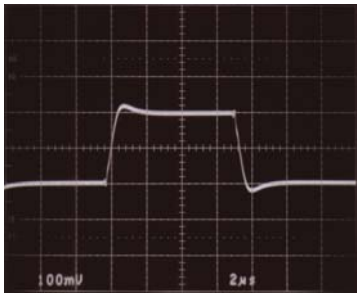
60845 G22

Total Harmonic Distortion and Noise vs Load Resistance



60845 G23

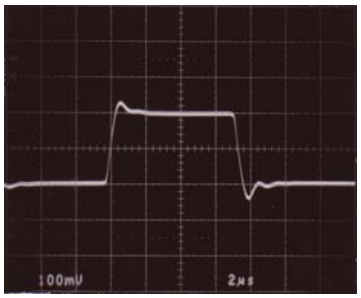
Small Signal Response



V_S = 5V
A_V = 1
R_L = ∞

60845 G24

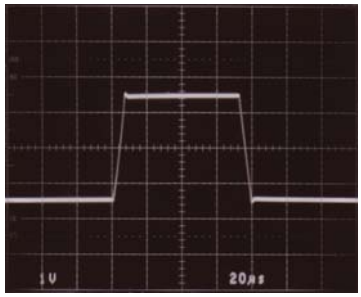
Small Signal Response



V_S = 5V
A_V = 1
R_L = ∞
C_L = 220pF

60845 G25

Large Signal Response



V_S = 5V
A_V = 1
R_L = ∞

60845 G26

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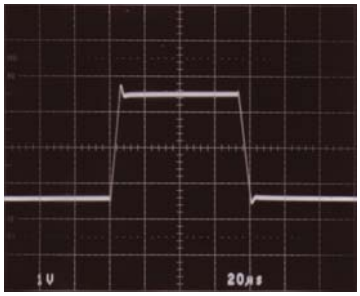
TYPICAL PERFORMANCE CHARACTERISTICS

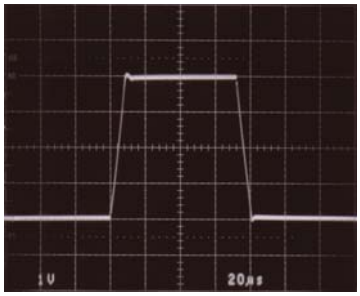
Large Signal Response



V_S = 5V
A_V = –1
R_L = 1k

60845 G27

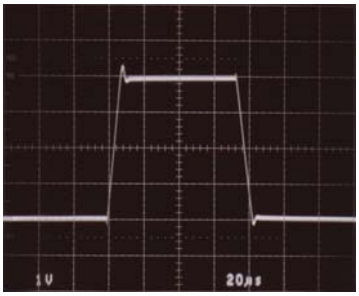
Large Signal Response



V_S = 5V
A_V = 1
R_L = ∞

60845 G28

Large Signal Response



V_S = 5V
A_V = –1
R_L = 1k

60845 G29

PIN FUNCTIONS

OUT: Amplifier Output.

–IN: Inverting Input.

+IN: Noninverting Input.

V^+: Positive Supply.

V^-: Negative Supply.

$\overline{SHDNA}$: Shutdown Pin of Amplifier A, active low and only available with the LTC6084DD. An internal current source pulls the pin to V^+ when floating.

$\overline{SHDNB}$: Shutdown Pin of Amplifier B, active low and only available with the LTC6084DD. An internal current source pulls the pin to V^+ when floating.

NC: Not Internally Connected.

Exposed Pad: Connected to V^-.

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APPLICATIONS INFORMATION

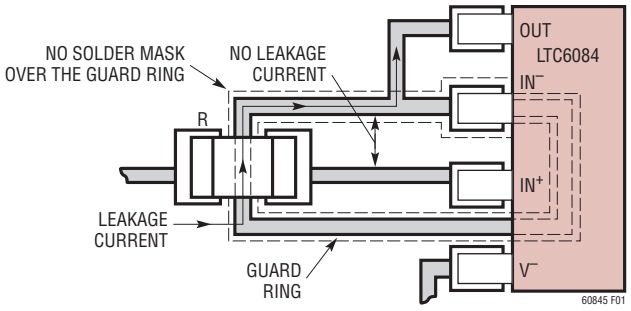

Figure 1. Sample Layout. Unity-Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage

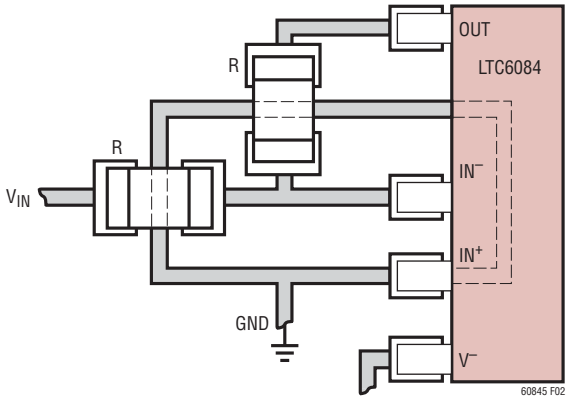

Figure 2. Sample Layout. Inverting Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage

Rail-to-Rail Input

The input stage of LTC6084/LTC6085 combines both PMOS and NMOS differential pairs, extending its input common mode voltage to both positive and negative supply voltages. At high input common mode range, NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between 1.3 and 0.9V below the positive supply.

Achieving Low Input Bias Current

The DD and DHC packages are leadless and make contact to the PCB beneath the package. Solder flux used during the attachment of the part to the PCB can create leakage current paths and can degrade the input bias current performance of the part. All inputs are susceptible because the backside paddle is connected to V^- internally. As the input voltage or V^- changes, a leakage path can be formed and alter the observed input bias current. For lowest bias current use the LTC6084/LTC6085 in the leaded MSOP/GN package. With fine PCB design rules, you can also provide a guard ring around the inputs.

For example, in high source impedance applications such as pH probes, photo diodes, strain gauges, etc., the low input bias current of these parts requires a clean board layout to minimize additional leakage current into a high impedance signal node. A mere 100GΩ of PC board resistance between a 5V supply trace and input trace near ground potential adds 50pA of leakage current. This leakage is far greater than the bias current of the operational amplifier. A guard ring around the high impedance input traces driven by a low impedance source equal to the input voltage prevents such leakage problems. The guard ring should extend as far as necessary to shield the high impedance signal from any and all leakage paths. Figure 1 shows the use of a guard ring in a unity-gain configuration. In this case the guard ring is connected to the output and is shielding the high impedance noninverting input from V^-. Figure 2 shows the inverting gain configuration.

Rail-to-Rail Output

The output stage of the LTC6084/LTC6085 swings within 5mV of the supply rails when driving high impedance loads, in other words when no DC load current is present. See the Typical Performance Characteristics for curves of output swing versus load current. The class AB design of the output stage enables the op amp to supply load currents which are much greater than the quiescent supply current. For example, the room temperature short-circuit current is typically 12.5mA.

Capacitive Load

LTC6084/LTC6085 can drive a capacitive load up to 300pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load further increases the amount of capacitance the amplifier can drive.

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APPLICATIONS INFORMATION

$\overline{SHDN}$ Pins

Pins 5 and 6 are used for power shutdown of the LTC6084 in the DD package. If they are floating, internal current sources pull pins 5 and 6 to V^+ and the amplifiers operate normally. In shutdown the amplifier output is high impedance, and each amplifier draws less than 1µA current. This feature allows the part to be used in muxed output applications as shown in Figure 3.

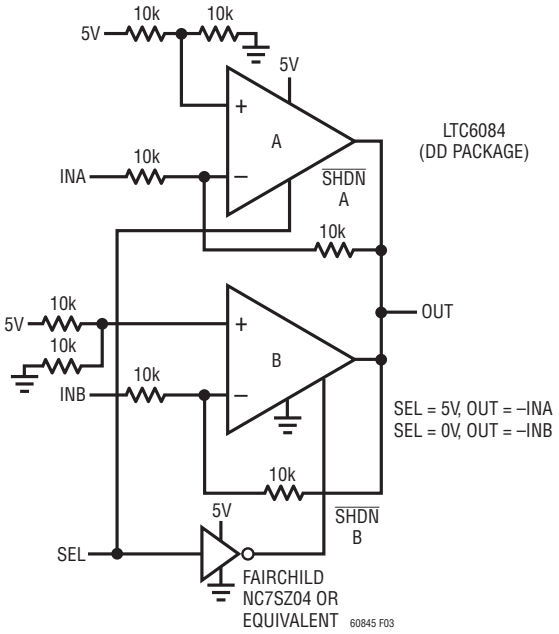

Figure 3. Inverting Amplifier with Muxed Output

ESD

The LTC6084/LTC6085 has reverse-biased ESD protection diodes on all inputs and outputs as shown in the Simplified Schematic. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to 100mA or less, no damage to the device will occur.

The amplifier input bias current is the leakage current of these ESD diodes. This leakage is a function of the temperature and common mode voltage of the amplifier, as shown in the Typical Performance Characteristics.

Noise

In the frequency region above 1kHz, the LTC6084/LTC6085 shows good noise voltage performance. In this region, noise can be dominated by the total source resistance of the particular application. Specifically, these amplifiers exhibit the noise of a 58k resistor, meaning it is desirable to keep the source and feedback resistance at or below this value, i.e., $R_S + R_G||R_{FB} \leq 58k$. Above this total source impedance, the noise voltage is dominated by the resistors.

At low frequency, noise current can be estimated from the expression $i_n = \sqrt{2qI_B}$, where $q = 1.6 \bullet 10^{-19}$ coulombs. Equating $\sqrt{4kTR\Delta f}$ and $R\sqrt{2qI_B\Delta f}$ shows that for a source resistor below 50GΩ the amplifier noise is dominated by the source resistance. Noise current rises with frequency. See the curve Input Noise Current vs Frequency in the Typical Performance Characteristics section.

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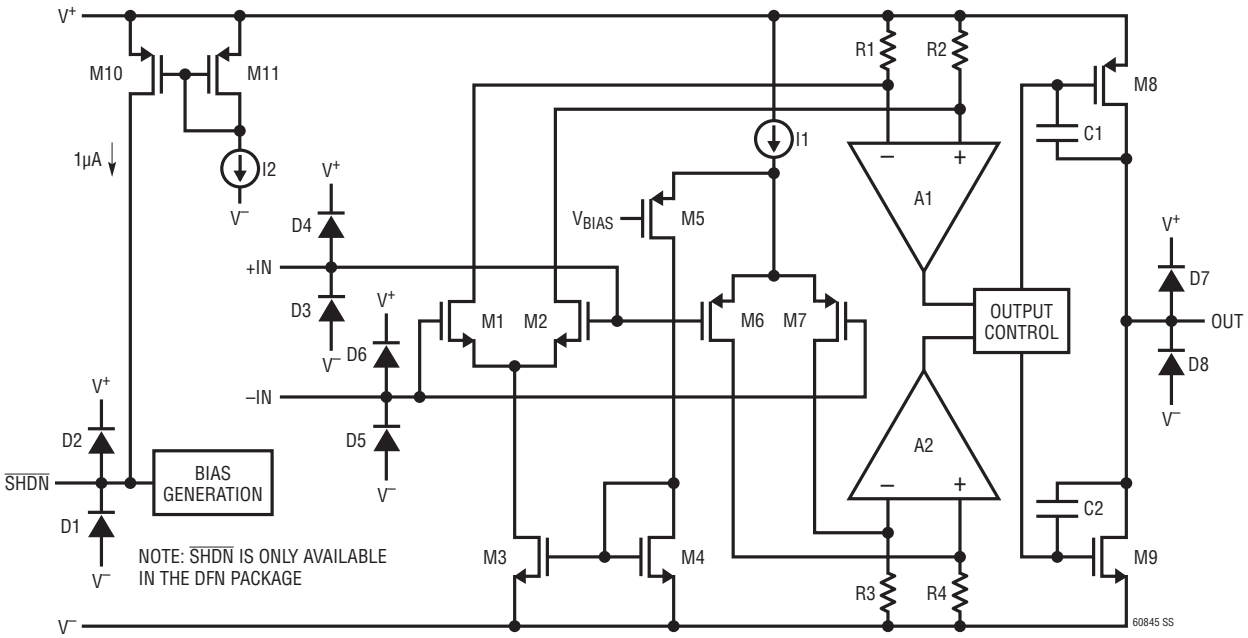
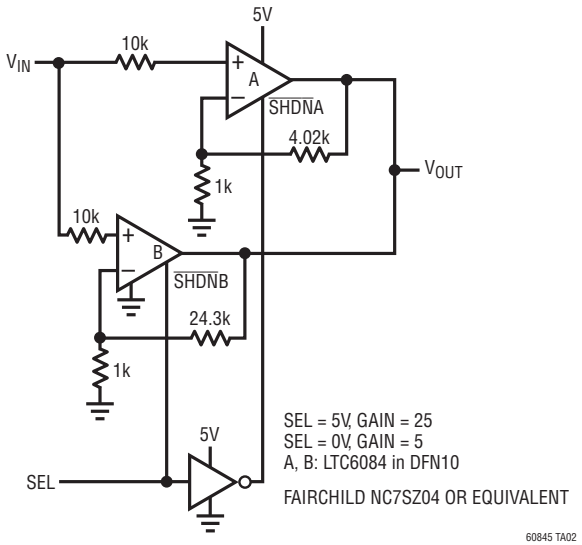
SIMPLIFIED SCHEMATIC

Simplified Schematic of the Amplifier



TYPICAL APPLICATIONS

Gain Selectable Amplifier



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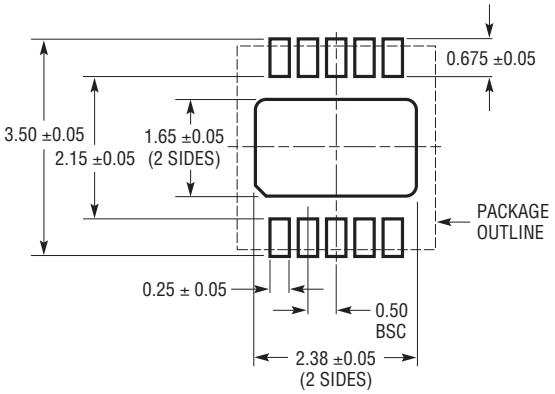
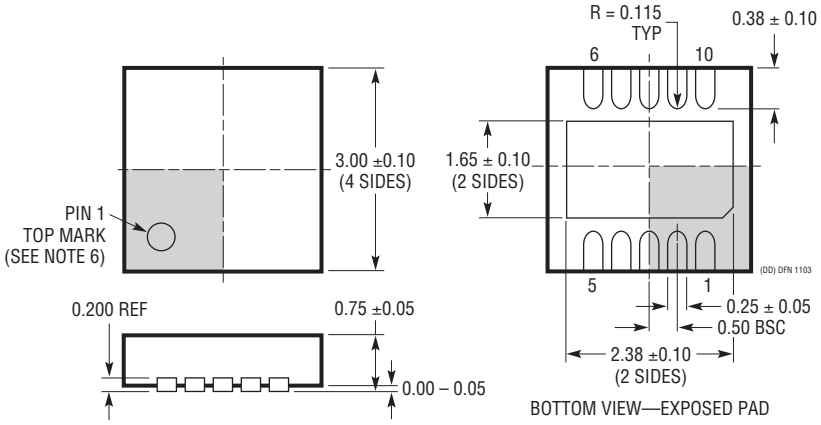
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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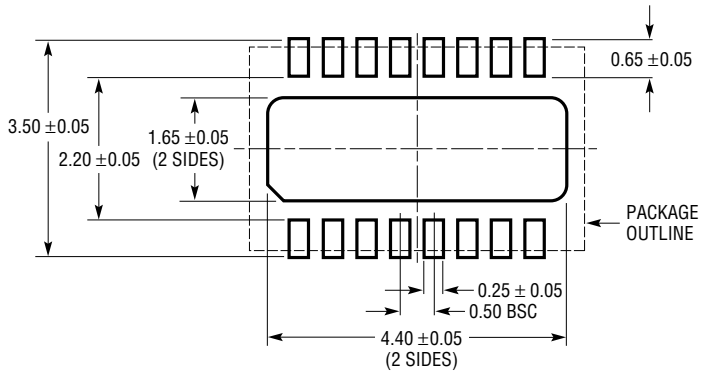
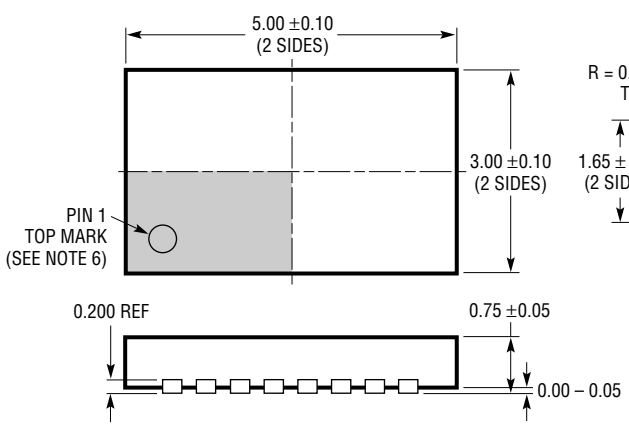
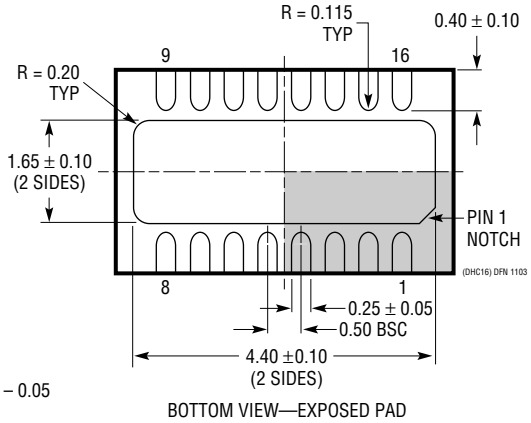
PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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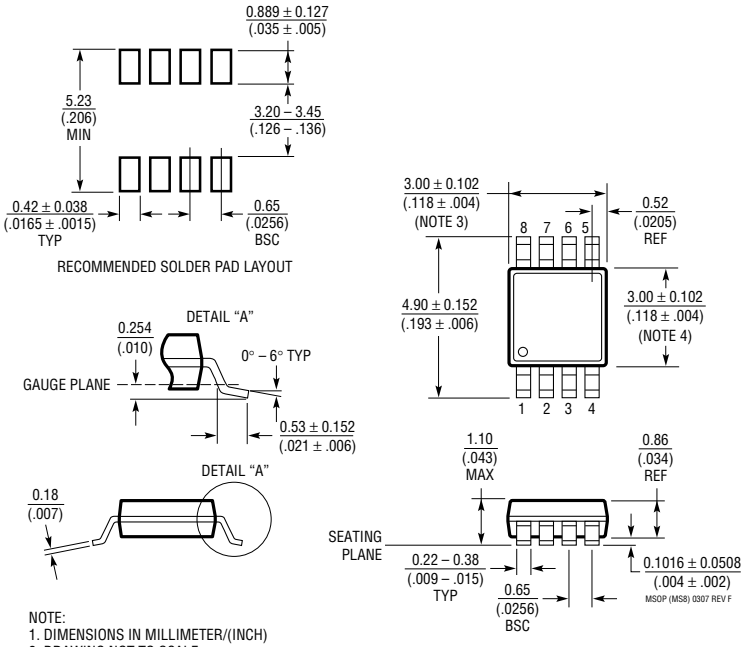
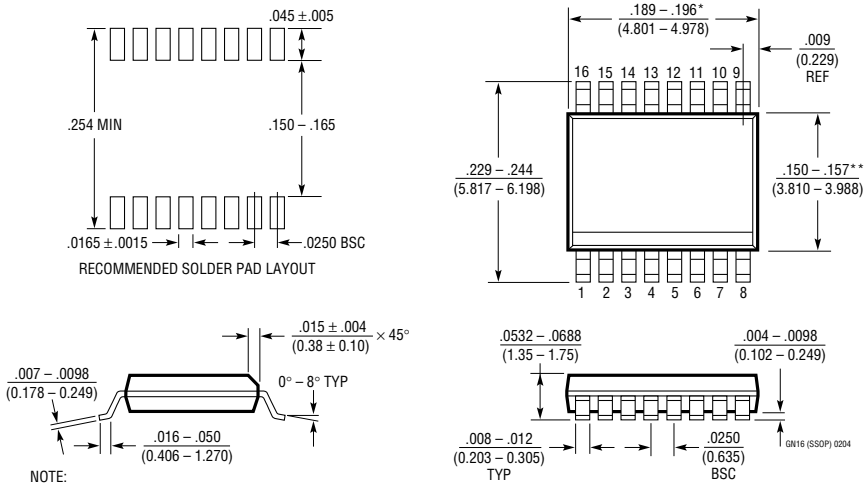
PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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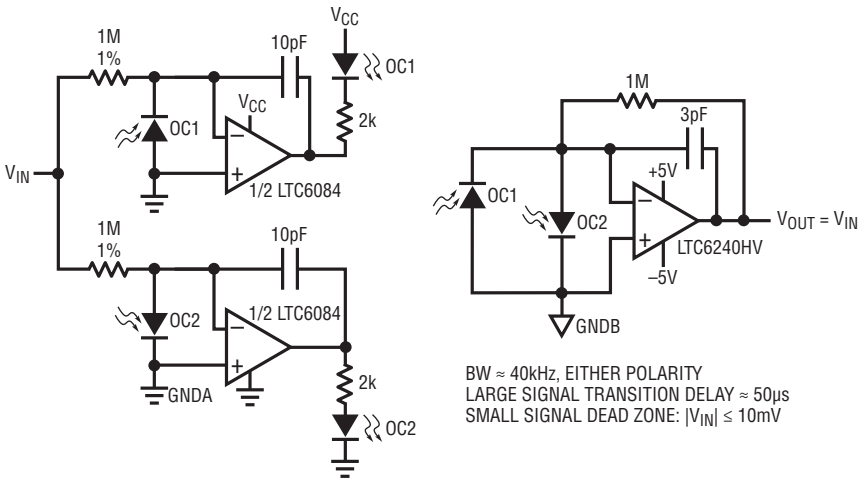
TYPICAL APPLICATION

Bipolar Analog Isolation Amplifier



BW ≈ 40kHz, EITHER POLARITY
LARGE SIGNAL TRANSITION DELAY ≈ 50µs
SMALL SIGNAL DEAD ZONE: $|V_{IN}| \leq 10mV$

V_{CC} = 5V,
V_{IN} = ±5V
RELATIVE TO GNDA

OC1, OC2: AVAGO TECHNOLOGIES HCNR201
www.avagotech.com

V_{OUT} = ±5V,
RELATIVE TO GNDB

60845 TA03

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6078/LTC6079	Dual/Quad Micropower Precision Rail-to-Rail Op Amps	25µV $V_{OS(MAX)}$, 0.7µV/°C V_{OS} Drift(MAX), 1pA $I_{BIAS(MAX)}$
LTC6081/LTC6082	Dual/Quad Precision Rail-to-Rail Input/Output Amps	70µV $V_{OS(MAX)}$, 0.8µV/°C V_{OS} Drift(MAX), 1pA $I_{BIAS(MAX)}$
LTC6087/LTC6088	Dual/Quad 14MHz Rail-to-Rail Input/Output Amps	750µV $V_{OS(MAX)}$, 5µV/°C V_{OS} Drift(MAX), 1pA I_{BIAS}
LTC6240/LTC6241/ LTC6242	Single/Dual/Quad Low Noise Rail-to-Rail Output Op Amps	7nV/$\sqrt{Hz}$ Noise, 0.2pA I_{BIAS}, 18MHz Gain Bandwidth
LTC6244	Dual Low Noise Rail-to-Rail Output Op Amps	8nV/$\sqrt{Hz}$ Noise, 1pA I_{BIAS}, 50MHz Gain Bandwidth

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