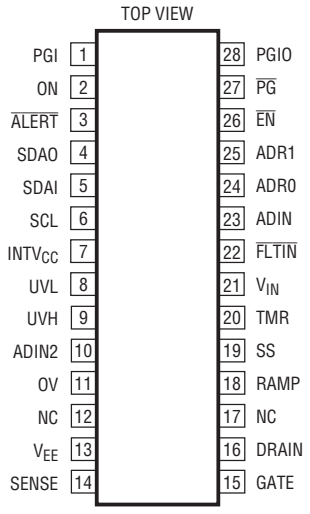
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

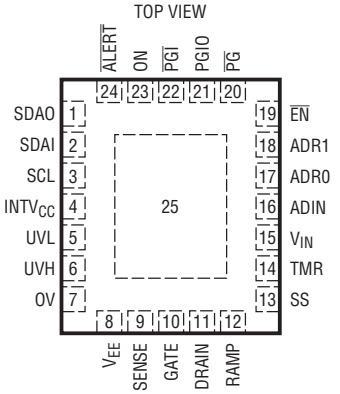
V_{IN} (Note 3)..... –0.3V to 10.65V
Drain (Note 4) ..... –0.3V to 3.5V
$\overline{PGI}$, ON, $\overline{ALERT}$, SDAO, SDAI, SCL, ADIN, ADIN2, OV, SENSE, ADR1, ADR0, $\overline{FLTIN}$, TMR, SS, RAMP Voltages .....–0.3V to $INTV_{CC}$ + 0.3V
UVL, UVH, $\overline{EN}$ ..... –0.3V to 10V
GATE Voltage ..... –0.3V to V_{IN} + 0.3V
$\overline{PG}$, PGIO Voltages ..... –0.3V to 80V
Supply Voltage ($INTV_{CC}$)..... –0.3V to 5.5V

Operating Ambient Temperature Range
LTC4261C ..... 0°C to 70°C
LTC4261I .....–40°C to 85°C
Storage Temperature Range
SSOP .....–65°C to 150°C
QFN.....–65°C to 125°C
Lead Temperature (Soldering, 10 sec)
SSOP Only .....300°C

PIN CONFIGURATION



GN PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 85°C/W



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4261CGN#PBF	LTC4261CGN#TRPBF	LTC4261CGN	28-Lead Plastic SSOP	0°C to 70°C
LTC4261IGN#PBF	LTC4261IGN#TRPBF	LTC4261IGN	28-Lead Plastic SSOP	–40°C to 85°C
LTC4261CGN-2#PBF	LTC4261CGN-2#TRPBF	LTC4261IGN-2	28-Lead Plastic SSOP	0°C to 70°C
LTC4261IGN-2#PBF	LTC4261IGN-2#TRPBF	LTC4261IGN-2	28-Lead Plastic SSOP	–40°C to 85°C
LTC4261CUFD#PBF	LTC4261CUFD#TRPBF	4261	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4261IUFD#PBF	LTC4261IUFD#TRPBF	4261	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4261CUFD-2#PBF	LTC4261CUFD-2#TRPBF	42612	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4261IUFD-2#PBF	LTC4261IUFD-2#TRPBF	42612	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at I_{IN} = 5mA, T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
General								
V_Z	Shunt Regulator Voltage at V_{IN}	I_{IN} = 5mA		●	10.65	11.2	11.8	V
ΔV_Z	Shunt Regulator Load Regulation	I_{IN} = 5mA to 25mA		●		370	600	mV
I_{IN}	V_{IN} Supply Current	$V_{IN} = V_Z - 0.3V$		●		2	5	mA
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising		●	8.5	9	9.5	V
$\Delta V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Hysteresis			●	0.3	0.7	1	V
$INTV_{CC}$	Internal Regulator Voltage	I_{LOAD} = 1mA to 20mA, I_{IN} = 25mA		●	4.75	5	5.25	V
Gate Drive								
V_{GATEH}	GATE Pin Output High Voltage	V_{IN} = 10.65V		●	10	10.25	10.5	V
$I_{GATE(UP)}$	GATE Pin Pull-Up Current	V_{GATE} = 4V		●	–7.5	–11.5	–15.5	µA
$I_{GATE(OFF)}$	GATE Turn-Off Current	V_{SENSE} = 400mV, V_{GATE} = 4V		●	45	90	120	mA
		Gate Off, V_{GATE} = 4V		●	60	110	140	mA
$t_{PHL(SENSE)}$	SENSE High to Current Limit Propagation Delay	V_{SENSE} = 100mV, GATE Open		●		0.5	1.5	µs
		V_{SENSE} = 300mV, GATE Open		●		0.2	0.5	µs
$t_{PHL(GATE)}$	GATE Off Propagation Delay	Input High (OV, $\overline{EN}$, $\overline{PGI}$), Input Low (ON, UVL), GATE Open		●		0.2	0.5	µs
t_{PHLCB}	Circuit Breaker Gate Off Delay	V_{GATE} < 2V, GATE Open		●	440	530	620	µs
I_{RAMP}	RAMP Pin Current	V_{SS} = 2.56V		●	–18	–20	–22	µA
V_{SS}	SS Pin Clamp Voltage			●	2.43	2.56	2.69	V
$I_{SS(UP)}$	SS Pin Pull-Up Current	V_{SS} = 0V		●	–7	–10	–13	µA
$I_{SS(DN)}$	SS Pin Pull-Down Current	V_{SS} = 2.56V		●	6	12	20	mA
Input Pins								
$V_{UVH(TH)}$	UVH Threshold Voltage	V_{UVH} Rising	LTC4261C LTC4261I	● ●	2.534 2.522	2.56 2.56	2.586 2.598	V
$V_{UVL(TH)}$	UVL Threshold Voltage	V_{UVL} Falling	LTC4261C LTC4261I	● ●	2.263 2.254	2.291 2.291	2.319 2.328	V
$\Delta V_{UV(HYST)}$	Built-In UV Hysteresis	UVH and UVL Tied Together		●	256	269	282	mV
δV_{UV}	UVH, UVL Minimum Hysteresis					15		mV
$V_{UVLR(TH)}$	UVL Reset Threshold Voltage	V_{UVL} Falling		●	1.12	1.21	1.30	V
$\Delta V_{UVLR(HYST)}$	UVL Reset Hysteresis					60		mV
$V_{OV(TH)}$	OV Pin Threshold Voltage	V_{OV} Rising	LTC4261C LTC4261I	● ●	1.744 1.735	1.770 1.770	1.796 1.805	V
$\Delta V_{OV(HYST)}$	OV Pin Hysteresis			●	18	37.5	62	mV
ΔV_{SENSE}	Current Limit Sense Voltage Threshold	$V_{SENSE} - V_{EE}$		●	45	50	55	mV
$V_{INPUT(TH)}$	ON, $\overline{EN}$, $\overline{PGI}$, $\overline{FLTIN}$ Threshold Voltage	ON, $\overline{EN}$, $\overline{PGI}$, $\overline{FLTIN}$ Falling or Rising		●	0.8	1.4	2	V
$\Delta V_{INPUT(HYST)}$	ON, $\overline{EN}$, $\overline{PGI}$, $\overline{FLTIN}$ Hysteresis					170		mV
$V_{PGIO(TH)}$	PGIO Pin Input Threshold Voltage	V_{PGIO} Rising		●	1.10	1.25	1.40	V
$\Delta V_{PGIO(HYST)}$	PGIO Pin Input Hysteresis					100		mV
I_{INPUT}	ON, $\overline{EN}$, UVH, UVL, OV, SENSE, $\overline{PGI}$, $\overline{FLTIN}$ Input Current	ON, $\overline{EN}$, UVH, UVL, OV, SENSE, $\overline{PGI}$, $\overline{FLTIN}$ = 3V		●		0	±2	µA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at I_{IN} = 5mA, T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timer							
$V_{TMR(H)}$	TMR Pin High Threshold	V_{TMR} Rising	●	2.43	2.56	2.69	V
$V_{TMR(L)}$	TMR Pin Low Threshold	V_{TMR} Falling	●	40	75	110	mV
$I_{TMR(UP)}$	TMR Pin Pull-Up Current	Turn-On and Auto-Retry (Except OC) Delays, V_{TMR} = 0.2V	●	–7	–10	–13	µA
		Power Good, $\overline{PGI}$ Check and OC Auto-Retry Delays, V_{TMR} = 0.2V	●	–3.5	–5	–6.5	µA
$I_{TMR(DN)}$	TMR Pin Pull-Down Current	Delays Except $\overline{PGI}$ Check or OC Auto-Retry, V_{TMR} = 2.56V	●	6	12	20	mA
		$\overline{PGI}$ Check and OC Auto-Retry Delays, V_{TRM} = 2.56V	●	3	5	7	µA
Output Pins							
V_{PWRGD}	$\overline{PG}$, PGIO Pins Output Low	$I_{\overline{PG}}$, I_{PGIO} = 3mA $I_{\overline{PG}}$, I_{PGIO} = 500µA	● ●		0.8 0.15	1.6 0.4	V V
I_{PWRGD}	$\overline{PG}$, PGIO Pins Leakage Current	$\overline{PG}$, PGIO = 80V	●		0	±10	µA
ADC							
	Resolution (No Missing Codes)	(Note 5)	●	10			Bits
INL	Integral Nonlinearity	SENSE	●		±0.5	±2.5	LSB
		ADIN2/OV, ADIN	●		±0.25	±1.25	LSB
V_{OS}	Offset Error	SENSE	●			±1.75	LSB
		ADIN2/OV, ADIN	●			±1.25	LSB
	Full-Scale Voltage	SENSE	●	62.8	64	65.2	mV
		ADIN2/OV, ADIN	●	2.514	2.560	2.606	V
	Total Unadjused Error	SENSE	●			±1.8	%
		ADIN2/OV, ADIN	●			±1.6	%
	Conversion Rate		●	5.5	7.3	9	Hz
R_{ADIN}	ADIN, ADIN2 Pins Input Resistance	ADIN, ADIN2 = 1.28V	●	2	10		MΩ
I_{ADIN}	ADIN, ADIN2 Pins Input Current	ADIN, ADIN2 = 2.56V	●		0	±2	µA
I^2C Interface							
$V_{ADR(H)}$	ADR0, ADR1 Input High Threshold		●	$INTV_{CC}$ – 0.8	$INTV_{CC}$ – 0.5	$INTV_{CC}$ – 0.3	V
$V_{ADR(L)}$	ADR0, ADR1 Input Low Threshold		●	0.3	0.5	0.8	V
$I_{ADR(IN)}$	ADR0, ADR1 Input Current	ADR0, ADR1 = 0V, 5V	●			±80	µA
		ADR0, ADR1 = 0.8V, ($INTV_{CC}$ – 0.8V)	●	±10			µA
$V_{\overline{ALERT}(OL)}$	$\overline{ALERT}$ Pin Output Low Voltage	$I_{\overline{ALERT}}$ = 4mA	●		0.2	0.4	V
$V_{SDAO(OL)}$	SDAO Pin Output Low Voltage	I_{SDAO} = 4mA	●		0.2	0.4	V
$I_{SDAO,\overline{ALERT}(IN)}$	SDAO, $\overline{ALERT}$ Input Current	SDAO, $\overline{ALERT}$ = 5V	●		0	±5	µA
$V_{SDAI,SCL(TH)}$	SDAI, SCL Input Threshold		●	1.6	1.8	2	V
$I_{SDAI,SCL(IN)}$	SDAI, SCL Input Current	SDAI, SCL = 5V	●		0	±2	µA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at I_{IN} = 5mA, T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Interface Timing (Note 5)							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency			400			kHz
t_{LOW}	Minimum SCL Low Period				0.65	1.3	µs
t_{HIGH}	Minimum SCL High Period				50	600	ns
$t_{BUF(MIN)}$	Minimum Bus Free Time Between Stop/Start Condition				0.12	1.3	µs
$t_{HD,STA(MIN)}$	Minimum Hold Time After (Repeated) Start Condition				140	600	ns
$t_{SU,STA(MIN)}$	Minimum Repeated Start Condition Set-Up Time				30	600	ns
$t_{SU,STO(MIN)}$	Minimum Stop Condition Set-Up Time				30	600	ns
$t_{HD,DATI(MIN)}$	Minimum Data Hold Time Input				–100	0	ns
$t_{HD,DATO(MIN)}$	Minimum Data Hold Time Output			300	600	900	ns
$t_{SU,DAT(MIN)}$	Minimum Data Set-Up Time Input				30	100	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width			50	110	250	ns
t_{RST}	Stuck-Bus Reset Time	SCL or SDAI Held Low		25	66		ms
C_X	SCL,SDA Input Capacitance	SDAI Tied to SDAO			5	10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to device GND (V_{EE}) unless otherwise specified.

Note 3: An internal shunt regulator limits the V_{IN} pin to a minimum of 10.65V. Driving this pin to voltages beyond 10.65V may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current below 50mA.

Note 4: An internal clamp limits the DRAIN pin to a minimum of 3.5V. Driving this pin to voltages beyond the clamp may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current below 2mA.

Note 5: Guaranteed by design and not subject to test.

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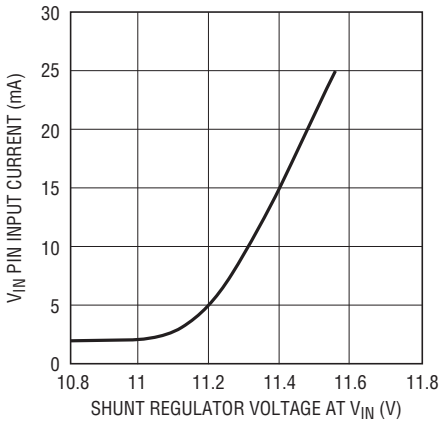
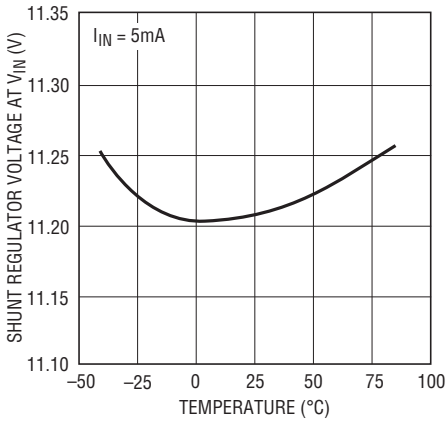
TYPICAL PERFORMANCE CHARACTERISTICS I_{IN} = 5mA, T_A = 25°C, unless otherwise noted

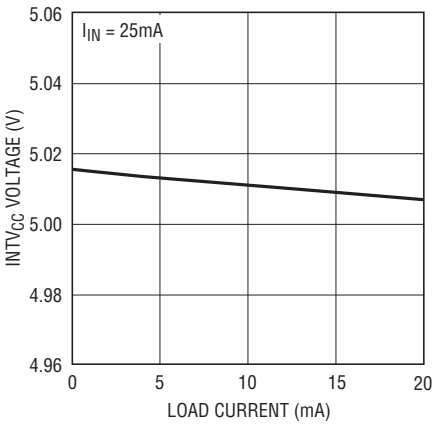
Shunt Regulator Voltage vs Input Current



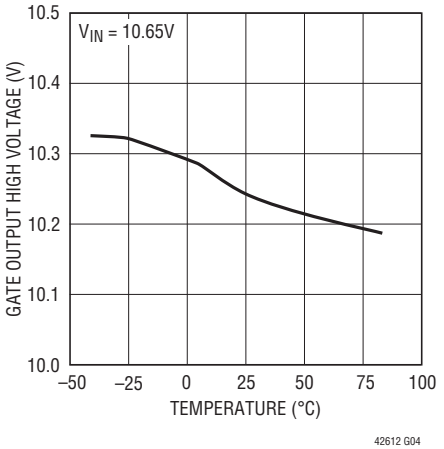
Shunt Regulator Voltage vs Temperature



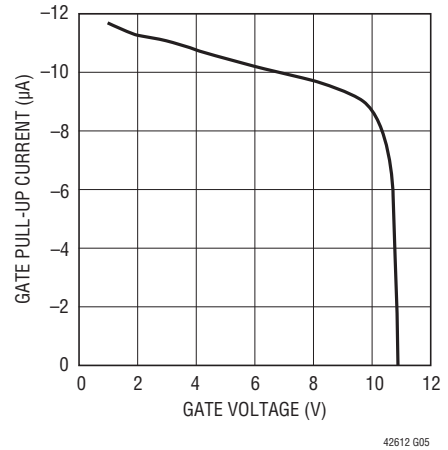
INTVCC vs Load Current



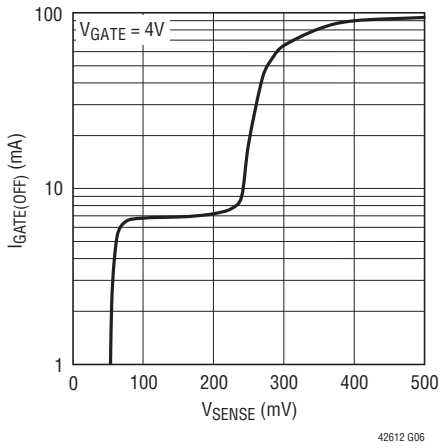
GATE Output High Voltage vs Temperature



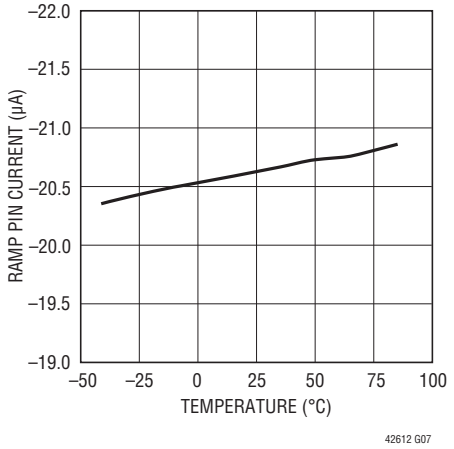
GATE Pull-Up Current vs GATE Voltage



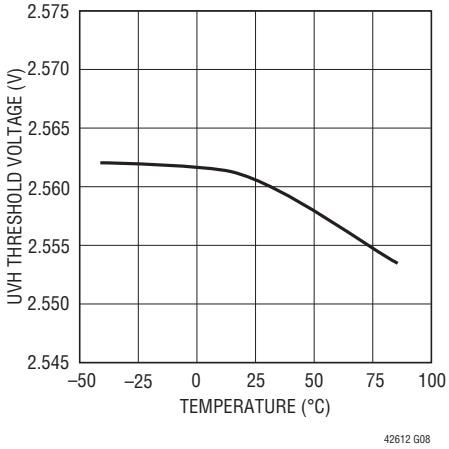
GATE Turn-Off Current vs SENSE Voltage



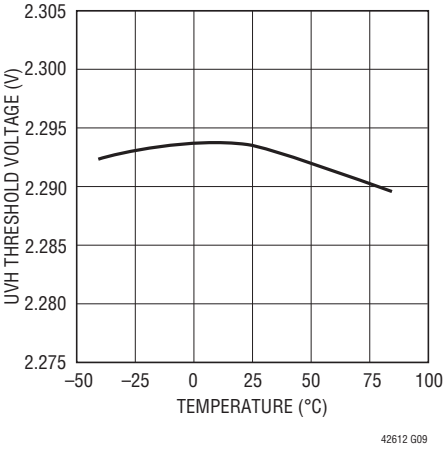
RAMP Pin Current vs Temperature



UVH Threshold vs Temperature



UVL Threshold vs Temperature



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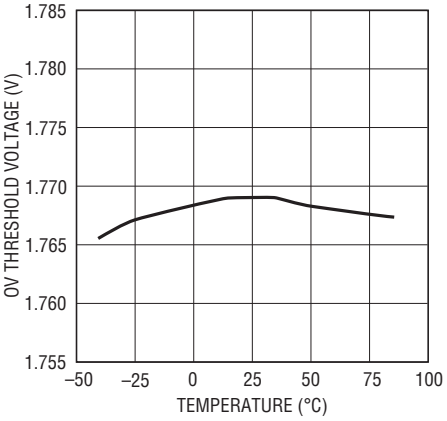
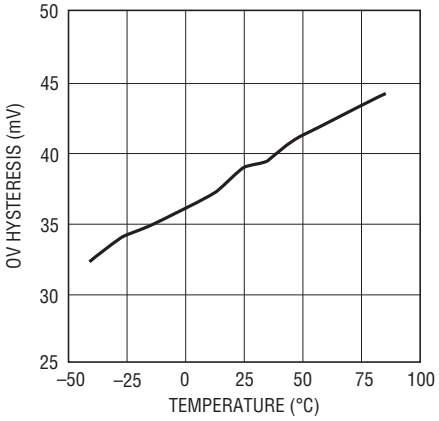
TYPICAL PERFORMANCE CHARACTERISTICS I_{IN} = 5mA, T_A = 25°C, unless otherwise noted

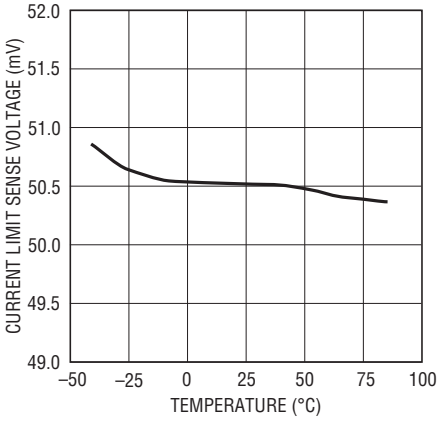
OV Threshold vs Temperature



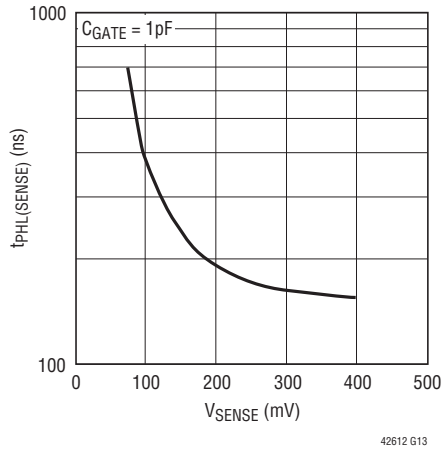
OV Hysteresis vs Temperature



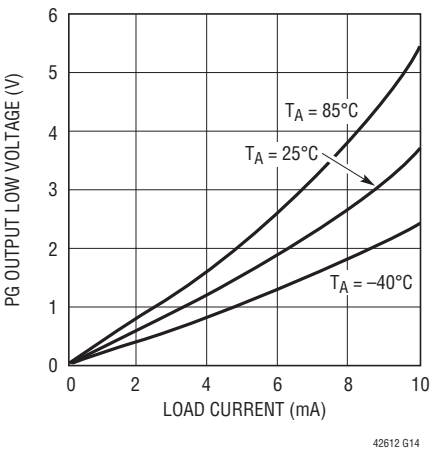
Current Limit Voltage vs Temperature



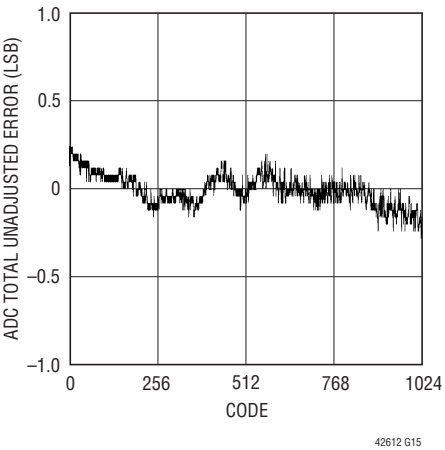
Current Limit Propagation Delay ($t_{PHL(SENSE)}$) vs V_{SENSE}



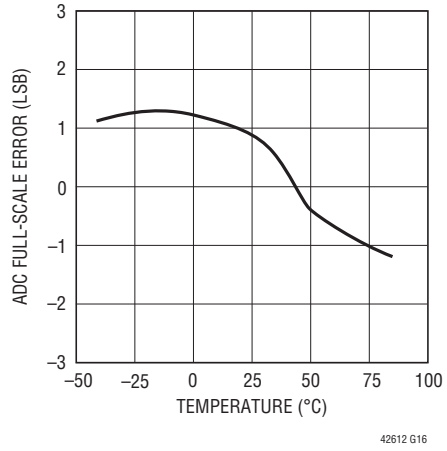
PG, PGIO Output Low vs Load Current



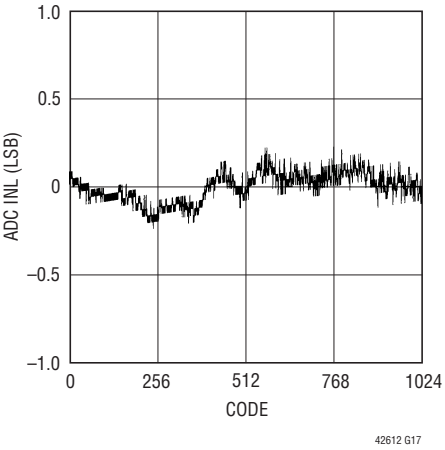
ADC Total Unadjusted Error vs Code (ADIN Pin)



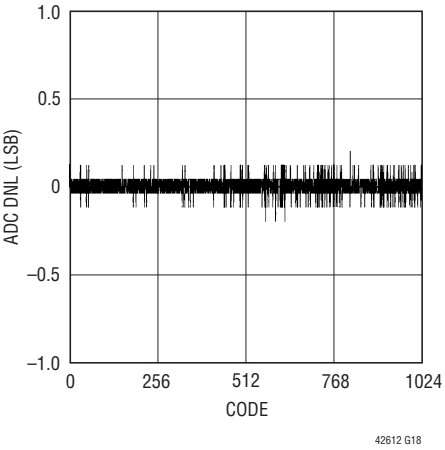
ADC Full-Scale Error vs Temperature (ADIN Pin)



ADC INL vs Code (ADIN Pin)



ADC DNL vs Code (ADIN Pin)



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PIN FUNCTIONS (SSOP/QFN)

ADIN (Pin 23/Pin 16): ADC Input. A voltage between 0V and 2.56V applied to this pin is measured by the on-chip ADC. Tie to V_{EE} if unused.

ADIN2 (Pin 10/NA): Second ADC Input. Not available on QFN package.

ADR0, ADR1 (Pins 24, 25/Pins 17, 18): Serial Bus Address Inputs. Tying these pins to V_{EE}, OPEN or $INTV_{CC}$ configures one of nine possible addresses. See Table 1 in Applications Information.

$\overline{ALERT}$ (Pin 3/Pin 24): Fault Alert Output. Open-drain logic output that pulls to V_{EE} when a fault occurs to alert the host controller. A fault alert is enabled by the $\overline{ALERT}$ register. See Applications Information. Connect to V_{EE} if unused.

DRAIN (Pin 16/Pin 11): Drain Sense Input. Connect an external 1M resistor between this pin and the drain terminal (V_{OUT}) of the N-channel FET. When the DRAIN pin voltage is less than 1.77V and the GATE pin voltage is above V_Z – 1.2V the power good outputs are asserted after a delay. The voltage at this pin is internally clamped to 4V.

$\overline{EN}$ (Pin 26/Pin 19): Device Enable Input. Pull low to enable the N-channel FET to turn-on after a start-up debounce delay set by the TMR pin. When this pin is pulled high, the FET is off. Transitions on this pin will be recorded in the FAULT register. A high-to-low transition activates the logic to read the state of the ON pin and clear faults. Requires external pull-up. Debouncing with an external capacitor is recommended when used to monitor board present. Connect to V_{EE} if unused.

Exposed Pad (Pin 25, QFN Only): Exposed Pad may be left open or connected to device ground (V_{EE}).

$\overline{FLTIN}$ (Pin 22/NA): General Purpose Fault Input. If this pin pulls low, the FAULT register bit B7 is latched to "1." This pin is used to sense an external fault condition and its status does not affect the FET control functions of the LTC4261. Not available on the QFN package. Connect to $INTV_{CC}$ if unused.

GATE (Pin 15/Pin 10): N-Channel FET Gate Drive Output. This pin is pulled up by an internal current source I_{GATE} (11.5µA when the SS pin reaches its clamping voltage). GATE stays low until V_{IN} and $INTV_{CC}$ cross the UVLO thresholds, UV and OV conditions are satisified and an adjustable timer delay expires. During turn-off, caused by faults or undervoltage lockout (V_{IN} or $INTV_{CC}$), a 110mA pull-down current between GATE and V_{EE} is activated.

$INTV_{CC}$ (Pin 7/Pin 4): Low Voltage (5V) Supply Output. This is the output of the internal linear regulator with an internal UVLO threshold of 4.25V. This voltage powers up the data converter and logic control circuitry. Bypass this pin with a 0.1µF capacitor to V_{EE}.

ON (Pin 2/Pin 23): On Control Input. A rising edge turns on the external N-channel FET while a falling edge turns it off. This pin is also used to configure the state of the FET ON register bit D3 in the CONTROL register (and hence the external FET) at power-up. For example if the ON pin is tied high, then the register bit D3 goes high one timer cycle after power-up. Likewise, if the ON pin is tied low, then the device remains off after power-up until the register bit D3 is set high using the I^2C bus. A high-to-low transition on this pin clears faults.

OV (Pin 11/Pin 7): Overvoltage Detection Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at the pin rises above 1.77V, the N-channel FET is turned off. The overvoltage condition does not affect the status of the power good outputs. On the QFN package, this pin is also measured by the on-chip ADC. Connect to V_{EE} if unused.

$\overline{PG}$ (Pin 27/Pin 20): Power Good Status Output. This open-drain pin pulls low and stays latched a timer delay after the FET is on (when GATE reaches V_Z – 1.2V and DRAIN is within 1.77V of V_{EE}). The power good output is reset in all GATE pull-down events except an overvoltage fault. Connect to V_{EE} if unused.

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PIN FUNCTIONS (SSOP/QFN)

$\overline{PGI}$ (Pin 1/Pin 22): Power Good Input. This pin along with the $\overline{PGI}$ check timer serves as a watchdog to monitor the power-up of the DC/DC converter. The $\overline{PGI}$ pin must be low before the $\overline{PGI}$ check timer expires, otherwise the GATE pin pulls down and stays latched and a power bad fault is logged into the FAULT register. The $\overline{PGI}$ timer is started after the second power good is latched and its delay is equal to four times the start-up debounce delay. Connect to V_{EE} if unused.

PGIO (Pin 28/Pin 21): General Purpose Input/Output. Open-drain logic output and logic input. Defaults to pull low a timer delay after the $\overline{PG}$ pin goes low to indicate a second power good output. Configure according to Table 6.

RAMP (Pin 18/Pin 12): Inrush Current Ramp Control Pin. The inrush current is set by placing a capacitor (C_R) between the RAMP pin and the drain terminal of the FET. At start-up, the GATE pin is pulled up by $I_{GATE(UP)}$ until the pass transistor begins to turn on. A current, I_{RAMP}, then flows through C_R to ramp down the output voltage V_{OUT}. The value of I_{RAMP} is controlled by the SS pin voltage. When the SS pin reaches its clamp voltage (2.56V), I_{RAMP} = 20µA. The ramp rate of V_{OUT} and the load capacitor C_L set the inrush current: $I_{INRUSH} = (C_L/C_R) \bullet I_{RAMP}$.

SCL (Pin 6/Pin 3): Serial Bus Clock Input. Data at the SDAI pin is shifted in and data at the SDAO pin is shifted out on rising edges of SCL. This is a high impedance pin that is generally connected to the output of the incoming optoisolator driven by the SCL port of the master controller. An external pull-up resistor or current source is required. Pull up to $INTV_{CC}$ if unused.

SDAI (Pin 5/Pin 2): Serial Bus Data Input. This is a high impedance input pin used for shifting in command bits, data bits and SDAO acknowledge bits. An external pull-up resistor or current source is required. Normally connected to the output of the incoming optoisolator that is driven by the SDA port of the master controller. If the master controller separates SDAI and SDAO, data read at SDAO needs to be echoed back to SDAI for proper I^2C communication. Pull up to $INTV_{CC}$ if unused.

SDAO (Pin 4/Pin 1): Serial Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. An external pull-up resistor or current source is required. Normally connected to the input of the outgoing optoisolator that outputs to the SDA port of the master controller. In the single-wire broadcast mode, the SDAO pin sends out selected data that is encoded with an internal clock.

SENSE (Pin 14/Pin 9): Current Limit Sense Input. Load current through the external sense resistor (R_S) is monitored and controlled by an active current limit amplifier to 50mV/R_S. Once V_{SENSE} reaches 50mV, a circuit breaker timer starts and turns off the pass transistor after 530µs. In the event of a catastrophic short circuit, if V_{SENSE} crosses 250mV, a fast response comparator immediately pulls the GATE pin down to control the current of the N-channel FET.

SS (Pin 19/Pin 13): Soft-Start Input. Connect a capacitor to this pin to control the rate of rise of inrush current (dI/dt) during start-up. An internal 10µA current source charging the external soft-start capacitor (C_{SS}) creates a voltage ramp. This voltage is converted to a current to charge the GATE pin up and to ramp the output voltage down. The SS pin is internally clamped to 2.56V limiting $I_{GATE(UP)}$ to 11.5µA and I_{RAMP} to 20µA. If the SS capacitor is absent, the SS pin ramps from 0V to 2.56V in 220µs.

TMR (Pin 20/Pin 14): Delay Timer Input. Connect a capacitor (C_{TMR}) to this pin to create timing delays at start-up, when power good outputs pull down, during PGI check and when auto-retrying after faults (except overvoltage fault). Internal pull-up currents of 10µA and 5µA and pull-down currents of 5µA and 12mA configure the delay periods as multiples of a nominal delay of 256ms • C_{TMR}/µF. Delays for start-up and auto-retry following undervoltage or power bad fault are the same as the nominal delay. Delays for sequenced power good outputs are twice of the nominal delay. Delays for $\overline{PGI}$ check and auto-retry following overcurrent fault are four times the nominal delay.

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PIN FUNCTIONS (SSOP/QFN)

UVH (Pin 9/Pin 6): Undervoltage High Level Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at the UVH pin rises above 2.56V the pass transistor is allowed to turn on. A small capacitor at this pin prevents transients and switching noise from affecting the UVH threshold. Connect to $INTV_{CC}$ if unused.

UVL (Pin 8/Pin 5): Undervoltage Low Level Input. Connect this pin to an external resistive divider from V_{EE}. If the voltage at the UVL pin drops below 2.291V, the pass transistor is turned off and the power good outputs go high impedance. Pulling this pin below 1.21V resets faults and allows the pass transistor to turn back on. Connect to $INTV_{CC}$ if unused.

V_{EE} (Pin 13/Pin 8): Negative Supply Voltage Input and Device Ground. Connect this pin to the negative side of the power supply.

V_{IN} (Pin 21/Pin 15): Positive Supply Input. Connect this pin to the positive supply through a dropping resistor. An internal shunt regulator clamps V_{IN} at 11.2V. An internal undervoltage lockout (UVLO) circuit holds the GATE low until V_{IN} is above 9V. Bypass this pin with a 1µF capacitor to V_{EE}.

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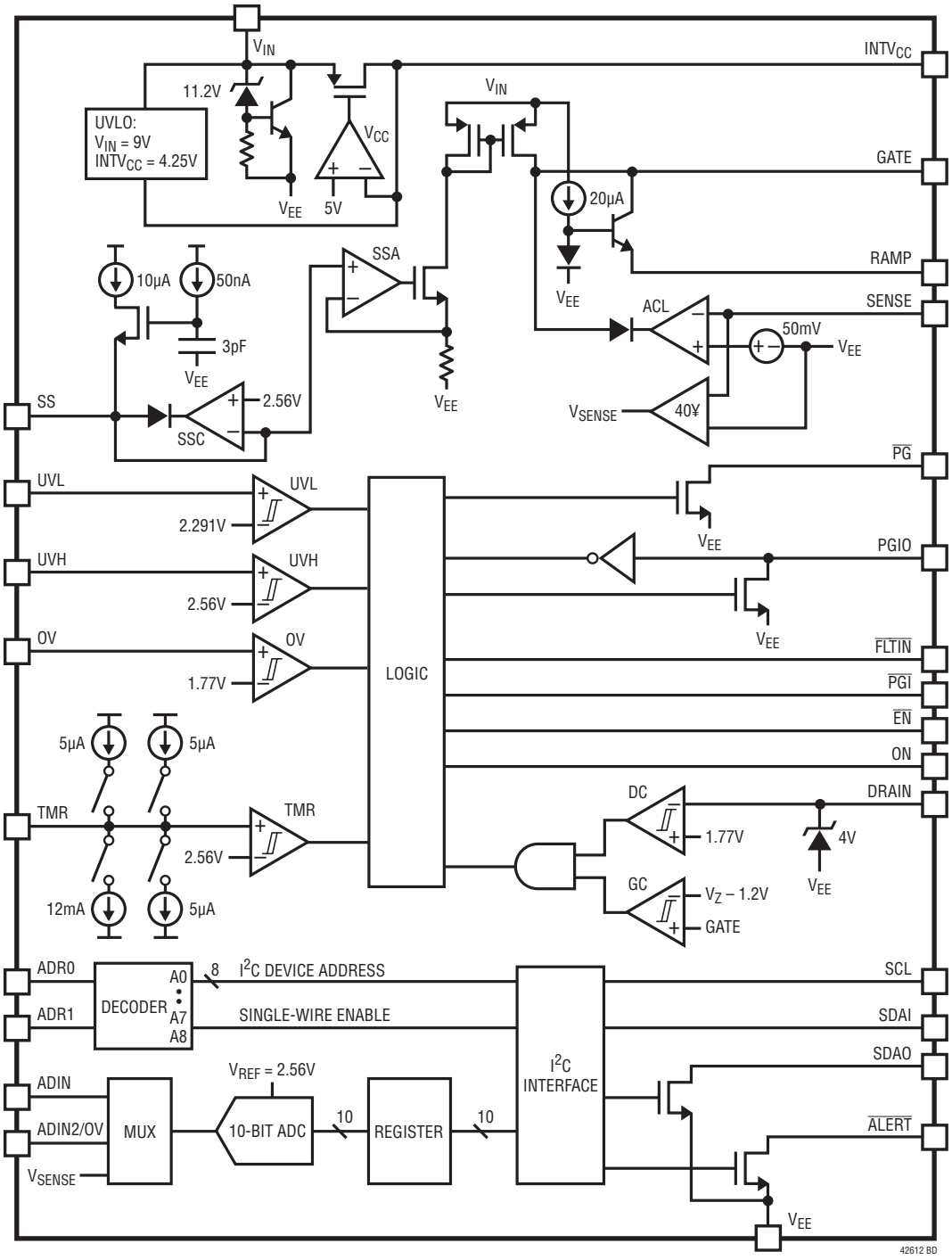
BLOCK DIAGRAM



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OPERATION

The LTC4261/LTC4261-2 are designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live –48V backplane. The devices also feature an onboard 10-bit ADC and I²C interface that allows monitoring board current, voltages and faults. The main functional circuits of the LTC4261/LTC4261-2 are illustrated in the Block Diagram.

In normal operation after a start-up debounce delay, the GATE pin turns on the external N-channel FET passing power to the load. The GATE pin is powered by a shunt regulated 11.2V supply on the V_{IN} pin that is derived from –48V RTN through a dropping resistor. The turn-on sequence starts by pulling the SS pin up. The voltage at the SS pin is converted to a current, $I_{GATE(UP)}$, pulling the GATE up. When the pass FET starts to turn on and charge the load capacitor, the inrush current flowing through the FET is a function of the capacitor at RAMP (C_R), the load capacitor (C_L) and the ramp current (I_{RAMP}) that flows from the RAMP pin to C_R:

$$I_{INRUSH} = I_{RAMP} \bullet \frac{C_L}{C_R}$$

I_{RAMP} and $I_{GATE(UP)}$ are approximately proportional to the SS pin voltage and are limited to 20µA and 11.5µA, respectively when SS reaches its clamping voltage (2.56V).

The ACL amplifier is used for overcurrent and short-circuit protection. It monitors the load current through the SENSE pin voltage and a sense resistor R_S. In an overcurrent condition, the ACL amplifier limits the current to 50mV/R_S by pulling down GATE in an active servo loop. After a 530µs timeout, the ACL amplifier turns off the pass FET. In the event of a catastrophic short circuit, when V_{SENSE} crosses 250mV, a fast response comparator immediately pulls the GATE pin down.

The DRAIN and the GATE voltages are monitored to determine if power is available for the load. Two power good signals are sequenced on the $\overline{PG}$ pin (first power good signal) and the PGIO pin (second power good signal), each with a debounce delay that is twice the start-up delay. The PGIO pin can also be used as a general purpose input or output. The $\overline{PGI}$ pin serves as a watchdog to monitor the output of the DC/DC module. If the module output fails to come up, the LTC4261/LTC4261-2 shut down.

The TMR pin generates delays for initial start-up, auto-retry following a fault, power good outputs and $\overline{PGI}$ check.

The logic circuits a re powered by an internally generated 5V supply (available on the $INTV_{CC}$ pin). Prior to turning on the pass FET, both V_{IN} and $INTV_{CC}$ voltages must exceed their undervoltage lockout thresholds. In addition, the control inputs UVH, UVL, OV, $\overline{EN}$, ON and $\overline{PGI}$ are monitored by comparators. The FET is held off until all start-up conditions are met.

A 10-bit analog-to-digital converter (ADC) is included in the LTC4261/LTC4261-2. The ADC measures SENSE resistor voltage as well as voltage at the ADIN2/OV (SSOP/QFN) and ADIN pins. The results are stored in on-board registers.

An I²C interface is provided to read the ADC data registers. It also allows the host to poll the device and determine if a fault has occurred. If the $\overline{ALERT}$ line is used as an interrupt, the host can respond to a fault in real time. The SDA line is divided into SDAI (input) and SDAO (output) to facilitate opto coupling with the system host. Two three-state pins, ADR0 and ADR1, are used to decode eight device addresses. The interface can also be configured through the ADR0 and ADR1 pins for a single-wire broadcast mode, sending ADC data and faults status through the SDAO pin to the host without clocking the SCL line. This single-wire, one-way communication simplifies system design by eliminating two optocouplers on SCL and SDAI that are required by an I²C interface.

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APPLICATIONS INFORMATION

The LTC4261/LTC4261-2 are ideally suited for –48V distributed power systems and AdvancedTCA systems. A basic 200W application circuit using the LTC4261 is shown in Figure 1. A more complete application circuit with AdvancedTCA connections is shown in Figure 2.

Input Power Supply

Power for the LTC4261/LTC4261-2 is derived from the –48V RTN through an external current limiting resistor (R_{IN}) to the V_{IN} pin. An internal shunt regulator clamps

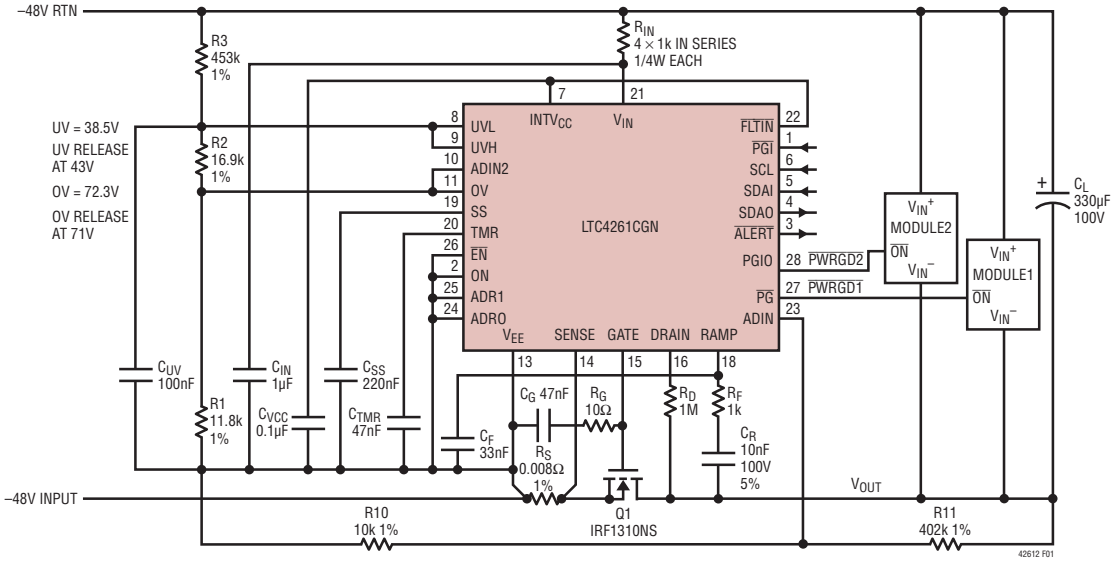

Figure 1. –48V/200W Hot Swap Controller Using LTC4261 with Current, Input Voltage and V_{DS} Monitoring (5.6A Current Limit, 0.66A Inrush)

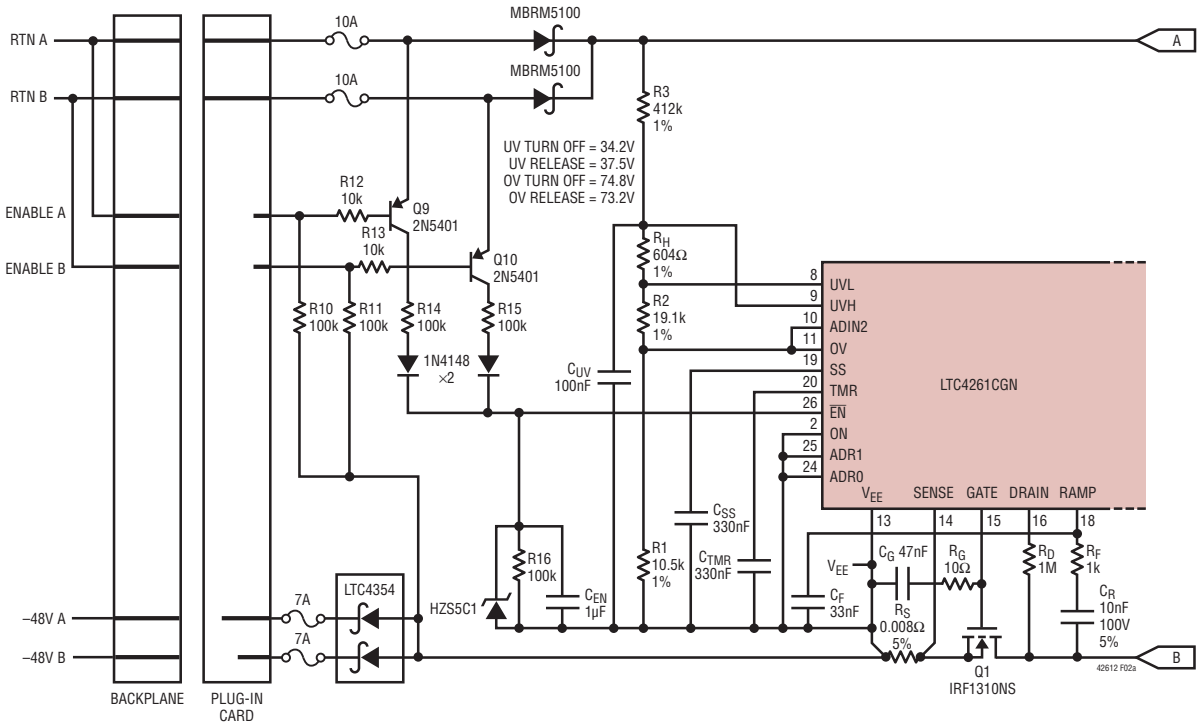

Figure 2a. 200W AdvancedTCA Hot Swap Controller with Input/Output Monitoring and Power Good Watchdog Using LTC4261 in I^2C Mode (Part One)

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APPLICATIONS INFORMATION

the voltage at V_{IN} to 11.2V (V_Z) and provides power to the GATE driver. The data converter and logic control circuits are powered by an internal linear regulator that derives 5V from the 11.2V supply. The 5V output is available at the $INTV_{CC}$ pin for driving external circuits (up to 20mA load current).

Bypass capacitors of 1µF and 0.1µF are recommended at V_{IN} and $INTV_{CC}$, respectively. R_{IN} should be chosen to accommodate the maximum supply current requirement of the LTC4261/LTC4261-2 (5mA) plus the supply current required by any external devices driven by the V_{IN} and $INTV_{CC}$ pins at the minimum intended operation voltage.

$$R_{IN} \leq \frac{V_{48V(MIN)} - V_{Z(MAX)}}{I_{IN(MAX)} + I_{EXTERNAL}}$$

The maximum power dissipation in the resistor is:

$$P_{MAX} = \frac{\left(V_{48V(MAX)} - V_{Z(MIN)}\right)^2}{R_{IN}}$$

If the power dissipation is too high for a single resistor, use multiple resistors in series or supply external loads from a separate NPN buffer as illustrated in Figure 3.

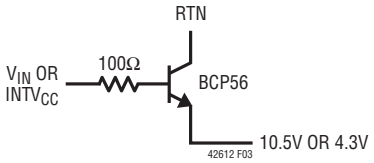

Figure 3. NPN Buffer Relieves R_{IN} of Excessive Dissipation when Supplying External Loads

Initial Start-Up and Inrush Control

Several conditions must be satisfied before the FET turn-on sequence is started. First the voltage at V_{IN} must exceed its 9V undervoltage lockout level. Next the internal supply $INTV_{CC}$ must cross its 4.25V undervoltage lockout level. This generates a 100µs to 160µs power-on-reset pulse during which the FAULT register bits are cleared and the CONTROL register bits are set or cleared as described in the register section. After the power-on-reset pulse, the voltages at the UVH, UVL and OV pins must satisfy UVH > 2.56V, UVL > 2.291V and OV < 1.77V to indicate that the input power is within the acceptable range and the $\overline{EN}$ pin must be pulled low. All the above conditions must be satisfied throughout the duration of the start-up debounce delay that is set by an external capacitor (C_{TMR}) connected to the TMR pin. C_{TMR} is charged with a pull-up current of

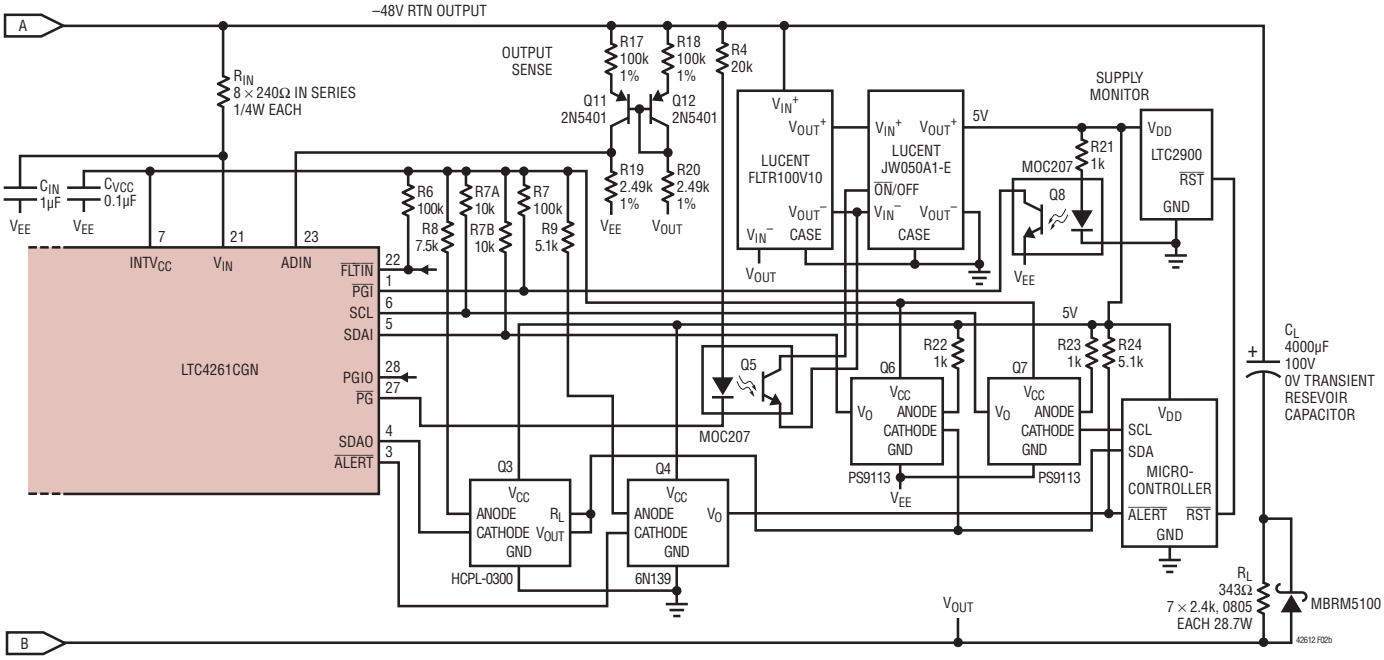

Figure 2b. 200W AdvancedTCA Hot Swap Controller with Input/Output Monitoring and Power Good Watchdog Using LTC4261 in I²C Mode (Part Two)

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APPLICATIONS INFORMATION

10µA until the voltage at TMR reaches 2.56V. C_{TMR} is then quickly discharged with a 12mA current. The initial delay expires when TMR is brought below 75mV. The duration of the start-up delay is given by:

$$t_D = 256ms \bullet \frac{C_{TMR}}{1\mu F}$$

If any of the above conditions is violated before the start-up delay expires, C_{TMR} is quickly discharged and the turn-on sequence is restarted. After all the conditions are validated throughout the start-up delay, the ON pin is then checked. If it is high, the FET will be turned on. Otherwise, the FET will be turned on when the ON pin is raised high or the FET ON bit D3 in the CONTROL register is set to "1" through the I^2C interface.

The FET turn-on sequence follows by charging an external capacitor at the SS pin (C_{SS}) with a 10µA pull-up current and the voltage at SS (V_{SS}) is converted to a current ($I_{GATE(UP)}$) of 11.5µA· V_{SS}/2.56V for GATE pull-up. When the GATE reaches the FET threshold voltage, the inrush current starts to flow through the FET and a current (I_{RAMP}) of 20µA· V_{SS}/2.56V flows out of the RAMP pin and through an external capacitor (C_R) connected between RAMP and V_{OUT}. The SS voltage is clamped to 2.56V, which corresponds to $I_{GATE(UP)}$ = 11.5µA and I_{RAMP} = 20µA. The RAMP pin voltage is regulated at 1.1V and the ramp rate of V_{OUT} determines the inrush current:

$$I_{INRUSH} = 20\mu A \bullet \frac{C_L}{C_R}$$

The ramp rate of V_{SS} determines dI/dt of the inrush current:

$$\frac{dI_{INRUSH}}{dt} = 20\mu A \bullet \frac{C_L}{C_R} \bullet \frac{1\mu F}{256ms \bullet C_{SS}}$$

If C_{SS} is absent, an internal circuit pulls the SS pin from 0V to 2.56V in about 220µs.

When V_{OUT} is ramped down to V_{EE}, I_{GATE} returns to the GATE pin and pulls the GATE up to V_{GATEH}. Figure 4 illustrates the start-up sequence of the LTC4261/LTC4261-2.

During board insertion and input power step, an internal clamp turns on to hold the RAMP pin low. Capacitor C_F and resistor R_F suppress the noise at the RAMP pin. For proper operation, $R_F \bullet C_R$ should not exceed 50µs. The recommended value of C_F is 3 • C_R.

Power Good Monitors

When V_{DS} of the pass transistor falls below 1.77V and GATE pulls above V_Z – 1.2V, an internal power good signal is latched and a series of three delay cycles are started as shown in Figure 4. When the first delay cycle with a duration of $2t_D$ expires, the $\overline{PG}$ pin pulls low as a power good signal to turn on the first module. When the second delay cycle ($2t_D$) expires, the PGIO pin pulls low as a power good signal to turn on the second module. The third delay cycle with a duration of $4t_D$ is for $\overline{PGI}$ check. Before the third delay cycle expires, the $\overline{PGI}$ pin must be pulled low by an external supply monitor (such as the LTC2900 in Figure 2) to keep the FET on. Otherwise, the FET is turned off and the power bad fault (PBAD) is logged in the FAULT register. The $2t_D$ timer delay is obtained by charging C_{TMR} with a 5µA current and discharging C_{TMR} with a 12mA current when TMR reaches 2.56V. For the $4t_D$ timer delay, the charging and discharging currents of C_{TMR} are both 5µA. The power good signals at $\overline{PG}$ and PGIO are reset in all FET turn-off conditions except the overvoltage fault.

Turn-Off Sequence and Auto-Retry

In any of the following conditions, the FET is turned off by pulling down GATE with a 110mA current, and C_{SS} and C_{TMR} are discharged with 12mA currents.

1. The ON pin is low or the ON bit in the CONTROL register is set to 0.
2. The $\overline{EN}$ pin is high.
3. The voltage at UVL is lower than 2.291V and the voltage at UVH is lower than 2.56V (undervoltage fault).
4. The voltage at OV is higher than 1.77V (overvoltage fault).
5. The voltage at V_{IN} is lower than 9V (V_{IN} undervoltage lockout).

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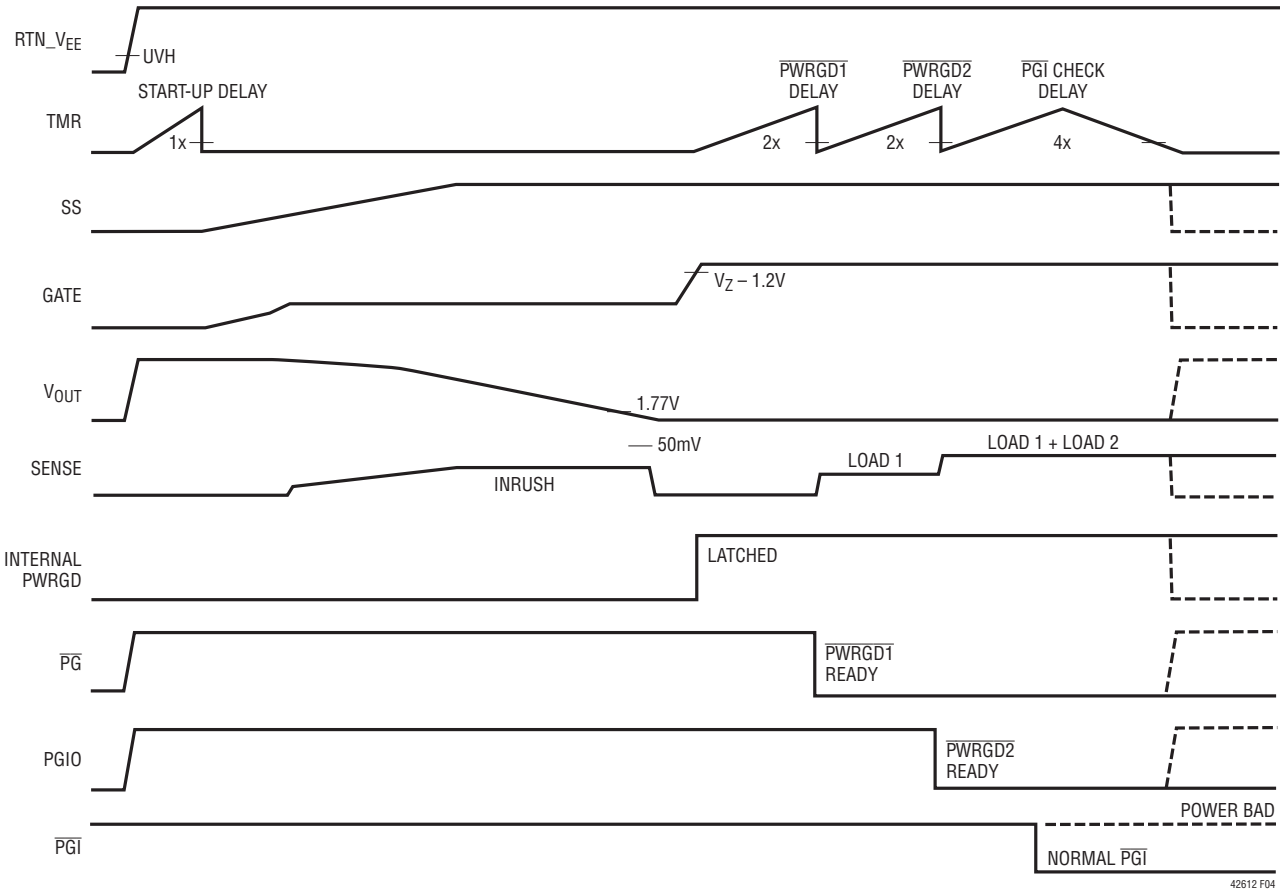

Figure 4. LTC4261 Turn-On Sequence

6. The voltage at $INTV_{CC}$ is lower than 4.25V ($INTV_{CC}$ undervoltage lockout).
7. V_{SENSE} > 50mV and the condition lasts longer than 530µs (overcurrent fault).
8. The $\overline{PGI}$ pin is high when the $\overline{PGI}$ check timer expires (power bad fault).

For conditions 1, 2, 5, 6, after the condition is cleared, the LTC4261/LTC4261-2 will automatically enter the FET turn-on sequence as previously described.

For any of the fault conditions 3, 4, 7, 8, the FET off mode is programmable by the corresponding auto-retry bit in the CONTROL register. If the auto-retry bit is set to 0, the FET is latched off upon the fault condition. If the auto-retry bit is set to 1, after the fault condition is cleared, a delay timer is started. After the timer expires, the FET enters the auto-retry mode and GATE is pulled up. The auto-retry delay following the undervoltage fault or the power bad fault has a duration of t_D. The auto-retry delay following the overcurrent fault has a duration of $4t_D$ for extra cooling time. The auto-retry following the overvoltage fault does not have a delay. The auto-retry control bits and their defaults at power up are listed in Table 6. Note that the LTC4261 defaults to latch-off while the LTC4261-2 defaults to auto-retry following the overcurrent fault.

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APPLICATIONS INFORMATION

$\overline{EN}$ and ON

Figure 5 shows a logic diagram for $\overline{EN}$ and ON as they relate to GATE, $\overline{ALERT}$ and internal registers A4, A7, B4, C4 and D3. Also affecting GATE is the status of UV, OV and several other fault conditions. The $\overline{EN}$ and ON pins have 0.8V to 2V logic thresholds relative to V_{EE} with a maximum input leakage current of ±2µA.

Register bit A4 indicates the present state of $\overline{EN}$, and B4 is set high whenever $\overline{EN}$ changes state. Rising and falling edges at the ON pin set and clear FET-on control bit, D3. Another path allows a falling edge at $\overline{EN}$ to latch a high state at the ON pin (such as when ON is permanently pulled high) into D3 after a time delay. Both B4 and D3 can be set or cleared directly by I^2C, and both are cleared low whenever $INTV_{CC}$ drops below its UVLO threshold. The condition of the GATE pin output is controlled by register bit A7, which is the AND of $\overline{A4}$, D3 and the absence of UV, OV and other faults.

Overcurrent Protection and Overcurrent Fault

The LTC4261/LTC4261-2 feature two levels of protection from short-circuit and overcurrent conditions. Load current is monitored by the SENSE pin and resistor R_S. There are two distinct thresholds for the voltage at SENSE: 50mV for engaging the active current limit loop and starting a 530µs circuit breaker timer and 250mV for a fast GATE pull-down to limit peak current in the event of a catastrophic short circuit or an input step.

In an overcurrent condition, when the voltage drop across R_S exceeds 50mV, the current limit loop is engaged and an internal 530µs circuit breaker timer is started. The current limit loop servos the GATE to maintain a constant output current of $50mV/R_S$. When the circuit breaker timer expires, the FET is turned off by pulling GATE down with a 110mA current, the capacitors at SS and TMR are discharged and the power good signals are reset. At this time, the overcurrent present bit A2 and the overcurrent fault bit B2 are set, and the circuit breaker timer is reset.

After the FET is turned off, the overcurrent present bit A2 is cleared. If the overcurrent auto-retry bit D2 has been set, the FET will turn on again automatically after a cooling time of $4t_D$. Otherwise, the FET will remain off until the overcurrent fault bit B2 is reset. When the overcurrent fault bit is reset (see Resetting Faults), the FET is allowed to turn on again after a delay of $4t_D$. The $4t_D$ cooling time associated with the overcurrent fault will not be interrupted by any other fault condition. See Figure 6 for operation of LTC4261/LTC4261-2 under overcurrent condition followed by auto-retry.

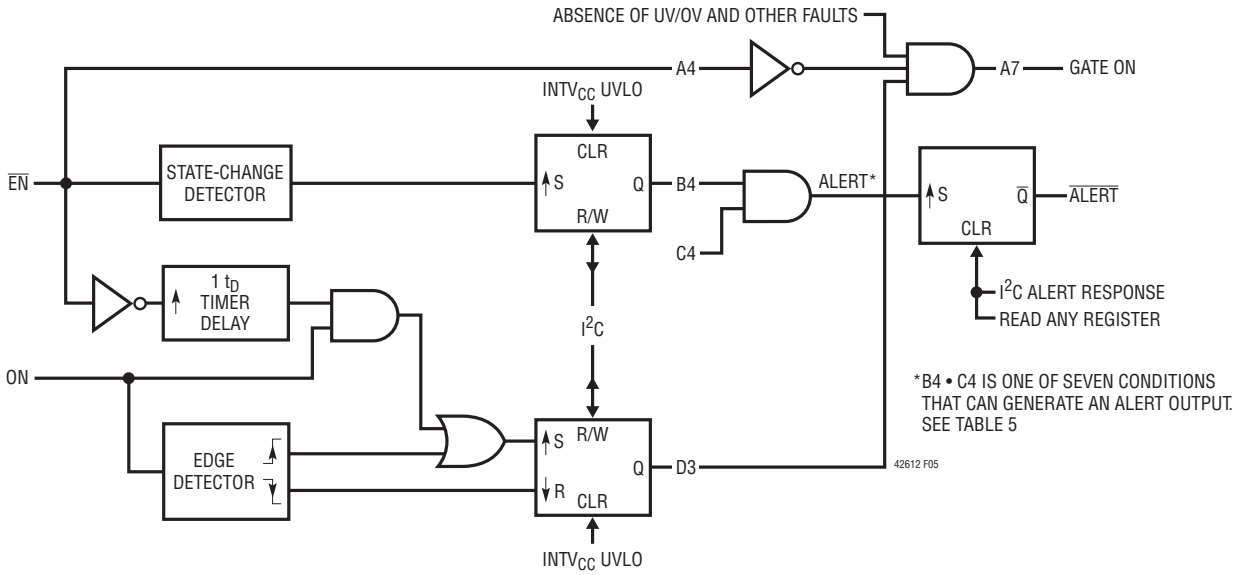

Figure 5. Logic Block Diagram of $\overline{EN}$ and ON Pins

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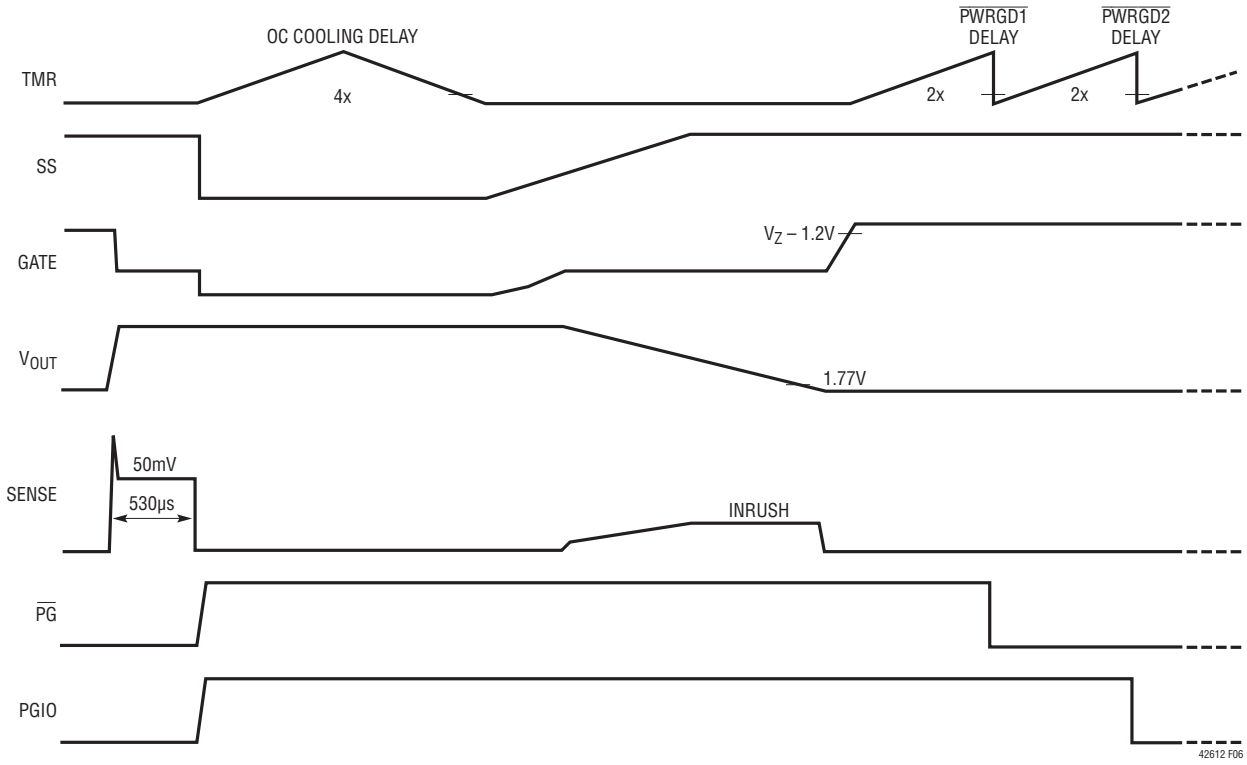

Figure 6. Overcurrent Fault and Auto-Retry

In the case of a low impedance short circuit on the load side or an input step during battery replacement, current overshoot is inevitable. A fast SENSE comparator with a threshold of 250mV detects the overshoot and immediately pulls GATE low. Once the SENSE voltage drops to 50mV, the current limit loop takes over and servos the current as previously described. If the short-circuit condition lasts longer than 530µs, the FET is shut down and the overcurrent fault is registered.

In the case of an input step, after an internal clamp pulls the RAMP pin down to 1.1V, the inrush control circuit takes over and the current limit loop is disengaged before the circuit breaker timer expires. From this point on, the device works as in the initial start-up: V_{OUT} is ramped down at the rate set by I_{RAMP} and C_R followed by GATE pull-up. The power good signals on the $\overline{PG}$ and PGIO pins, the TMR pin, and the SS pin are not interrupted through the input step sequence. The waveform in Figure 7 shows how the LTC4261/LTC4261-2 responds to an input step.

Note that the current limit threshold should be set sufficiently high to accommodate the sum of the load current and the inrush current to avoid engagement of the current limit loop in the event of an input step. The maximum value of the inrush current is given by:

$$I_{INRUSH} \leq 0.8 \bullet \frac{45mV}{R_S} - I_{LOAD}$$

where the 0.8 factor is used as a worst case margin combined with the minumum threshold (45mV).

The active current limit circuit is compensated using the capacitor C_G with a series resistor R_G (10Ω) connected between GATE and V_{EE}, as shown in Figure 1. The suggested value for C_G is 50nF. This value should work for most pass transistors (Q1).

Overvoltage Fault

An overvoltage fault occurs when the OV pin rises above its 1.77V threshold. This shuts off the pass transistor immediately, sets the overvoltage present bit A0 and the overvoltage fault bit B0, and pulls the SS pin down. Note that the power good signals are not affected by the overvoltage fault. If the OV pin subsequently falls back below the threshold, the pass transistor will be allowed to turn on again immediately (without delay) unless the

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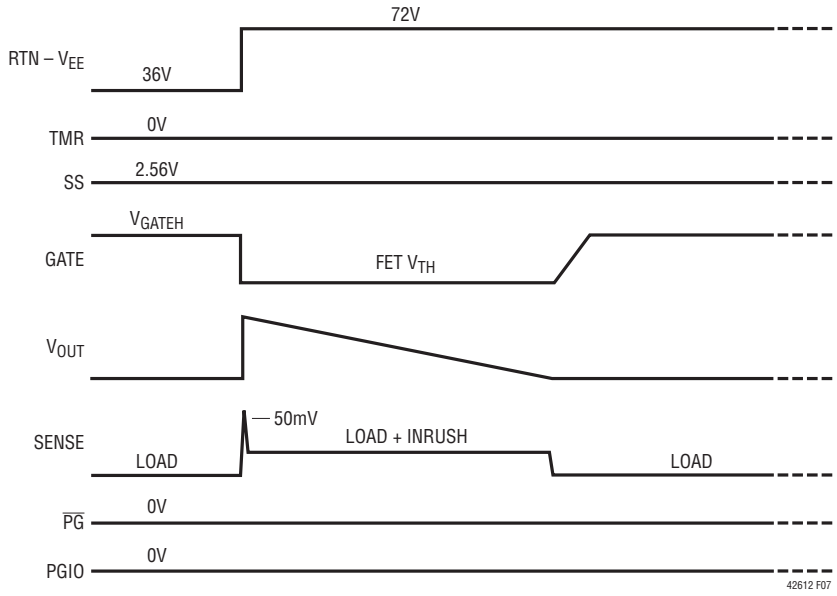

Figure 7. –36V to –72V Step Response

overvoltage auto-retry has been disabled by clearing register bit D0.

Undervoltage Comparator and Undervoltage Fault

The LTC4261/LTC4261-2 provide two undervoltage pins, UVH and UVL, for adjustable UV threshold and hysteresis. The UVH and UVL pins have the following accurate thresholds:

For UVH rising, $V_{UVH(TH)}$ = 2.56V, turn on

For UVL falling, $V_{UVL(TH)}$ = 2.291V, turn off

Both UVH and UVL pins have a minimum hysteresis of δV_{UV} (15mV typical). In either a rising or a falling input supply, the undervoltage comparator works in such a way that both the UVH and the UVL pins have to cross their thresholds for the comparator output to change state.

The UVH, UVL, and OV threshold ratio is designed to match the standard telecom operating range of 43V to 71V and UV hysteresis of 4.5V when UVH and UVL are tied together as in Figure 1, where the built-in UV hysteresis referred to the UVL pin is:

$$\Delta V_{UV(HYST)} = V_{UVH(TH)} - V_{UVL(TH)} = 0.269V$$

Using R1 = 11.8k, R2 = 16.9k and R3 = 453k as in Figure 1 gives a typical operating range of 43.0V to 70.7V, with an undervoltage shutdown threshold of 38.5V and an overvoltage shutdown threshold of 72.3V.

The UV hysteresis can be adjusted by separating the UVH and the UVL pins with a resistor R_H (Figure 8). To increase the UV hysteresis, the UVL tap should be placed above the UVH tap as in Figure 8a. To reduce the UV hysteresis, place the UVL tap under the UVH tap as in Figure 8b. UV hysteresis referred to the UVL pin is given by:

for $V_{UVL} \geq V_{UVH}$,

$$\Delta V_{UVL(HYST)} = \Delta V_{UV(HYST)} + 2.56V \bullet \frac{R_H}{R1+R2}$$

or for $V_{UVL} < V_{UVH}$,

$$\Delta V_{UVL(HYST)} = \Delta V_{UV(HYST)} - 2.56V \bullet \frac{R_H}{R1+R2+R_H}$$

For $V_{UVL} < V_{UVH}$, the minimum UV hysteresis allowed is the minimum hysteresis at UVH and UVL: δV_{UV} = 15mV when $R_{H(MAX)}$ = 0.11 • (R1 + R2)

The design of the LTC4261/LTC4261-2 protects the UV comparator from chattering even when R_H is larger than $R_{H(MAX)}$.

An undervoltage fault occurs when the UVL pin falls below 2.291V and the UVH pin falls below 2.56V – δV_{UV}. This activates the FET turn-off and sets the undervoltage

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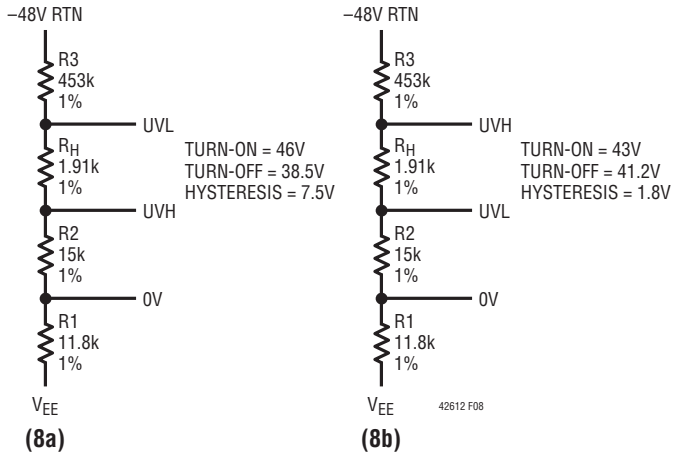

Figure 8. Adjustment of Undervoltage Thresholds for Larger (8a) or Smaller (8b) Hysteresis

present bit A1 and the undervoltage fault bit B1. The power good signals at $\overline{PG}$ and PGIO are also reset.

The undervoltage present bit A1 is cleared when the UVH pin rises above 2.56V and the UVL pin rises above 2.291V + δV_{UV}. After a delay of t_D, the FET will turn on again unless the undervoltage auto-retry has been disabled by clearing bit D1.

When power is applied to the device, if UVL is below the 2.291V threshold and UVH is below 2.56V – δV_{UV} after $INTV_{CC}$ crosses its undervoltage lock out threshold (4.25V), an undervoltage fault will be logged in the fault register.

Because of the compromises of selecting from a table of discrete resistor values (1% resistors in 2% increments, 0.1% resistors in 1% increments), best possible OV and UV accuracy is achieved using separate dividers for each pin. This increases the total number of resistors from three or four to as many as six, but maximizes accuracy, greatly simplifies calculations and facilitates running changes to accommodate multiple standards or customization without any board changes.

To improve noise immunity, put the resistive divider to the UV and OV pins close to the chip and keep traces to RTN and V_{EE} short. A 0.1µF capacitor from the UVH or UVL pin (and OV pin through resistor R2) to V_{EE} helps reject supply noise.

FET Short Fault

A FET short fault will be reported if the data converter measures a current sense voltage greater than or equal to 2mV while the FET is turned off. This condition sets the FET short present bit A5 and the FET short fault bit B5.

Power Bad Fault

After the FET is turned on and the power good outputs pull $\overline{PG}$ and PGIO low, a delay timer with duration of $4t_D$ is started and the level of the $\overline{PGI}$ pin is checked (Figure 3). If the $\overline{PGI}$ pin is pulled below its 1.4V threshold before the $\overline{PGI}$ check timer expires, the FET will remain on. Otherwise, the FET is immediately turned off, the power good signals are reset and the power bad present bit A3 and the power bad fault bit B3 are set. After the FET is turned off, the power bad present bit A3 will be cleared. If the $\overline{PGI}$ pin is subsequently pulled low, the FET will remain off unless the power bad auto-retry has been enabled by setting bit D4 or the power bad fault bit B3 is cleared. In either of those two conditions, the FET will turn on again following a delay of t_D and the $\overline{PGI}$ pin is checked again as described above.

External Fault Monitors

The $\overline{FLTIN}$ pin (SSOP only) and the PGIO pin, when configured as general purpose input, allow monitoring of external fault conditions such as broken fuses. If $\overline{FLTIN}$ is pulled below its 1.4V threshold, bit B7 in the FAULT register is set. An associated alert bit, C7, is also available in the ALERT register. When the PGIO pin is configured as general purpose input, if the voltage at PGIO is above 1.25V, both bit A6 in the STATUS register and bit B6 in the FAULT register are set, though there is no alert bit associated with this fault. The external fault conditions do not directly affect the GATE control functions.

Fault Alerts

When any of the fault bits in FAULT register B is set, an optional bus alert can be generated by setting the appropriate bit in the $\overline{ALERT}$ register C. This allows only selected faults to generate alerts. At power-up the default state is not to alert on faults. If an alert is enabled, the corresponding

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fault will cause the $\overline{\text{ALERT}}$ pin to pull low. After the bus master controller broadcasts the alert response address, the LTC4261/LTC4261-2 will respond with its address on the SDA line and release $\overline{\text{ALERT}}$ as shown in Figure 14. If there is a collision between two LTC4261's responding with their addresses simultaneously, then the device with the lower address wins arbitration and responds first. The $\overline{\text{ALERT}}$ line will also be released if the device is addressed by the bus master.

Once the $\overline{\text{ALERT}}$ signal has been released for one fault, it will not be pulled low again until the FAULT register indicates a different fault has occurred, or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated FAULT register bit has been cleared.

Resetting Faults

Faults are reset with any of the following conditions. First, writing zeros to the FAULT register B will clear the associated fault bits. Second, the entire FAULT register is cleared when either the ON pin or bit D3 goes from high to low, or if $INTV_{CC}$ falls below its 4.25V undervoltage lockout. Pulling the UVL pin below its 1.21V reset threshold also clears the entire FAULT register. When the UVL pin is brought back above 1.21V but below 2.291V, the undervoltage fault bit B1 is set if the UVH pin is below 2.56V. This can be avoided by holding the UVH pin above 2.56V while toggling the UVL pin to reset faults. Finally, when $\overline{\text{EN}}$ is brought from high to low, all fault bits except bit B4 are cleared. The bit B4 that indicates an $\overline{\text{EN}}$ change of state will be set.

Fault bits with associated conditions that are still present (as indicated in the STATUS Register A) cannot be cleared. The FAULT register will not be cleared when auto-retrying. When auto-retry is disabled, the existence of B0 (overvoltage), B1 (undervoltage), B2 (overcurrent) or B3 (power bad) fault keeps the FET off. After the fault bit is cleared and a delay of t_D (for B0, B1 and B3) or $4t_D$ (for B4) expires, the FET will turn on again. Note that if the overvoltage fault bit B0 is cleared by writing a zero through I^2C, the FET is allowed to turn on without a delay. If auto-retry is enabled, then a high value in A0, A1, A2 or A3 will hold the FET off and the FAULT register is ignored. Subsequently, when the A0, A1, A2 and A3 bits are cleared, the FET is allowed to turn on again.

Turning the LTC4261/LTC4261-2 On and Off

Many methods of on/off control are possible using the ON, $\overline{\text{EN}}$, UV/OV, $\overline{\text{FLTIN}}$ or PGIO pins along with the I^2C port. The $\overline{\text{EN}}$ pin works well with logic inputs or floating switch contacts; I^2C control is intended for systems where the board operates only under command of a central control processor and the ON pin is useful with signals referenced to RTN, as are the UV (UVH, UVL) and OV pins. PGIO and $\overline{\text{FLTIN}}$ control nothing directly, but are useful for I^2C monitoring of connection sense or other important signals.

On/off control is possible with or without I^2C intervention. Further, the LTC4261/LTC4261-2 may reside on either the removable board or on the backplane. Even when operating autonomously, the I^2C port can still exercise control over the GATE output, although depending on how they are connected, $\overline{\text{EN}}$ and ON could subsequently override conditions set by I^2C. UV, OV and other fault conditions seize control as needed to turn off the GATE output, regardless of the state of $\overline{\text{EN}}$, ON or the I^2C port. Figure 9 shows five configurations of on/off control of the LTC4261/LTC4261-2.

Determining factors in selecting a pin configuration for autonomous operation are the polarity and voltage of the controlling signal.

Optical Isolation. Figure 9a shows an opto-isolator driving the ON pin. Rising and falling edges at the ON pin turn the GATE output on and off. If ON is already high when power is applied, GATE is delayed one t_D period. The status of ON can be examined or overridden through the I^2C port at register bit D3. This circuit works in both backplane and board resident applications.

Logic Control. Figure 9b shows an application using logic signal control. Again, the ON pin is used as an input; all remarks made concerning opto-isolator control apply here as well.

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Ejector Switch or Loop-Through Connection Sense. Floating switch contacts or a connection sense loop also work well with the ON pin, replacing the phototransistor in Figure 9a. If an insertion debounce delay is desired, use the $\overline{EN}$ pin as shown in Figure 9c. Like Figures 9a and 9b, this circuit works on either side of the backplane connector.

Short Pin to RTN. Figure 9d uses the UV divider string to detect board insertion. This method works equally well in both backplane and board resident applications.

AdvancedTCA Style Control. Figure 2 shows an ATCA application using $\overline{EN}$ as the interface to the LTC4261. Register bit A4 allows the I²C port to monitor the status of $\overline{EN}$ and by setting C4 high, bit B4 can generate an alert to instantly report any changes in the state of $\overline{EN}$.

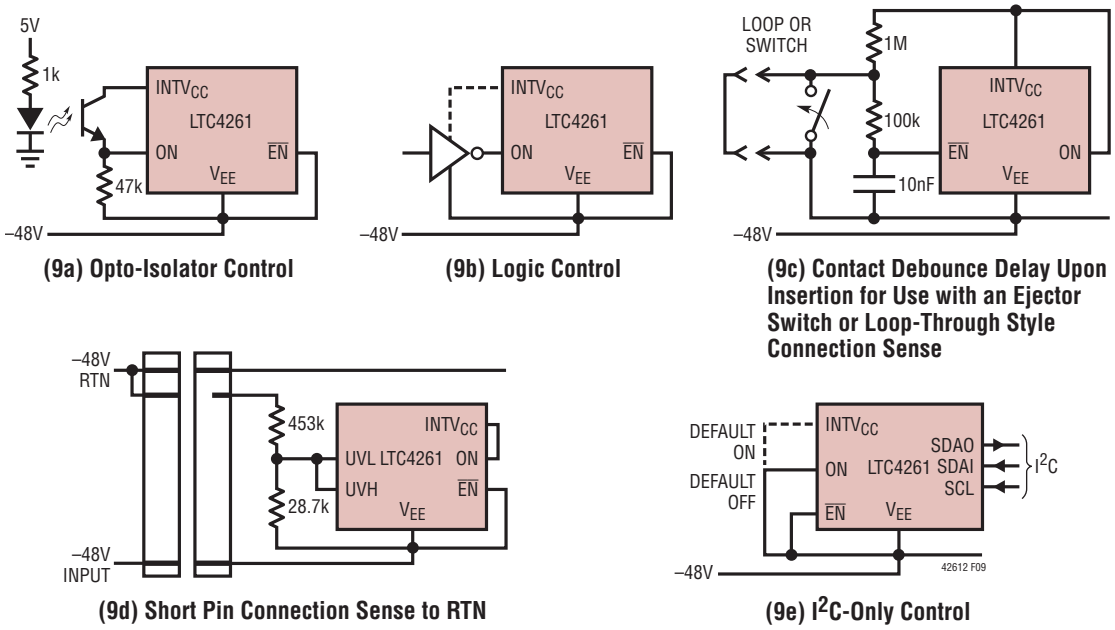
I²C Only Control. To lock out $\overline{EN}$ and ON, use the configuration shown in Figure 9e and control the GATE pin with register bit D3. The circuit defaults off at power up. To default on, connect the ON pin to $INTV_{CC}$. Either $\overline{FLTIN}$ or PGIO can be used as an input to monitor a connection sense or other control signal. PGIO is configured as an input by setting register bits D6 and D7 high; its input state is stored at location B6. $\overline{FLTIN}$ is always an input whose state is available from register bit B7. $\overline{FLTIN}$ generates an alert if C7 is set high.

Data Converter

The LTC4261/LTC4261-2 incorporates a 10-bit ΔΣ analog-to-digital converter (ADC) that continuously monitors three different voltages at (in the sequence of) SENSE, ADIN2/OV (SSOP/QFN) and ADIN. The ΔΣ architecture inherently averages signal noise during the measurement period. The voltage between the SENSE pin and V_{EE} is monitored with a 64mV full scale and 62.5μV resolution, and the data is stored in registers E and F. The ADIN and the ADIN2/OV pins are monitored with a 2.56V full scale and 2.5mV resolution. The data for the ADIN2/OV pin is stored in registers G and H. The data for the ADIN pin is stored in registers I and J.

The results in registers E, F, G, H, I and J are updated at a frequency of 7.3Hz. Setting CONTROL register bit D5 invokes a test mode that halts updating of these registers so that they can be written to and read from for software testing. By invoking the test mode right before reading the ADC data registers, the 10-bit data separated in two registers are synchronized.

The ADIN and ADIN2 pins can be used to monitor input and output voltages of the Hot Swap controller as shown in Figures 1 and 2.



(9a) Opto-Isolator Control

(9b) Logic Control

(9c) Contact Debounce Delay Upon Insertion for Use with an Ejector Switch or Loop-Through Style Connection Sense

(9d) Short Pin Connection Sense to RTN

(9e) I²C-Only Control

Figure 9. On/Off Control of the LTC4261

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Configuring the PGIO Pin

Table 6 describes the possible states of the PGIO pin using the CONTROL register bits D6 and D7. At power-up the default state is for the PGIO pin to pull low when the second power good signal is ready. Other uses for the PGIO pin are to go high impedence when the second power good is ready, a general purpose output and a general purpose input. When the PGIO pin is configured as a general purpose output, the status of bit C6 is sent out to the pin. When it is configured as a general purpose input, if the input voltage at PGIO is higher than 1.25V, both bit A6 in the STATUS register and bit B6 in the FAULT register are set. If the input voltage at PGIO subsequently drops below 1.25V, bit A6 is cleared. Bit B6 can be cleared by resetting the FAULT register as described previously.

Design Example

As a design example, consider the 200W application with C_L = 330µF as shown in Figure 1. The operating voltage range is from 43V to 71V with a UV turn-off threshold of 38.5V.

The design flow starts with calculating the maximum input current:

$$I_{MAX} = \frac{200W}{36V} = 5.6A$$

where 36V is the minimum input voltage.

The selection of the sense resistor, R_S, is determined by the minimum current limit threshold and maximum input current:

$$R_S = \frac{\Delta V_{SENSE(MIN)}}{I_{MAX}} = \frac{45mV}{5.6A} = 8m\Omega$$

The inrush current is set to 0.66A using C_R:

$$C_R = C_L \bullet \frac{I_{RAMP}}{I_{INRUSH}} = 330\mu F \bullet \frac{20\mu A}{0.66A} = 10nF$$

The value of R_F and C_F are chosen to 1k and 33nF as discussed previously.

The FET is selected to handle the maximum power dissipation during start-up or an input step. The latter usually results in a larger power due to summation of the inrush current charging C_L and the load current. For a 36V input step, the total P^2t in the FET is approximated by:

$$P^2t = (36V \bullet I_{MAX})^2 \bullet \frac{t}{3}$$

where t is the time it takes to charge up C_L:

$$t = \frac{C_L \bullet 36V}{I_{INRUSH}} = \frac{330\mu F \bullet 36V}{0.66A} = 18ms$$

which gives a P^2t value of $244W^2s$.

Now the P^2t given by the SOA (safe operating area) curves of candidate FETs must be higher than $244W^2s$. The SOA curves of the IRF1310NS provide for 5A at 50V (250W) for 10ms, which gives a P^2t value of $625W^2s$ and satisfies the requirement.

Sizing R1, R2 and R3 for the required UV and OV threshold voltages:

$V_{UV(RISING)}$ = 43V, $V_{UV(FALLING)}$ = 38.5V, (using $V_{UVH(TH)}$ = 2.56V and $V_{UVH(TH)}$ = 2.291V)

$V_{OV(RISING)}$ = 72.3V, $V_{OV(FALLING)}$ = 70.7V (using $V_{OV(TH)}$ = 1.77V rising and 1.7325V falling)

Layout Considerations

To achieve accurate current sensing, a Kelvin connection is recommended (Figure 10). The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/square. Small resistances add up quickly in high current applications.

The V_{EE} pin of the LTC4261 should be connected to a separate plane that is different from the main –48V input plane. To improve noise immunity, as shown in Figure 10, the V_{EE} connections of all capacitors, resistive dividers, opto-isolators and I^2C common must be made directly to the local V_{EE} plane, not the –48V input plane.

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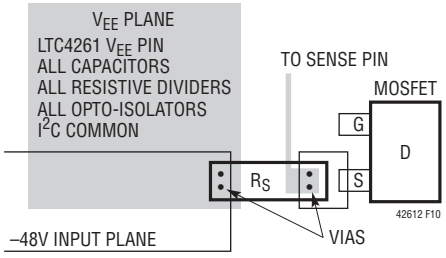

Figure 10. Layout Example of V_{EE} Plane, –48V Input Plane and Sense Resistor Connection

I²C Interface

The LTC4261/LTC4261-2 feature an I²C interface to provide access to the ADC data registers and four other registers for monitoring and control of the pass FET. Figure 11 shows a general data transfer format using the I²C. The LTC4261/LTC4261-2 are read-write slave devices and support SMBus bus Read Byte, Write Byte, Read Word and Write Word commands. The second word in a Read Word command will be identical to the first word. The second word in a Write Word command is ignored. The data formats for these commands are shown in Figures 12 to 15.

Using Opto-Isolators with SDA

The LTC4261/LTC4261-2 split the SDA line into SDAI (input) and SDAO (output) for convenience of opto-coupling with the host. If opto-isolators are not used then tie SDAI and SDAO together to form a normal SDA line. When using opto-isolators, connect the SDAI pin to the output of the incoming opto-isolator and connect the SDAO pin to the input of the outgoing opto-isolator (see Figure 2). If the SDAI and SDAO on the master controller are not tied together, the ACK bit of SDAO must be returned back to SDAI. If the $\overline{ALERT}$ line is used as an interrupt for the host to respond to a fault in real time, connect the $\overline{ALERT}$ pin to an opto-isolator in a way similar to that for the SDAO pin as shown in Figure 2.

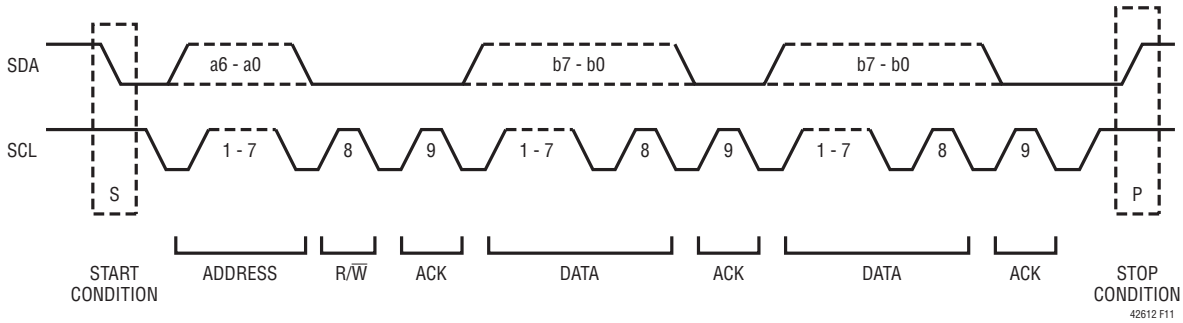

Figure 11. Data Transfer over I²C or SMBus

S	ADDRESS	W	A	COMMAND	A	DATA	A	P
	0 0 1 a3:a0	0	0	X X X X b3:b0	0	b7:b0	0	

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

42612 F12

Figure 12. LTC4261 Serial Bus SDA Write Byte Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	P
	0 0 1 a3:a0	0	0	X X X X b3:b0	0	b7:b0	0	X X X X X X X X	0	

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Figure 13. LTC4261 Serial Bus SDA Write Word Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	$\overline{A}$	P
	0 0 1 a3:a0	0	0	X X X X b3:b0	0		0 0 1 a3:a0	1	0	b7:b0	1	

42612 F14

Figure 14. LTC4261 Serial Bus SDA Read Byte Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	0 0 1 a3:a0	0	0	X X X X b3:b0	0		0 0 1 a3:a0	1	0	b7:b0	0	b7:b0	1	

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Figure 15. LTC4261 Serial Bus SDA Read Word Protocol

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START and STOP Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transiting SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transiting SDA from low to high while SCL is high. The bus is then free for another transmission.

Stuck-Bus Reset

The LTC4261/LTC4261-2 I^2C interface features a stuck-bus reset timer. The low conditions of the SCL and the SDAI pins are ORed to start the timer. The timer is reset when both SCL and SDAI are pulled high. If the SCL pin or the SDAI pin is held low for over 66ms, the stuck-bus timer will expire and the internal I^2C state machine will be reset to allow normal communication after the stuck-low condition is cleared. When the SCL pin and the SDAI pin are held low alternatively, if the ORed low period of SCL and SDAI exceeds 66ms before the timer reset condition (both SCL and SDAI are high) occurs, the stuck-bus timer will expire and the I^2C state machine is reset.

I^2C Device Addressing

Any of eight distinct I^2C bus addresses are selectable using the three-state pins ADR0 and ADR1, as shown in Table 1. Note that the configuration of ADR0 = L and ADR1 = H is used to enable the single-wire broadcasting mode. For the eight I^2C bus addresses, address bits B6, B5 and B4 are configured to (001) and the least significant bit B0 is the R/W bit. In addition, the LTC4261/LTC4261-2 will respond to two special addresses. Address (0011 111) is a mass write used to write to all LTC4261/LTC4261-2s, regardless of their individual address settings. Address (0001 100) is the SMBus Alert Response Address. If the LTC4261/LTC4261-2 are pulling low on the $\overline{\text{ALERT}}$ pin, it will acknowledge this address using the SMBus Alert Response Protocol.

Acknowledge

The acknowledge signal is used for handshaking between the transmitter and the receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. When the slave is the receiver, it must pull down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA HIGH, then the master can abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master must pull down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master will leave the SDA line HIGH (not acknowledge) and issue a STOP condition to terminate the transmission.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the R/W bit set to zero. The addressed LTC4261/LTC4261-2 acknowledge this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTC4261/LTC4261-2 acknowledge this and then latch the lower four bits of the command byte into its internal Register Address pointer. The master then delivers the data byte and the LTC4261/LTC4261-2 acknowledge once more and latch the data into its internal register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a Write Word command, the second data byte will be acknowledged by the LTC4261/LTC4261-2 but ignored.

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the R/W bit set to zero. The addressed LTC4261/LTC4261-2 acknowledge this and then the master sends a command byte that indicates which internal register the master wishes to read. The LTC4261/LTC4261-2 acknowledge this and then latch the lower four bits of the command byte into its internal Register Address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/$\overline{\text{W}}$ bit now set to one. The LTC4261/LTC4261-2 acknowledge and send the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the

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master acknowledges the transmitted data byte, as in a Read Word command, the LTC4261/LTC4261-2 will repeat the requested register as the second data byte. Note that the Register Address pointer is not cleared at the end of the transaction. Thus the Receive Byte protocol can be used to repeatedly read a specific register.

Alert Response Protocol

The LTC4261/LTC4261-2 implement the SMBus Alert Response Protocol as shown in Figure 16. If enabled to do so through the $\overline{\text{ALERT}}$ register C, the LTC4261/LTC4261-2 will respond to faults by pulling the $\overline{\text{ALERT}}$ pin low. Multiple LTC4261/LTC4261-2s can share a common $\overline{\text{ALERT}}$ line and the protocol allows a master to determine which LTC4261/LTC4261-2s are pulling the line low. The master begins by sending a START bit followed by the special Alert Response Address (0001 100)b with the R/W bit set to one. Any LTC4261/LTC4261-2 that is pulling its $\overline{\text{ALERT}}$ pin low will acknowledge and begin sending back its individual slave address.

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{\text{A}}$	P
	0 0 0 1 1 0 0	1	0	0 0 1 a3:a0 0	1	

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Figure 16. LTC4261 Serial Bus SDA Alert Response Protocol

An arbitration scheme ensures that the LTC4261/LTC4261-2 with the lowest address will have priority; all others will abort their response. The successful responder will then release its $\overline{\text{ALERT}}$ pin while any others will continue to hold their $\overline{\text{ALERT}}$ pins low. Polling may also be used to search for any LTC4261/LTC4261-2 that have detected faults. Any LTC4261/LTC4261-2 pulling its $\overline{\text{ALERT}}$ pin low will also release it if it is individually addressed during a read or write transaction.

The $\overline{\text{ALERT}}$ signal will not be pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated FAULT register bit has been cleared.

Single-Wire Broadcast Mode

The LTC4261/LTC4261-2 provides a single-wire broadcast mode in which selected register data are sent out to the SDAO pin without clocking the SCL line (Figure 17). The single-wire broadcast mode is enabled by setting the ADR1 pin high and the ADR0 pin low (the I^2C interface is disabled). At the end of each conversion of the three ADC channels, a stream of eighteen bits are broadcasted to SDAO with a serial data rate of 15.3kHz ±20% in a format as illustrated in Figure 18. The data bits are encoded with an internal clock in a way similar to Manchester encoding that can be easily decoded by a microcontroller or FPGA. Each data bit consists of a noninverting phase and an inverting phase. During the conversion of each ADC channel, SDAO is idle at high. At the end of the conversion, the SDAO pulls low. The START bit indicates the beginning of data broadcasting and is used along with the dummy bit (DMY) to measure the internal clock cycle (i.e., the serial data rate). Following the DMY bit are two channel code bits CH1 and CH0 labeling the ADC channel (see Table 10). Ten data bits of the ADC channel (ADC9-0) and three FAULT register bits (B2, B1 and B0) are then sent out. A parity bit (PRTY) ends each data stream. After that the SDAO line enters the idle mode with SDAO pulled high.

The following data reception procedure is recommended:

0. Wait for $INTV_{CC}$ rising edge.
1. Wait for SDAO falling edge.
2. The first falling edge could be a glitch, so check again after a delay of 10µs. If back to high, wait again. If still low, it is the START bit.
3. Use the following low-to-high and high-to-low transitions to measure 1/2 of the internal clock cycle.

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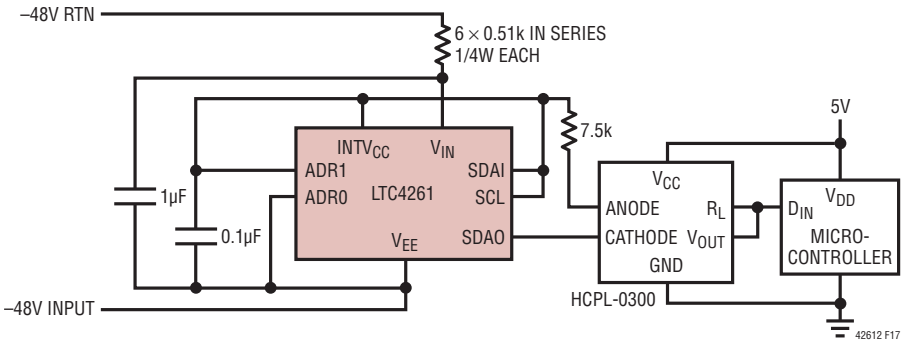

Figure 17. Single-Wire Broadcast Mode

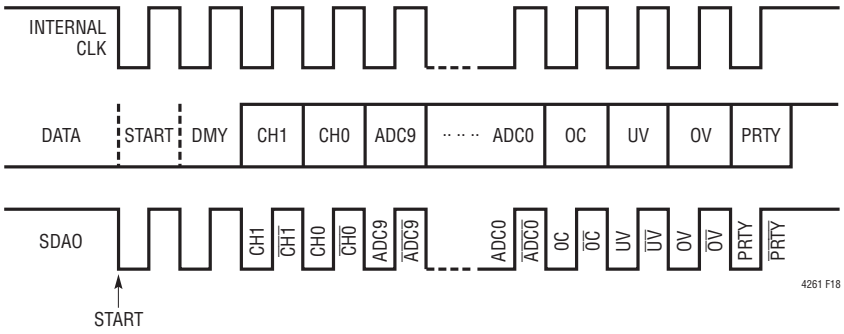

Figure 18. Single-Wire Broadcast Data Format

4. Wait for the second low-to-high transistion (middle of DMY bit).
5. Wait 3/4 of a clock cycle.
6. Sample bit CH1, wait for transistion.
7. Wait 3/4 of a clock cycle.
8. Sample bit CH0, wait for transistion.
9. Wait 3/4 of a clock cycle.
10. Sample ADC9, wait for transistion.
11. Continue until all bits are read.

The above procedure can be ported to a microcontroller or used to design a state machine in FPGA. Code should have timeouts in case an edge is missed. Abort the read if it takes more than double the typical time (1.2ms) for all 18 bits to be clocked out.

A typical application circuit with the LTC4261/LTC4261-2 in the broadcast mode is illustrated in Figure 19, where input voltage, V_{DS} of the FET and V_{SENSE} are monitored.

Register Addresses and Contents

The register addresses and contents are summerized in Table 1 and Table 2. The function of each register bit is detailed in Tables 3 to 9.

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Table 1. LTC4261 Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTC4261 ADDRESS PINS	
	h	6	5	4	3	2	1	0	R/$\overline{W}$	ADR1	ADR0
Mass Write	3E	0	0	1	1	1	1	1	0	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X
0	20	0	0	1	0	0	0	0	X	L	L
1	22	0	0	1	0	0	0	1	X	L	NC
2	24	0	0	1	0	0	1	0	X	H	NC
3	26	0	0	1	0	0	1	1	X	L	H
4	28	0	0	1	0	1	0	0	X	NC	L
5	2A	0	0	1	0	1	0	1	X	NC	NC
6	2C	0	0	1	0	1	1	0	X	H	H
7	2E	0	0	1	0	1	1	1	X	NC	H
8	Single-Wire Broadcast Mode									H	L

H = Tie to INV_{CC}; L = Tie to V_{EE}; NC = No connect, open; X = Don't care

Table 2. LTC4261 Register Address and Contents

REGISTER ADDRESS*	REGISTER NAME	READ/WRITE	DESCRIPTION
00h	STATUS (A)	R	System Status Information
01h	FAULT (B)	R/W	Fault Log and PGIO Input
02h	ALERT (C)	R/W	Controls Whether the $\overline{ALERT}$ Pin is Pulled Low After a Fault is Logged in the Fault Register
03h	CONTROL (D)	R/W	Controls Whether the Part Retries After Faults, Set the On/Off Switch State
04h	SENSE (E)	R/W**	ADC Current Sense Voltage Data (8 MSBs)
05h	SENSE (F)	R/W**	ADC Current Sense Voltage Data (2 LSBs)
06h	ADIN2/OV (G)	R/W**	ADC ADIN2/OV (SSOP/QFN) Voltage Data (8 MSBs)
07h	ADIN2/OV (H)	R/W**	ADC ADIN2/OV (SSOP/QFN) Voltage Data (2 LSBs)
08h	ADIN (I)	R/W**	ADC ADIN Voltage Data (8 MSBs)
09h	ADIN (J)	R/W**	ADC ADIN Voltage Data (2 LSBs)

*Register address MSBs b7-b4 are ignored. **Writable if bit D5 set.

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Table 3. STATUS Register A (00h)—Read Only

BIT	NAME	OPERATION
A7	FET On	Indicates State of FET; 1 = FET On, 0 = FET Off
A6	PGIO Input	Indicates State of the PGIO Pin when Configured to General Purpose Input: 1 = PGIO High, 0 = PGIO Low
A5	FET Short	Indicates Potential FET Short if Current Sense Voltage Exceeds 2mV While FET is Off; 1 = FET is Shorted, 0 = FET is Not Shorted
A4	$\overline{EN}$	Indicates State of the $\overline{EN}$ Pin; 1 = $\overline{EN}$ Pin High, 0 = $\overline{EN}$ Pin Low
A3	Power Bad	Indicates Power is Bad when $\overline{PGI}$ is High at the End of the $\overline{PGI}$ Check Timer; 1 = $\overline{PGI}$ High, 0 = $\overline{PGI}$ Low
A2	Overcurrent	Indicates Overcurrent Condition; 1 = Overcurrent, 0 = Not Overcurrent
A1	Undervoltage	Indicates Input Undervoltage when Both UVH and UVL are Low; 1 = UVH and UVL Low, 0 = UVH or UVL High
A0	Overvoltage	Indicates Input Overvoltage when OV is High; 1 = OV High, 0 = OV Low

Table 4. FAULT Register B (01h)—Read/Write

BIT	NAME	OPERATION
B7	External Fault Occurred	Latched to 1 if $\overline{FLTIN}$ Goes Low; 1 = $\overline{FLTIN}$ Low State Detected, 0 = $\overline{FLTIN}$ has Not Been Low
B6	PGIO Input High Occurred	Latched to 1 if the PGIO Pin Goes High when Configured to General Purpose Input; 1 = PGIO High Detected, 0 = PGIO has Been Low
B5	FET Short Fault Occurred	Indicates Potential FET Short was Detected When Measured Current Sense Voltage Exceeded 2mV While FET was Off; 1 = FET Short Fault Occurred, 0 = No FET Short Fault
B4	$\overline{EN}$ Changed State	Indicates That a Board was Inserted or Extracted when $\overline{EN}$ Changed State; 1 = $\overline{EN}$ Changed State, 0 = $\overline{EN}$ Unchanged
B3	Power Bad Fault Occurred	Indicates Power was Bad when $\overline{PGI}$ was High at the End of the PGI Check Timer; 1 = Power Bad Fault Occurred, 0 = No Power Bad Fault
B2	Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred; 1 = Overcurrent Fault Occurred, 0 = No Overcurrent Fault
B1	Undervoltage Fault Occurred	Indicates Input Undervoltage Fault Occurred when Both UVH and UVL went Low; 1 = Undervoltage Fault Occurred, 0 = No Undervoltage Fault
B0	Overvoltage Fault Occurred	Indicates Input Overvoltage Fault Occurred when OV was High; 1 = Overvoltage Fault Occurred, 0 = No Overvoltage Fault

Table 5. ALERT Register C (02h)—Read/Write

BIT	NAME	OPERATION
C7	External Fault Alert	Enables Alert for External Fault When $\overline{FLTIN}$ was Low; 1 = Enable Alert, 0 = Disable Alert (Default)
C6	PGIO Output	Output Data Bit to PGIO Pin when Configured as Output. Defaults to 0
C5	FET Short Alert	Enables Alert for FET Short Fault; 1 = Enable Alert, 0 = Disable Alert (Default)
C4	$\overline{EN}$ State Change Alert	Enables Alert when $\overline{EN}$ Changed State; 1 = Enable Alert, 0 Disable Alert (Default)
C3	Power Bad Alert	Enables Alert for Power Bad Fault; 1 = Enable Alert, 0 Disable Alert (Default)
C2	Overcurrent Alert	Enables Alert for Overcurrent Fault; 1 = Enable Alert, 0 Disable Alert (Default)
C1	Undervoltage Alert	Enables Alert for Undervoltage Fault; 1 = Enable Alert, 0 Disable Alert (Default)
C0	Overvoltage Alert	Enables Alert for Overvoltage Fault; 1 = Enable Alert, 0 Disable Alert (Default)

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Table 6. CONTROL Register D (03h)—Read/Write

BIT	NAME	OPERATION
D7:6	PGIO Configure	Configures Behavior of PGIO Pin FUNCTION / D6 / D7 / PGIO PIN $\overline{\text{Power Good}}$ (Default) / 0 / 0 / Open Drain Power Good / 0 / 1 / Open Drain General Purpose Output / 1 / 0 / PGIO = C6 General Purpose Input / 1 / 1 / PGIO = Hi-Z
D5	Test Mode Enable	Test Mode Halts ADC Operation and Enables Writes to ADC Registers; 1 = Enable Test Mode, 0 = Disable Test Mode (Default)
D4	Power Bad Auto-Retry	Enables Auto-Retry After a Power Bad Fault; 1 = Retry Enabled, 0 = Retry Disabled (Default)
D3	FET On Control	Turns FET On and Off; 1 = Turn FET On, 0 = Turn FET Off. Defaults to ON Pin State at End of Start-Up Debounce Delay
D2	Overcurrent Auto-Retry	Enables Auto-Retry After an Overcurrent Fault; 1 = Retry Enabled (Default, LTC4261-2), 0 = Retry Disabled (Default, LTC4261)
D1	Undervoltage Auto-Retry	Enables Auto-Retry After an Undervoltage Fault; 1 = Retry Enabled (Default), 0 = Retry Disabled
D0	Overvoltage Auto-Retry	Enables Auto-Retry After an Overvoltage Fault; 1 = Retry Enabled (Default), 0 = Retry Disabled

Table 7. SENSE Registers E (04h) and F (05h)—Read/Write

BIT	NAME	OPERATION
E7:0, F7:6	SENSE Voltage Data	10-Bit Data of Current Sense Voltage with 62.5µV LSB and 64mV Full Scale
F5:0	Reserved	Always Returns 0, Not Writable

Table 8. ADIN2/OV Registers G (06h) and H (07h)—Read/Write

BIT	NAME	OPERATION
G7:0, H7:6	ADIN2/OV Voltage Data	10-Bit Data of ADIN2/OV (SSOP/QFN) Voltage with 2.5mV LSB and 2.56V Full Scale
H5:0	Reserved	Always Returns 0, Not Writable

Table 9. ADIN Registers I (08h) and J (09h)—Read/Write

BIT	NAME	OPERATION
I7:0, J7:6	ADIN Voltage Data	10-Bit Data of ADIN Voltage with 2.5mV LSB and 2.56V Full Scale
J5:0	Reserved	Always Returns 0, Not Writable

Table 10. ADC Channel Labeling for Single-Wire Broadcast Mode

CH1	CH0	ADC CHANNEL
0	0	SENSE Voltage
0	1	ADIN2/OV (SSOP/QFN) Voltage
1	0	ADIN Voltage

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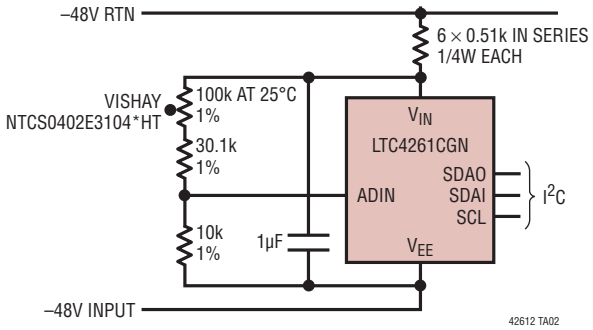
TYPICAL APPLICATION

Using the LTC4261 and a Thermistor to Monitor Temperature

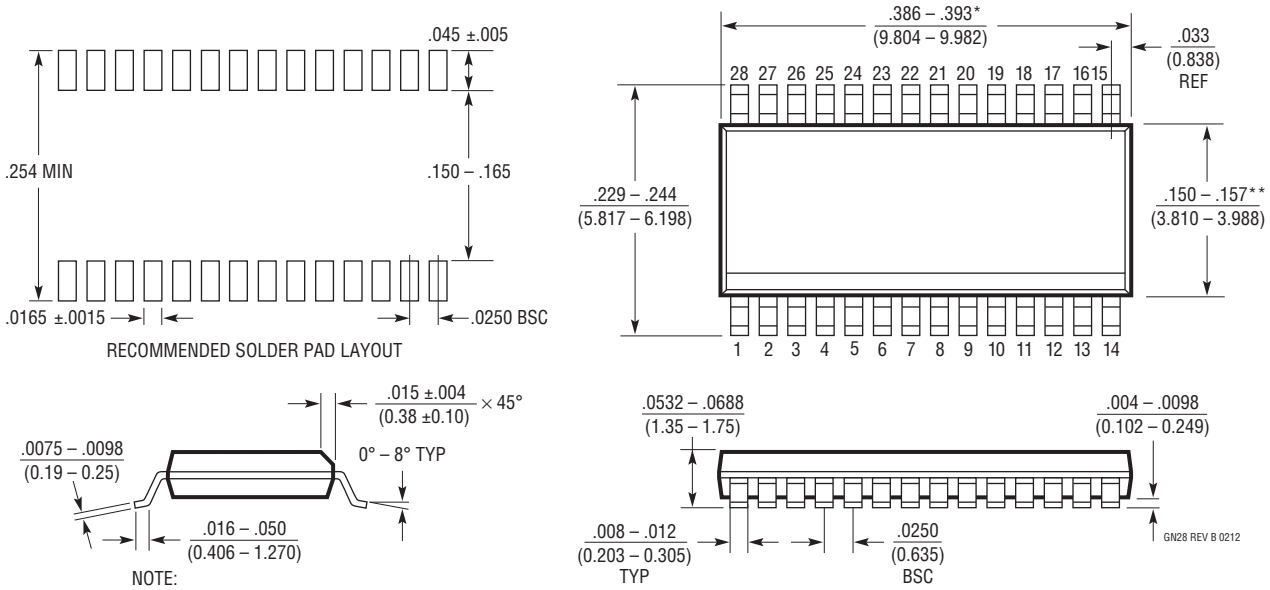


$T\,(°C) = 38.05 \bullet (V_{ADIN}\,(V) - 0.1458),\ 20°C < T < 60°C$

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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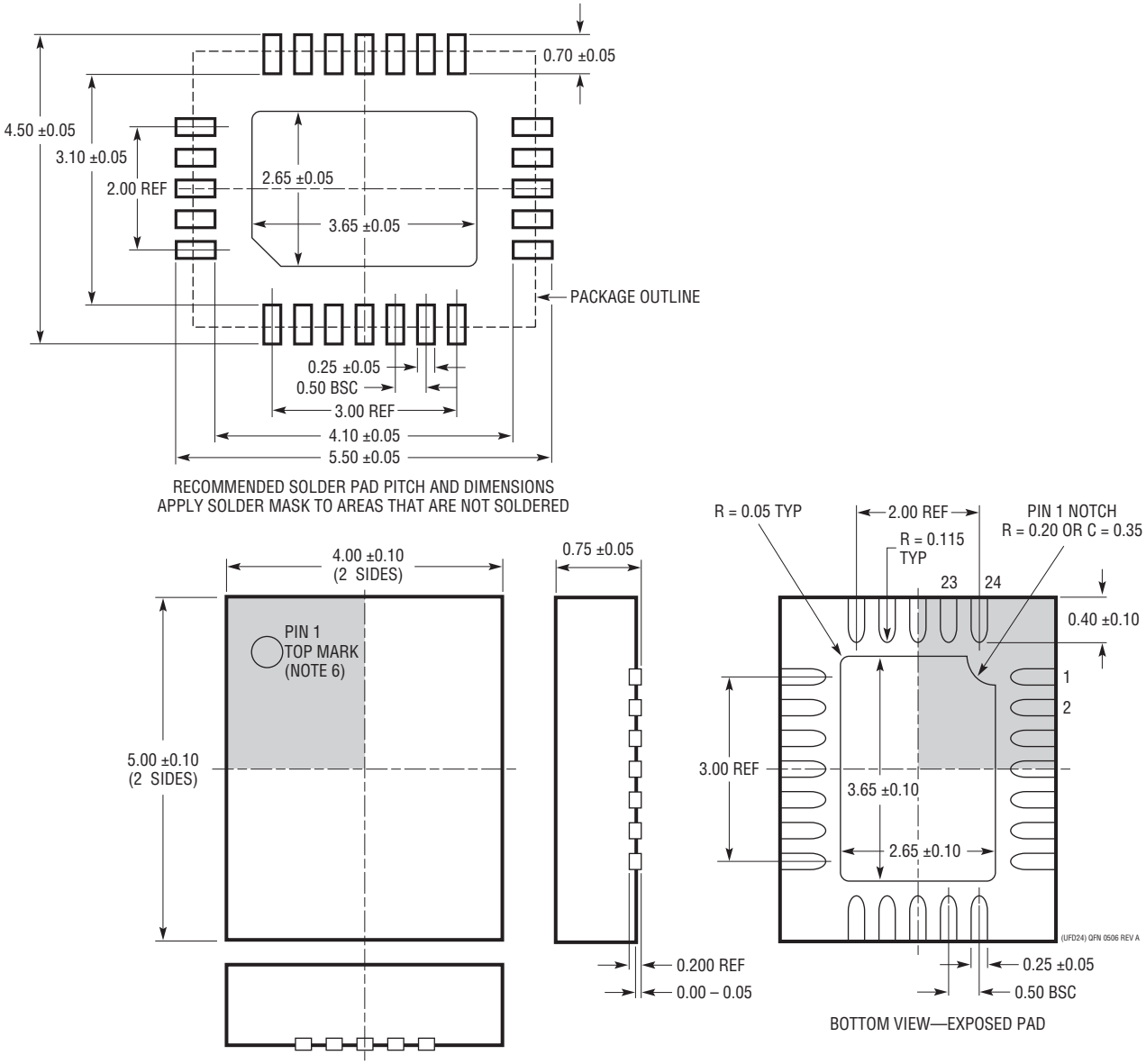
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	9/11	Change to Electrical Characteristics Gate Turn-Off Current	3
		Update to Typical Performance Characteristics graph G06	6
		Update to Pin Functions SDAI (Pin 5/Pin 2) description	9
		Update to Block Diagram	11
		Text changes to Operations section	12
		Added Figure 3	14
		Update to Figure 4	16
		Text changes to Applications Information	14, 17, 18, 22, 24
		Update to Typical Applications Figure 17	34
D	6/14	Separated V_{EE} connection of LTC4261 and related components from –48V input plane in circuit figures	1, 13, 20, 22, 27, 31, 34
		Added patent numbers	1
		Changed delay conditions to GATE Open from C_{GATE} = 1pF	3
		Layout Considerations section: Added paragraph and Figure 10 on separating local V_{EE} plane from -48V input plane	23, 24

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TYPICAL APPLICATIONS

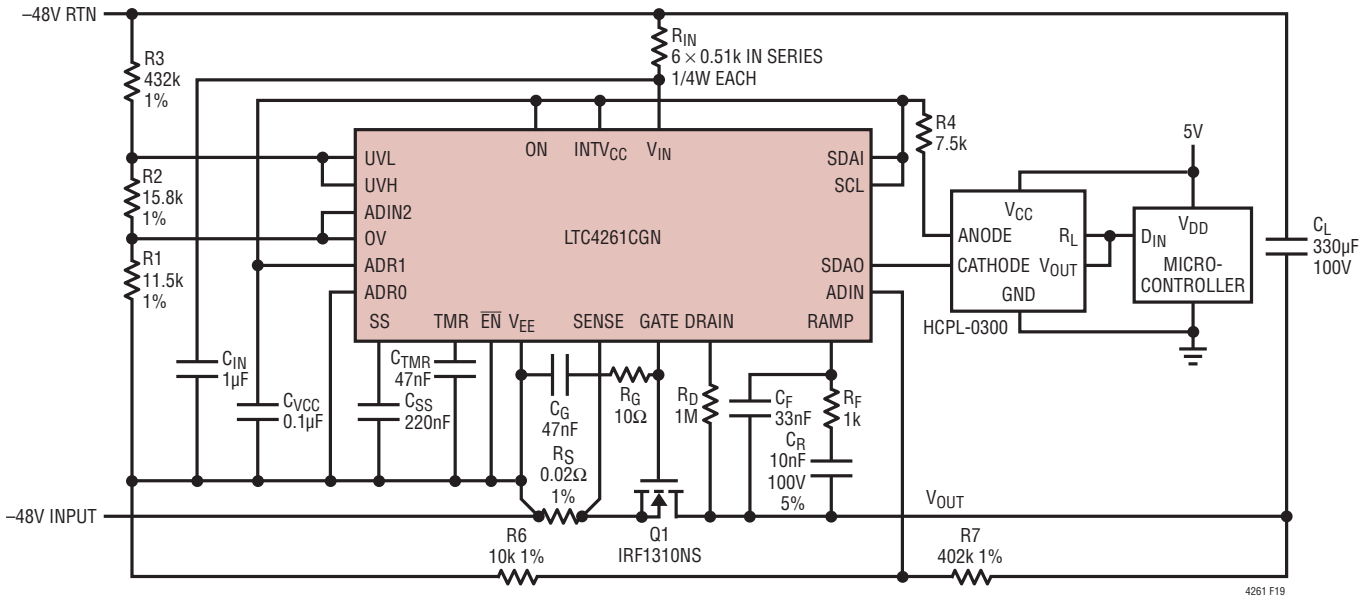

Figure 19. Application Circuit of the LTC4261 in Single-Wire Broadcast Mode

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1640AH/LT1640AL	Negative High Voltage Hot Swap Controllers in SO-8	Negative High Voltage Supplies from –10V to –80V
LTC1921	Dual –48V Supply and Fuse Monitor	UV/OV Monitor, –10V to –80V Operation, MSOP Package
LT4250L/LT4250H	–48V Hot Swap Controllers in SO-8	Active Current Limiting, Supplies from –18V to –80V
LTC4251/LTC4251-1	–48V Hot Swap Controllers in SOT-23	Fast Active Current Limiting, Supplies from –15V
LTC4252-1/LTC4252-2 LTC4252A-1/LTC4252A-2	–48V Hot Swap Controllers in MS8	Fast Active Current Limiting, Supplies from –15V, ±1% UV/OV (LTC4252A)
LTC4253	–48V Hot Swap Controller with Sequencer	Fast Current Limiting with Three Sequenced Power Good Outputs, Supplies from –15V
LTC4260	Positive High Voltage Hot Swap Controller	With I^2C and ADC, Supplies from 8.5V to 80V
LTC4354	Negative Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 1.2µs Turn-Off, 80V Operation

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC4261
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