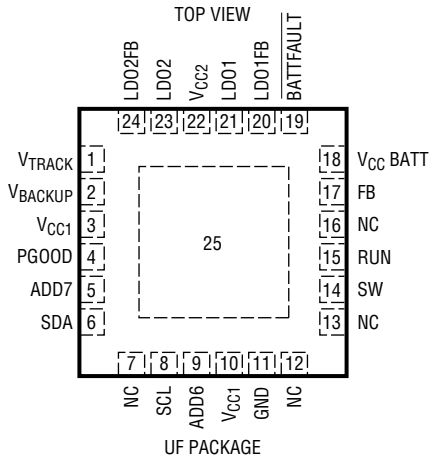
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC1}, V_{CC2}, SDA, SCL Voltages ..... –0.3V to 6V
RUN, V_{TRACK}, V_{BACKUP}, PGOOD, ADD7,
ADD6, FB, V_{CC} BATT,
BATTFAULT Voltages ..... –0.3V to V_{CC1}
SW Voltage ..... –0.3V to (V_{CC1} + 0.3V)
LDO1FB, LDO2FB Voltages ..... –0.3V to V_{CC2}
LDO1, LDO2 Voltages ..... –0.3V to (V_{CC2} + 0.3V)
LDO1, LDO2 Source Current 50mA
V_{CC} BATT Source Current 8mA
P-Channel Switch Source Current (DC) 800mA
N-Channel Switch Sink Current (DC) 800mA
Peak SW Sink and Source Current 1.3A
LDO1, LDO2, V_{CC} BATT Output Short-Circuit
Duration ..... Indefinite
Operating Temperature Range (Note 2) ...–40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 2.6°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	UF PART MARKING
LTC3445EUF	3445

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = V_{CC2} = 3.6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC1}, V_{CC2}	Input Voltage Range		●	2.5		5.5	V
RUN	Run Threshold		●	0.3	1	1.5	V
PGOOD	Reports Undervoltage of any Regulator	PGOOD = 0.4V	●	3			mA
I_S	DC Bias Current (Shutdown)	RUN = 0			27	50	µA
	DC Bias Current (Buck, LDO1, LDO2 Disabled)	RUN = V_{CC1}			105	150	µA
Buck Regulator							
R_{FB}	Feedback Resistance				340		kΩ
$V_{OUT(MIN)}$	Regulated Output Voltage	I_{OUT} = 100mA, Burst Mode Operation Disabled	●	0.824	0.850	0.875	V
$V_{OUT(MAX)}$	Regulated Output Voltage	I_{OUT} = 100mA, Burst Mode Operation Disabled	●	1.504	1.55	1.597	V
$V_{OUT(STEP)}$	Output Voltage Step Size (0 to 48)	I_{OUT} = 100mA	●	13.1	14.7	16.1	mV
	Output Voltage Slew Rate = 00	I_{OUT} = 100mA, V_{OUT} = 0.85V to 1.55V			11.3		mV/µs
	Output Voltage Slew Rate = 01	I_{OUT} = 100mA, V_{OUT} = 0.85V to 1.55V			7.5		mV/µs
	Output Voltage Slew Rate = 10	I_{OUT} = 100mA, V_{OUT} = 0.85V to 1.55V			3.8		mV/µs
	Output Voltage Slew Rate = 11	I_{OUT} = 100mA, V_{OUT} = 0.85V to 1.55V			0.9		mV/µs
I_{PK}	Peak Inductor Current	V_{CC1} = 3V, V_{FB} = 0.5V or V_{OUT} = 90%, Duty Cycle < 35%		0.75	1	1.25	A
$V_{LOADREG}$	Output Voltage Load Regulation				0.5		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = V_{CC2} = 3.6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Additional Input DC Bias Current For Buck Active Mode Sleep Mode	(Note 4) V_{OUT} = 90%, I_{LOAD} = 0A V_{OUT} = 103%, I_{LOAD} = 0A			 220 6		 µA µA
f_{OSC}	Nominal Oscillator Frequency	V_{OUT} = 100% V_{OUT} = 0V	● 	1.2	1.5 300	1.8	MHz kHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA			0.45		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = –100mA			0.325		Ω
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{CC1} = 5V			1		µA
LDO1							
I_S	Additional DC Bias for LDO1				23	30	µA
V_{OUT}	Regulated Output Voltage	2.5V < V_{IN} < 5.5V, 1mA < I_{LOAD} < 50mA		0.582		V_{CC2} – 0.3	V
	Line Regulation	ΔV_{CC2} = 2.5V to 5.5V, I_{LOAD} = 1mA, V_{OUT} = 1.2V			1	5	mV
	Load Regulation	V_{CC2} = 2.5V, ΔI_{LOAD} = 1mA to 50mA, V_{OUT} = 1.2V				15	mV
	Dropout Voltage	I_{LOAD} = 50mA			0.3		V
V_{FB}	LDO Feedback Voltage	I_{LOAD} = 0mA	●	0.582	0.6	0.618	V
LDO2							
I_S	Additional DC Bias for LDO2				23	30	µA
V_{OUT}	Regulated Output Voltage	2.5V < V_{IN} < 5.5V, 1mA < I_{LOAD} < 50mA		0.582		V_{CC2} – 0.3	V
	Line Regulation	ΔV_{CC2} = 2.5V to 5.5V, I_{LOAD} = 1mA, V_{OUT} = 1.2V			1	5	mV
	Load Regulation	V_{CC2} = 2.5V, ΔI_{LOAD} = 1mA to 50mA, V_{OUT} = 1.2V				15	mV
	Dropout Voltage	I_{LOAD} = 50mA			0.3		V
V_{FB}	LDO Feedback Voltage	I_{LOAD} = 0mA	●	0.582	0.6	0.618	V
PowerPath Controller							
V_{TRACK}	Tracked Input Voltage			3		V_{CC1} – 0.2	V
V_{TRACK} – V_{CC} BATT	Tracked Output Voltage at V_{CC} BATT	3V < V_{TRACK} < V_{CC1} – 0.2V		–0.2	0	0.2	V
V_{BACKUP}	Backup Battery Voltage			2		5.5	V
I_{BACKUP}	Backup Battery Bias Current	V_{CC1} = V_{TRACK} = 0V, V_{BACKUP} = 2.5V			4	6.5	µA
V_{CC} BATT	V_{CC} BATT Output	V_{TRACK} = 0V, V_{CC1} = 4V, I_{VCCBAT} = 8mA		2.85	3	3.1	V
$I_{VCCBATT}$	Max V_{CC} BATT Output Current	V_{CC1} = 2.5V			8		mA
$\overline{BATTFAULT}$	V_{CC1} High Level (Good)	Where $\overline{BATTFAULT}$ Goes High		2.65	2.8	2.9	V
	V_{CC1} Low Level (Bad)	Where $\overline{BATTFAULT}$ Goes Low		2.4	2.5	2.6	V
	Hysteresis	V_{CC1} = 0V to 4.2V, 4.2 to 0V			0.3		V
I²C Interface							
$f_{I2C(MAX)}$	Maximum I²C Operating Frequency	(Note 5)				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 5)				1.3	µs
$t_{HD(RSTA)}$	Hold Time After (Repeated) Start Condition	(Note 5)				600	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = V_{CC2} = 3.6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{SU(RSTA)}$	Repeated Start Condition Setup Time	(Note 5)				600	ns
$t_{SU(STOP)}$	Stop Condition Setup Time	(Note 5)				600	ns
$t_{HD(DIN)}$	Data Hold Time, Input	(Note 5)				0	ns
$t_{SU(DAT)}$	Data Setup Time	(Note 5)				100	ns
V_{THR}	SCL and SDA Logic Input Threshold				1.8		V
V_{HYS}	SCL and SDA Logic Input Hysteresis	(Note 5)			50		mV
$I_{LVTRACK}$	V_{TRACK} Leakage	V_{CC} = 3.6V			1.44	2.2	µA
$I_{LVBACKUP}$	V_{BACKUP} Leakage	V_{CC} = 3.6V	●			1	µA
I_{LADD7}	ADD7 Leakage	V_{CC} = 3.6V	●			1	µA
I_{LADD6}	ADD6 Leakage	V_{CC} = 3.6V	●			1	µA
I_{LSCL}	SCL Leakage	V_{CC} = 3.6V	●			1	µA
I_{LSDA}	SCL Leakage	V_{CC} = 3.6V	●			1	µA
I_{LLDO1}	LDO1 Leakage	V_{CC} = 3.6V, RUN = 0	●			1	µA
I_{LLDO2}	LDO2 Leakage	V_{CC} = 3.6V, RUN = 0	●			1	µA
$I_{LLDO1FB}$	LDO1FB Leakage	V_{CC} = 3.6V, RUN = 0	●			1	µA
$I_{LLDO2FB}$	LDO2FB Leakage	V_{CC} = 3.6V, RUN = 0	●			1	µA
$I_{L\overline{BATTFAULT}}$	$\overline{BATTFAULT}$ Leakage	V_{CC} = 3.6V	●			1	µA
$I_{FB1,2}$	LDO Feedback Input Current	V_{FB1} = 0.6V	●			1	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3445EUF is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

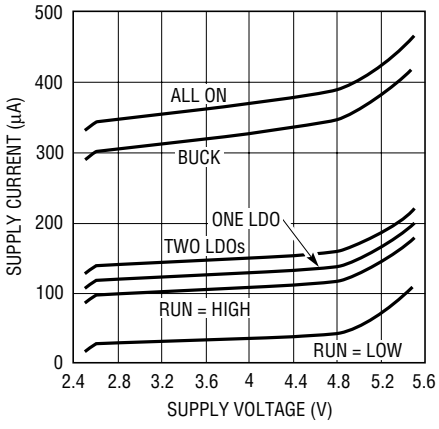
$T_J = T_A + P_D \bullet 37°C/W$

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

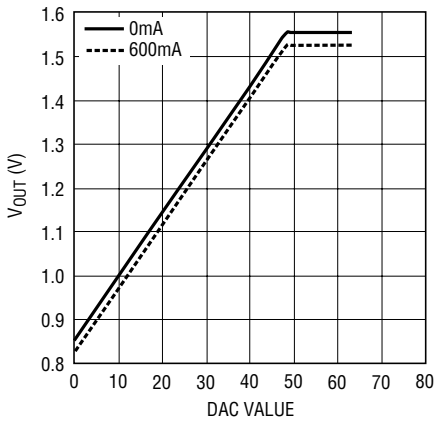
Note 5: Determined by design, not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

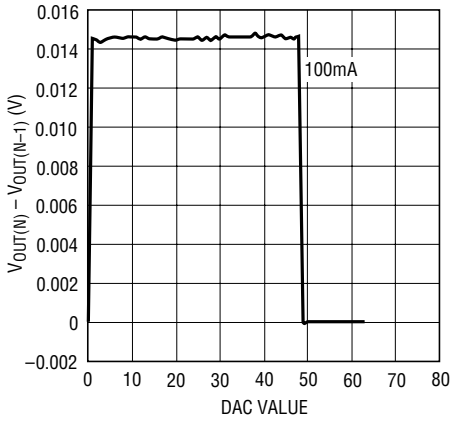
Supply Current vs Supply Voltage



V_{OUT} vs DAC

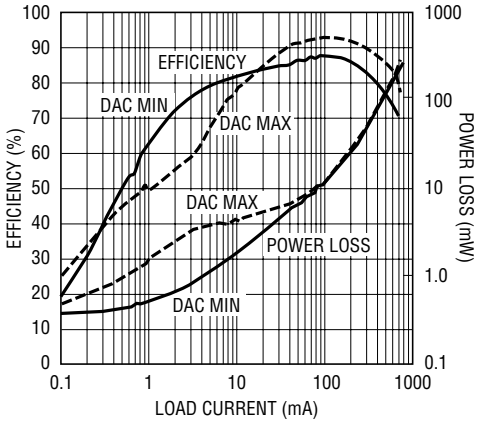


V_{OUT} Step Size vs DAC

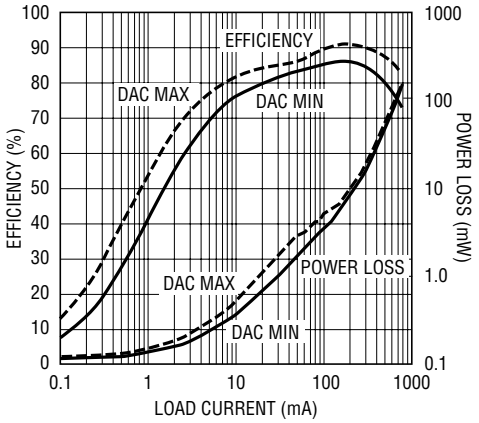


TYPICAL PERFORMANCE CHARACTERISTICS

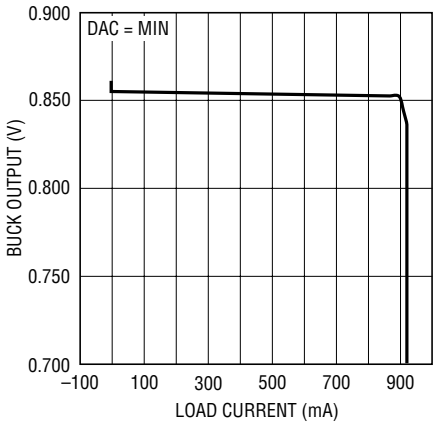
Buck Efficiency and Power Loss vs Load Current, V_{CC1} = 2.5V



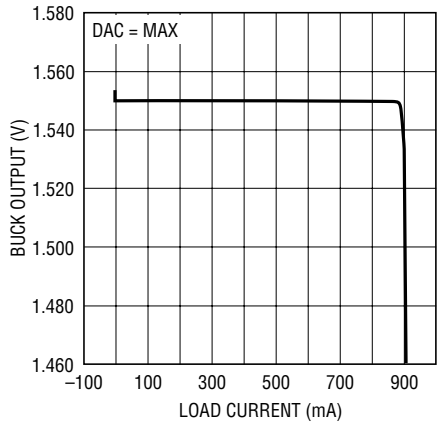
Buck Efficiency and Power Loss vs Load Current, V_{CC1} = 4.2V



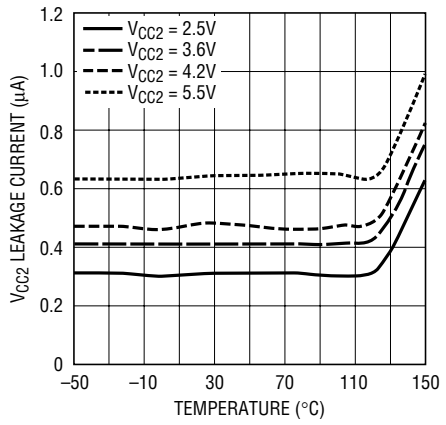
Buck Output Voltage vs Load Current



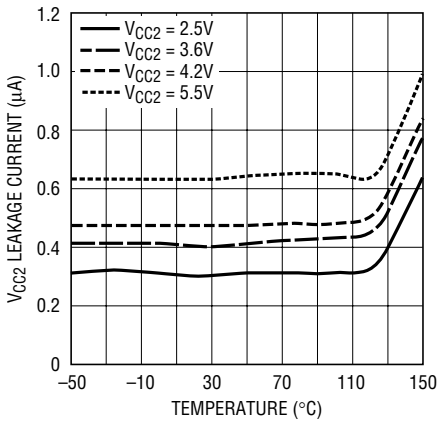
Buck Output Voltage vs Load Current



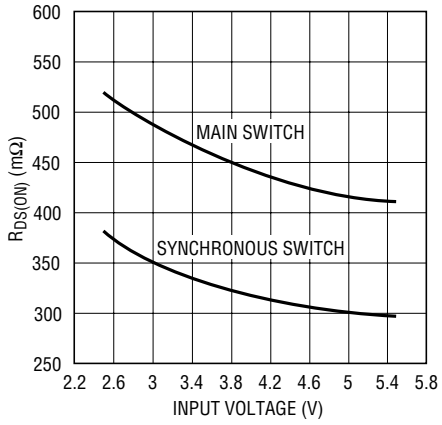
I_{VCC2} vs Temperature (RUN = V_{CC1})



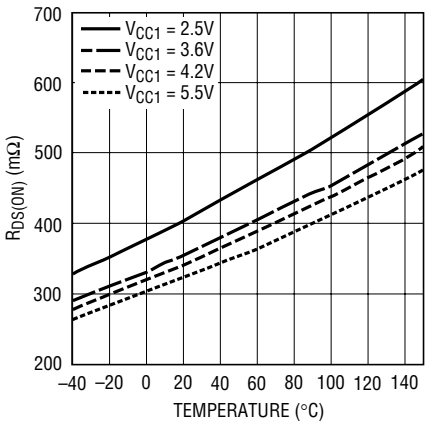
I_{VCC2} vs Temperature (RUN = 0V)



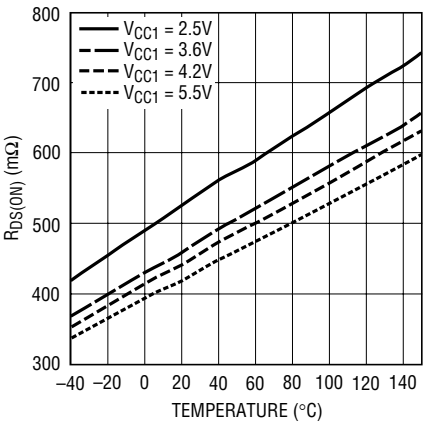
$R_{DS(ON)}$ vs Input Voltage



Synchronous Switch $R_{DS(ON)}$ vs Temperature

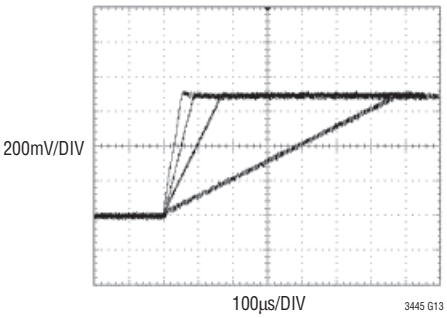


Main Switch $R_{DS(ON)}$ vs Temperature

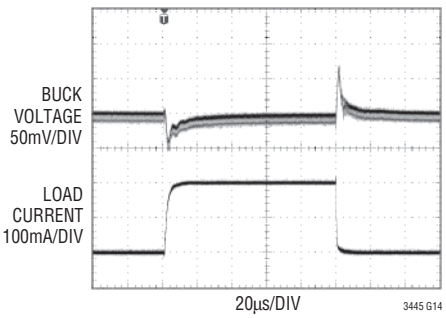


TYPICAL PERFORMANCE CHARACTERISTICS

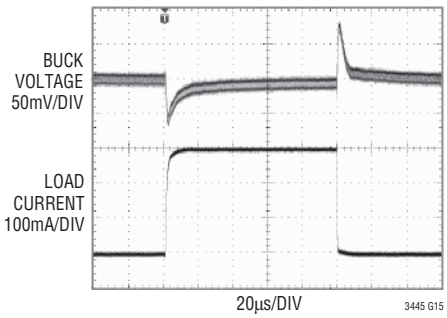
Slew Rates DAC Min to DAC Max



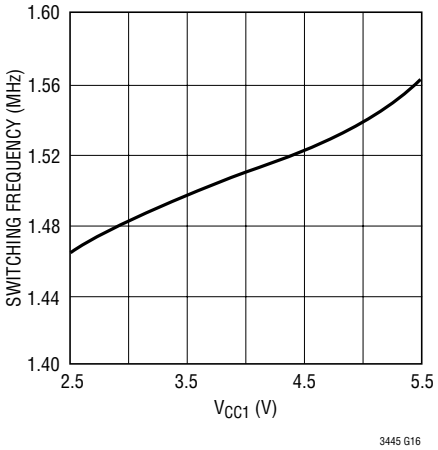
Buck (DAC = Min) 100mA to 300mA Load Step



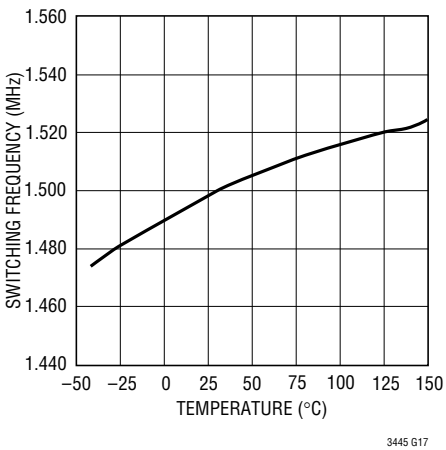
Buck (DAC = Max) 100mA to 400mA Load Step



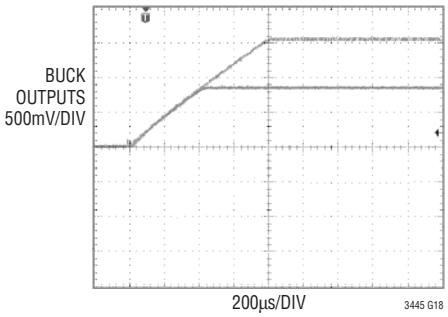
Buck Switching Frequency vs V_{CC1}



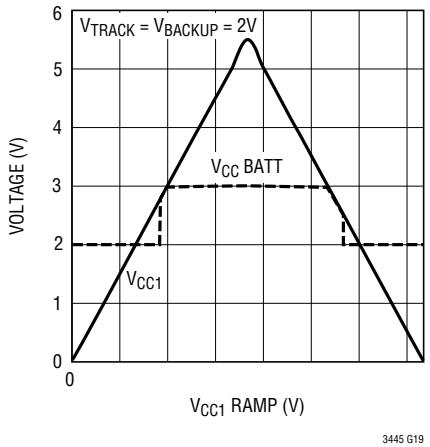
Buck Switching Frequency vs Temperature



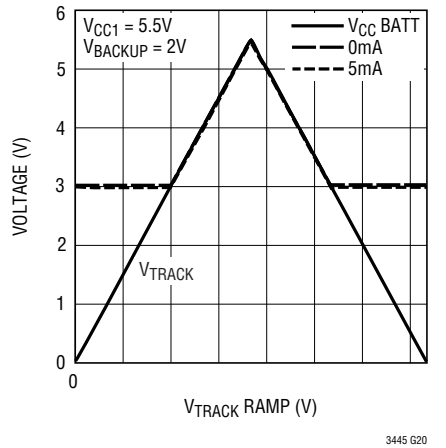
Soft-Start (DAC = Min and Max) 4.7Ω Load



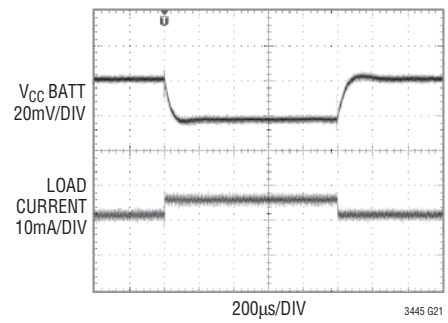
V_{CC} BATT vs V_{CC1}



V_{CC} BATT vs V_{TRACK}

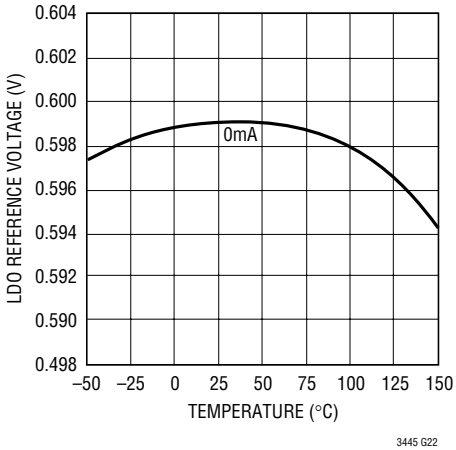


PowerPath LDO Load Step 1mA to 5.5mA

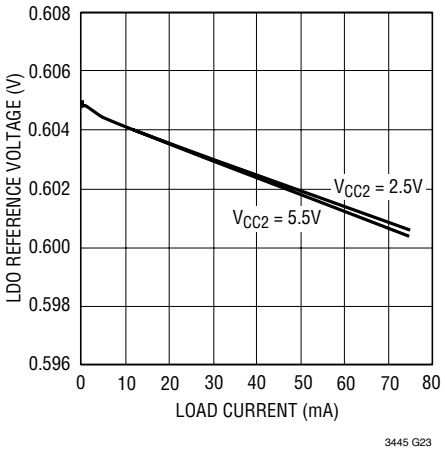


TYPICAL PERFORMANCE CHARACTERISTICS

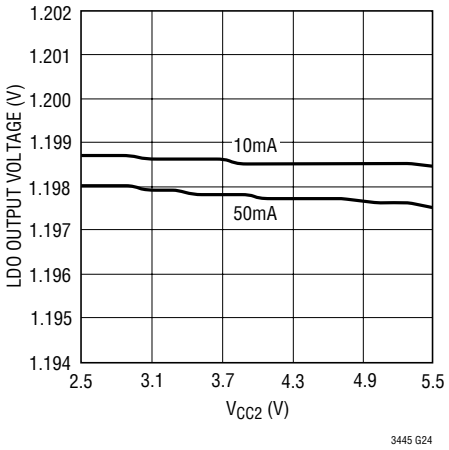
LDO Reference Voltage vs Temperature



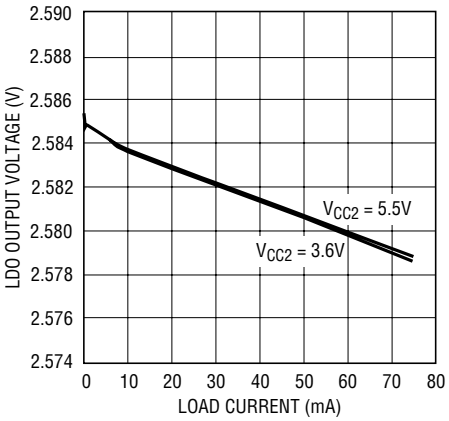
LDO Reference Voltage vs Load Current



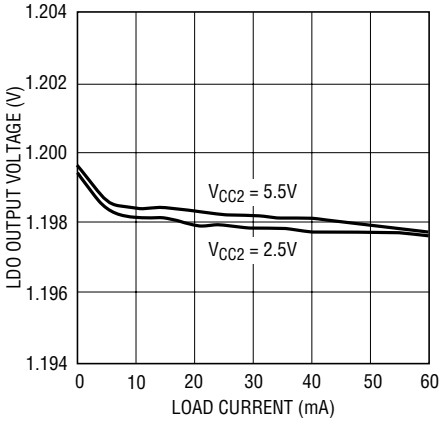
LDO Output Voltage vs V_{CC2}



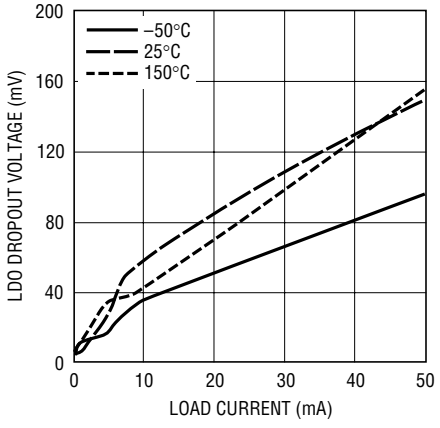
LDO Output Voltage vs Load Current



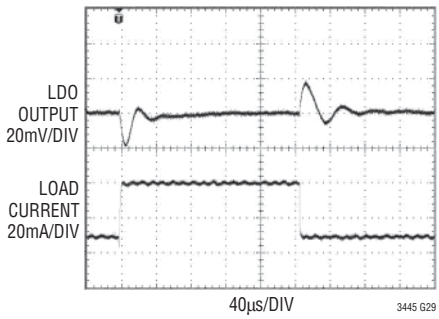
LDO Output Voltage vs Load Current



LDO Dropout Voltage vs Load Current



LDO Load Step (10mA to 40mA)



PIN FUNCTIONS

V_{TRACK} (Pin 1): Supply Sense that V_{CC} BATT Tracks when above 3V. Must be ≤ V_{CC1}.

V_{BACKUP} (Pin 2): Back-Up Battery Input.

V_{CC1} (Pins 3, 10): Power Supply (2.5V to 5.5V). Both V_{CC1} pins must be connected externally to the 2.5V to 5.5V supply.

PGOOD (Pin 4): Fault Report (Undervoltage). Open-drain driver sinks current whenever LDO1, LDO2 or buck outputs are low.

ADD7 (Pin 5): I^2C Strappable Address (Bit 7)—V_{CC1} or ground.

SDA (Pin 6): I^2C Data Input.

NC (Pin 7): Not Connected.

SCL (Pin 8): I^2C Clock Input.

ADD6 (Pin 9): I^2C Strappable Address (Bit 6)—V_{CC1} or ground.

GND (Pin 11): Buck NFET Ground.

NC (Pin 12): Not Connected.

NC (Pin 13): Not Connected.

SW (Pin 14): Buck Regulator Switch.

RUN (Pin 15): Chip Enable. 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. In shutdown, all functions are disabled, drawing <35µA supply current. Do not leave RUN floating. Must be ≤ V_{CC1}.

NC (Pin 16): Not Connected.

FB (Pin 17): Buck Regulator Feedback.

V_{CC} BATT (Pin 18): V_{CC} BATT PowerPath Output.

$\overline{\text{BATTFAULT}}$ (Pin 19): Open-Drain Output. It is low when V_{CC1} is low.

LDO1FB (Pin 20): LDO1 Regulator Sense.

LDO1 (Pin 21): LDO1 Regulator Output.

V_{CC2} (Pin 22): LDO Regulator Supply Voltage.

LDO2 (Pin 23): LDO2 Regulator Output.

LDO2FB (Pin 24): LDO2 Regulator Sense.

Exposed Pad (Pin 25): Ground. Must be soldered to PCB ground for electrical contact and optimum thermal performance.

FUNCTIONAL DIAGRAMS

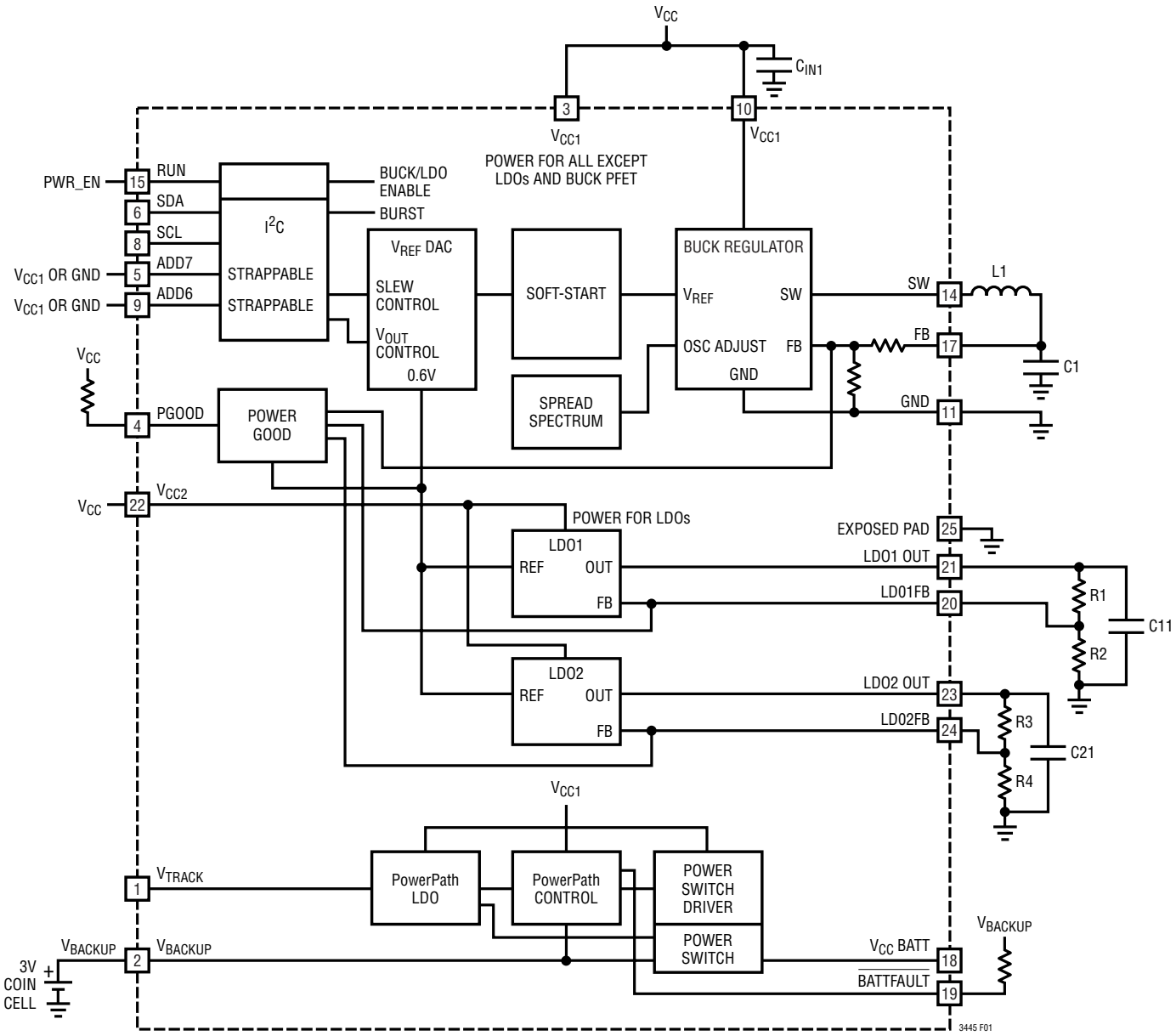


Figure 1

FUNCTIONAL DIAGRAMS

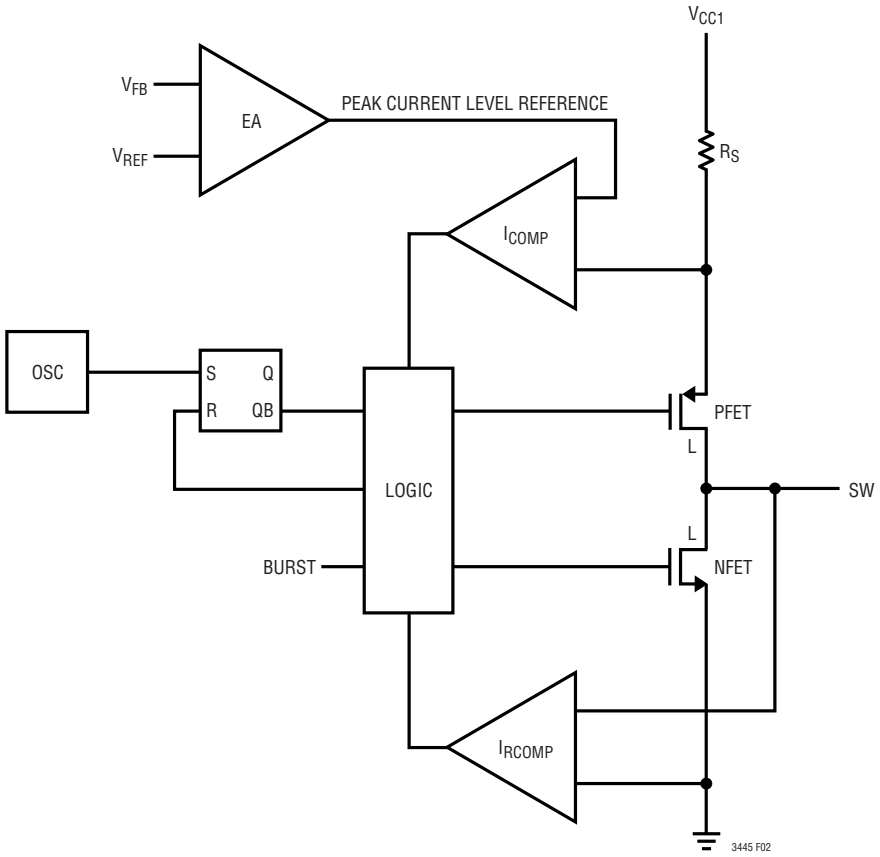
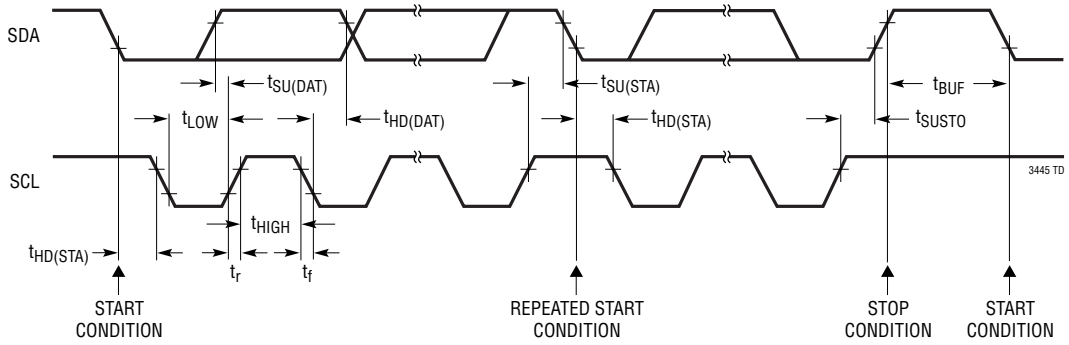


Figure 2. Buck Regulator Detail

TIMING DIAGRAM



I²C Fast Mode Timing Specifications (for Reference)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$f_{I2C(MAX)}$	Maximum I²C Operating Frequency	0		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	1.3			µs
$t_{HD(RSTA)}$	Hold Time After (Repeated) Start Condition	0.6			µs
$t_{SU(RSTA)}$	Repeated Start Condition Setup Time	0.6			µs
$t_{SU(STOP)}$	Stop Condition Setup Time	0.6			µs
$t_{HD(DAT)}$	Data Hold Time	0		0.9	ns
$t_{SU(DAT)}$	Data Setup Time	100			ns
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	0.6			µs
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter	0		50	ns
t_f	Clock, Data Fall Time (Note 1)	20 + 0.1 • C_B		300	ns
tr	Clock, Data Rise Time (Note 1)	20 + 0.1 • C_B		300	ns

Note 1: C_B = Capacitance of one bus line.

OPERATION (refer to Figure 1)

BUCK REGULATOR

Main Control Loop

The LTC3445 uses a constant or spread spectrum frequency, current mode step-down architecture (Figure 2). Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch is controlled by the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage, FB, relative to an internal reference voltage, which in turn, causes the EA's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle.

OPERATION (refer to Figure 1)

Burst Mode Operation

The LTC3445 is capable of Burst Mode operation, in which the internal power MOSFETs operate intermittently based on load demand.

In Burst Mode operation, the peak current of the inductor is set to approximately 200mA regardless of the output load. Each burst event can last from a few cycles at light loads to almost continuous cycling with short sleep intervals at moderate loads. In between these burst events, the power MOSFETs and any nonessential circuitry are turned off, reducing the buck regulator's quiescent current to 6µA. In this sleep state, the load current is being supplied solely from the output capacitor. As the output voltage droops, the EA's output rises above the sleep threshold, signaling the BURST comparator to trip and turn the top MOSFET on. This process repeats at a rate that is dependent on the load demand.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 300kHz. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing current runaway. The oscillator's frequency will progressively increase to 1.5MHz when V_{OUT} rises above 0V.

Low Supply Operation

The LTC3445 will operate with input supply voltages as low as 2.5V, but the maximum allowable output current is reduced at this low voltage. Figure 3 shows the reduction in the typical maximum output current as a function of input voltage for various output voltages.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%. However, the LTC3445 uses a patent-pending scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

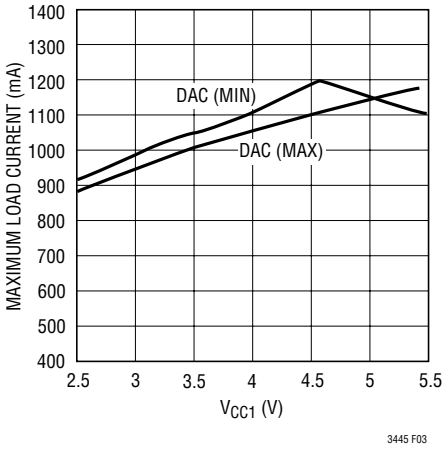


Figure 3. Buck Maximum Peak Current vs V_{CC1}

Spread Spectrum

The LTC3445 has a spread spectrum mode that can be enabled via two register bits. In the spread spectrum mode, the switching frequency is dithered about a center frequency of 1.5MHz. Spread spectrum lowers noise at the regulated output and at the input.

Figure 4 shows the noise reduction capabilities of the LTC3445 in spread spectrum mode. The percent spread of the frequency is controlled by two bits in register 5.

00 = 0% Spread
01 = 7.4% Spread
10 = 14.8% Spread
11 = 22.4% Spread

DAC

The buck output voltage is controlled by programming a 6-bit DAC register (REG0[5:0]) and GO bit (REG2[0]). The output voltage range is 0.85V to 1.55V in ~15mV steps. The DAC setting range is from 0 to 48. Any settings above 48 will default to the 48 settings value. When the desired DAC setting is loaded, the GO bit needs to be changed from 0 to 1. Once the GO bit transition occurs, V_{OUT} will begin to change to the DAC setting loaded at that instant.

Slew Rate

A 2-bit register is used to control the rate of change of V_{OUT} between DAC settings. The slew rate is controlled by stepping V_{OUT} to its new setting using a series of

OPERATION (refer to Figure 1)

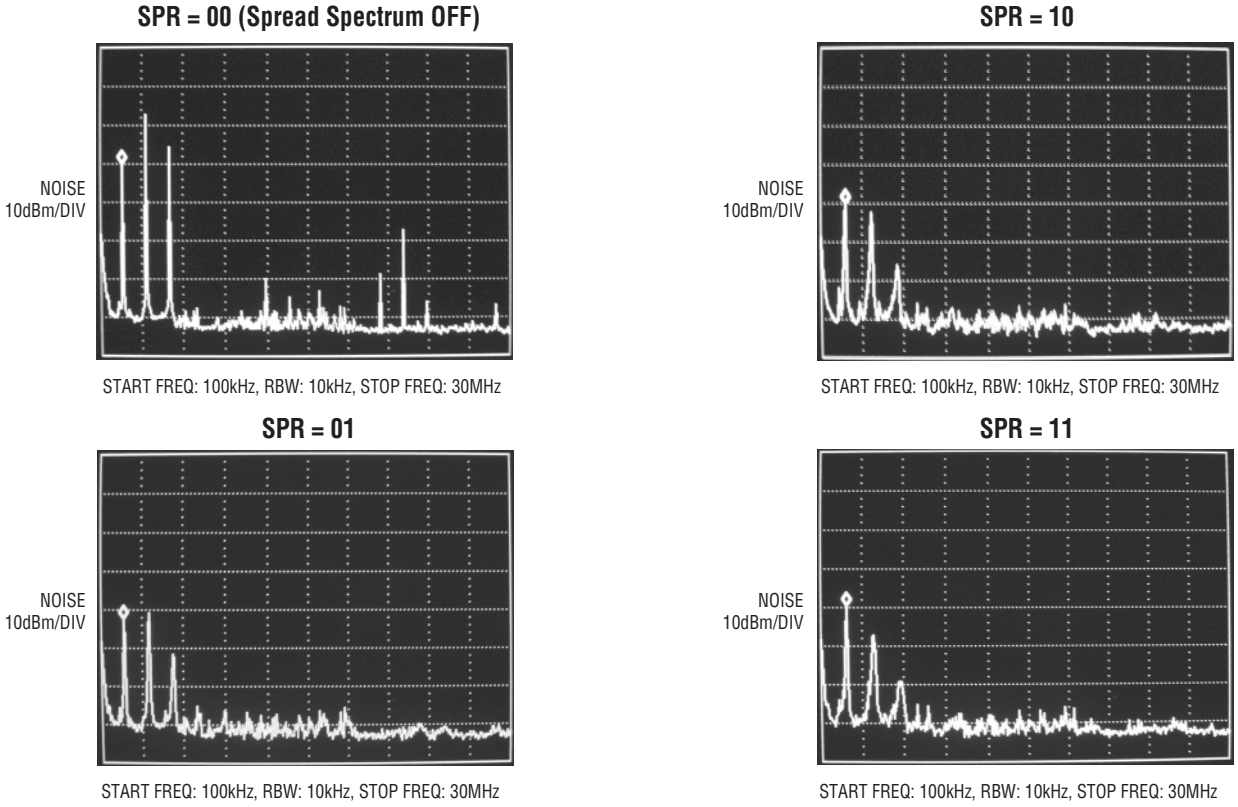


Figure 4. LTC3445 Output Noise Spectrum

micro-steps. The table below shows the register settings and corresponding slew rates.

REG1 [1:0]	SLEW RATE (mV/µs)
00	11.3
01	7.5
10	3.8
11	0.9

It should be noted that during DAC transistions, PGOOD fault reporting is disabled.

LDO OPERATION

Adjustable Operation

The LTC3445 contains two 50mA LDOs with an output voltage range of 0.6V to (V_{CC2} – 0.3V). The output voltage is set by the ratio of two external resistors as shown in Figure 1. Each LDO servos the output voltage (Pin LDOx) in order to maintain a feedback voltage (Pin LDOxFB) of 0.6V. The current in R1 and R2 is then equal to 0.6V/R2. The regulated voltage is equal to:

$$V_{OUT} = (0.6V/R2) \bullet (R1+R2)$$

Frequency Compensation

The LT3445 is frequency compensated by an internal dominant pole. An output capacitor of 2µF to 10µF is usually large enough to provide good stability. In order to insure stability, a feedforward capacitor may be needed between the output pin and the feedback pin. This cancels the pole formed by the stray capacitance in large value feedback resistors. Also, a feedback capacitor minimizes noise pickup and improves ripple rejection.

PowerPath OPERATION

The output of the PowerPath (V_{CC} BATT) is controlled by a combination of three inputs: main battery (V_{CC1}), V_{TRACK}, and V_{BACKUP}.

OPERATION (refer to Figure 1)

When V_{CC1} rises above 2.8V, the PowerPath's LDO is enabled and set to the lesser of 3V or V_{CC1}. Once V_{TRACK} is 3V or higher, it controls the PowerPath's LDO output (V_{CC} BATT) voltage to within 200mV of V_{TRACK}. Note that V_{TRACK} needs to be less than or equal to V_{CC1}. When V_{TRACK} falls below 3V, V_{CC1} is used to regulate the PowerPath's LDO (V_{CC} BATT) to 3V. When V_{CC1} falls below 2.4V, the PowerPath LDO is disconnected and V_{BACKUP} is connected to V_{CC} BATT.

The PowerPath's fault detection circuit uses an open-drain driver ($\overline{\text{BATTFAULT}}$) to report when the main battery is disconnected.

Figure 5 shows the different states of the PowerPath circuits. Typically, V_{BACKUP} is a coin cell; however, other types of back up power supplies may be used.

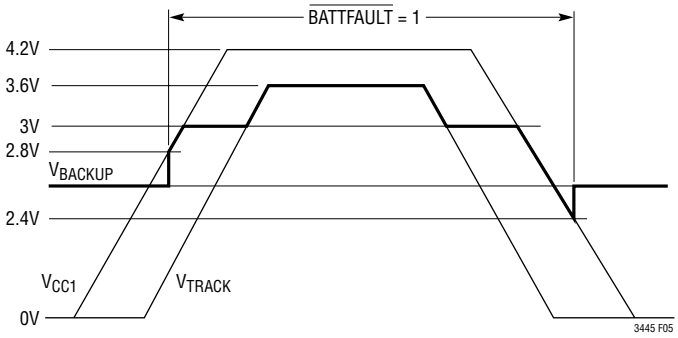


Figure 5

I²C OPERATION

- Simple 2-wire interface
- Multiple devices on same bus
- Idle bus must have SDA and SCL lines high
- LTC3445 is read/write
- Master controls bus
- Devices listen for unique address that precedes data

General I²C Bus/SMBus Description

I²C Bus and SMBus are reasonably similar examples of 2-wire, bidirectional, serial communications busses. Calling them 2-wire is not strictly accurate, as there is an implied third wire, which is the ground line. Large ground drops or spikes between the grounds of different parts on the bus can interrupt or disrupt communications, as the signals on the two wires are both inherently referenced to a ground which is expected to be common to all parts on the bus. Both bus types have one data line and one clock line which are externally pulled to a high voltage when they are not being controlled by a device on the bus. The devices on the bus can only pull the data and clock lines low, which makes it simple to detect if more than one device is trying to control the bus; eventually, a device will release a line and it will not pull high because another device is still holding it low. Pull-ups for the data and clock lines are usually provided by external discrete resistors, but external current sources can also be used. Since there are no dedicated lines to use to tell a given device if another device is trying to communicate with it, each device must have a unique address to which it will respond. The first part of any communication is to send out an address on the bus and wait to see if another device responds to it. After a response is detected, meaningful data can be exchanged between the parts.

Typically, one device will control the clock line at least most of the time and will normally be sending data to the other parts and polling them to send data back to it, and this device is called the master. There can certainly be more than one master, since there is an effective protocol to resolve bus contentions, and non-master (slave) devices can also control the clock to delay rising edges and give themselves more time to complete calculations or communications (clock stretching). Slave devices need to

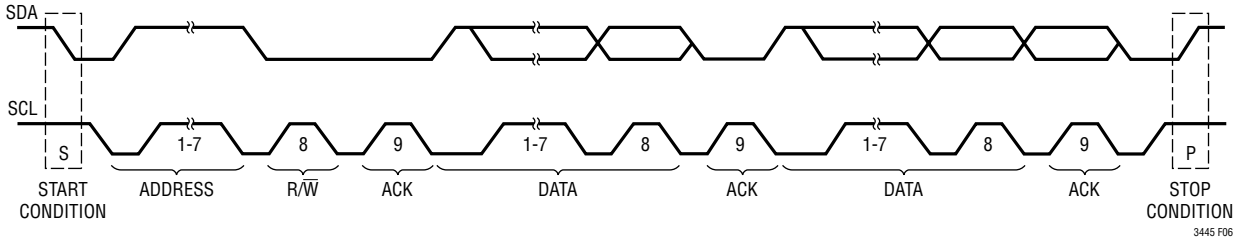


Figure 6. Typical 2-Wire Serial I²C Waveforms

OPERATION (refer to Figure 1)

be able to control the data line to acknowledge communications from the master, and some devices will need to able to send data back to the master; they will be in control of the data line while they are doing so. Many slave devices will have no need to stretch the clock signal and will have no ability to pull the clock line low, which is the case with the LTC3445.

Data is exchanged in the form of bytes, which are 8-bit packets. Any byte needs to be acknowledged by the slave (data line pulled low) or not acknowledged by the master (data line left high), so communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging. For example, sending out an address consists of 7 bits of device address, 1 bit that signals whether a read or write operation will be performed, and then 1 more bit to allow the slave to acknowledge. There is no theoretical limit to how many total bytes can be exchanged in a given transmission.

I^2C and SMBus are very similar specifications, SMBus having been derived from I^2C. In general, SMBus is targeted to low power devices (particularly battery-powered ones) and emphasizes low power consumption, while I^2C is targeted to higher speed systems where the power consumption of the bus is not so critical. I^2C has three different specifications for three different maximum speeds, these being standard mode (100kHz max), fast mode (400kHz max) and HS mode (3.4MHz max). Standard and fast mode are not radically different, but HS mode is very different from a hardware and software perspective and requires an initiating command at standard or fast speed before data can start transferring at HS speed. SMBus simply specifies a 100kHz maximum speed.

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. An acknowledge signal (LOW active) as generated by the slave lets the master know that the latest byte of information was received. The acknowledge-related clock pulse is generated by the master. The transmitter master releases the SDA line (HIGH) during the acknowledge clock pulse. The slave receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

When a slave receiver doesn't acknowledge the slave address (for example, it's unable to receive because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition. The

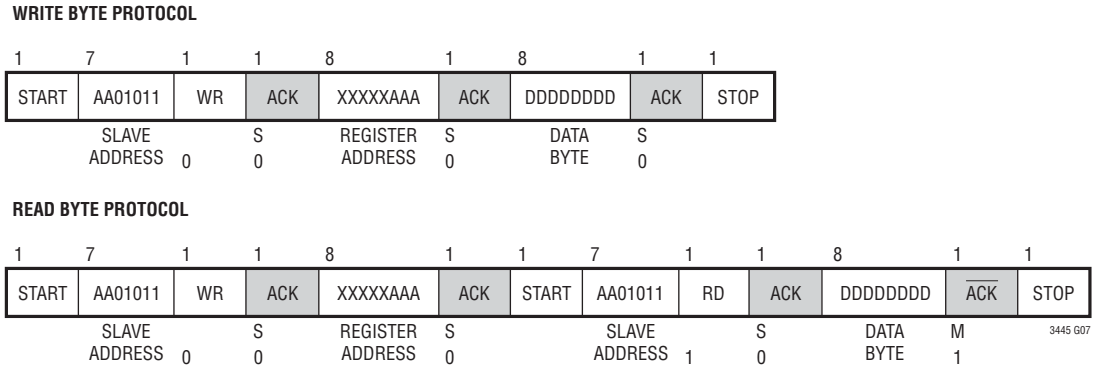


Figure 7

OPERATION (refer to Figure 1)

data line is also left high by the slave and master after a slave has transmitted a byte of data to the master in a read operation, but this is a not-acknowledge that indicates that the data transfer is successful.

1^2C Register Definitions
(POR = 00 for all registers)

REG 0

7	0 (Logic Low)
6	0 (Logic Low)
5	Buck DAC5
4	Buck DAC4
3	Buck DAC3
2	Buck DAC2
1	Buck DAC1
0	Buck DAC0

REG 1

7	0 (Logic Low)
6	0 (Logic Low)
5	0 (Logic Low)
4	0 (Logic Low)
3	0 (Logic Low)
2	0 (Logic Low)
1	Slew Rate 1
0	Slew Rate 0

REG 2

7	0 (Logic Low)
6	0 (Logic Low)
5	0 (Logic Low)
4	STATUS—Buck Thermal Shutdown
3	STATUS—Buck PGOODb
2	STATUS—LDO2 PGOODb
1	STATUS—LDO1 PGOODb
0	Buck Update (GO Bit)

REG 3

7	PGOOD Blank Disable
6	0 (Logic Low)
5	0 (Logic Low)
4	0 (Logic Low)
3	BURST Mode
2	LDO2 Disable
1	LDO1 Disable
0	Buck Disable

REG 5

7	0 (Logic Low)
6	% SPR1
5	% SPR0
4	(Logic Low)
3	(Logic Low)
2	(Logic Low)
1	(Logic Low)
0	(Logic Low)

Commands Supported

The LTC3445 supports read byte and write byte commands. For the ACK bits, an S indicates that the slave is pulling the data line low and an M indicates that the master is effectively acknowledging by leaving the data line high.

Data Transfer Timing for Write Commands

In order to help assure that bad data is not written into the part, data from a write command is only stored after a valid acknowledge has been performed. The part will detect that SDA is low on the rising edge of SCL that marks the end of the period in which the LTC3445 acknowledges the data write and then latch the data during the following SCL low period.

APPLICATIONS INFORMATION

BUCK REGULATOR

The basic LTC3445 application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 4.7µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{CC1} or lower V_{OUT} also increases the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current is ΔI_L = 240mA (40% of 600mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{CC1}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated inductor should be enough for most applications (600mA + 120mA). For better efficiency, choose a low DC-resistance inductor.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 200mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3445 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3445 applications.

Table 1

MANUFACTURER PART NUMBER	VALUE (µH)	DCR (mΩ MAX)	MAX DC (A)	SIZE L × W × H (mm³)
Sumida CDRH3D16/HP2R2	2.2	72	1.2	4.0 × 4.0 × 1.8
Sumida CR434R7	4.7	109	1.15	4.0 × 4.5 × 3.5
TDK TDK7030T-2R2M5R4	2.2	12	5.5	7.3 × 6.8 × 3.2
Coilcraft D03316P-222	2.2	12	7	12.45 × 9.4 × 5.21

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{CC1}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{CC1}-V_{OUT})\right]^{1/2}}{V_{CC1}} \quad (2)$$

This formula has a maximum at $V_{CC1} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR+\frac{1}{8fC_{OUT}}\right) \quad (3)$$

APPLICATIONS INFORMATION

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3445's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{CC1}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{CC1}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Buck Output Voltage Programming

The LTC3445 has an internal resistor divider network tied to the FB pin. The output voltage is controlled by a DAC (6-bit register) whose setting is controlled by the I^2C interface. The effective DAC bit range is from 0 to 48. Note that any DAC settings above 48 defaults to the 48 setting. The DAC controls the V_{OUT} range of 0.85V to 1.55V in ~15mV steps. The default value for V_{OUT} is 1.35V and is reset to this value whenever V_{CC1} comes up.

When the DAC's value is changed, LTC3445 controls V_{OUT}'s slew rate via a 2-bit RATE register. The RATE register can be updated via the I^2C interface. The slew rate can be set to approximately 0.9mV/µs, 3.8mV/µs, 7.5mV/µs or 11.3mV/µs. The default value for RATE is 10mV/µs and is reset to this value whenever V_{CC1} comes up.

The DAC and RATE values are not lost whenever the RUN pin is deasserted.

Once the DAC and RATE registers are programmed, a GO bit transition is required for the buck to update. This is accomplished by changing the GO bit (REG2[0]) from logic low to a logic high.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3445 buck regulator circuits: V_{CC1} quiescent current and I^2R losses. The V_{CC1} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 8.

1. The V_{CC1} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the

APPLICATIONS INFORMATION

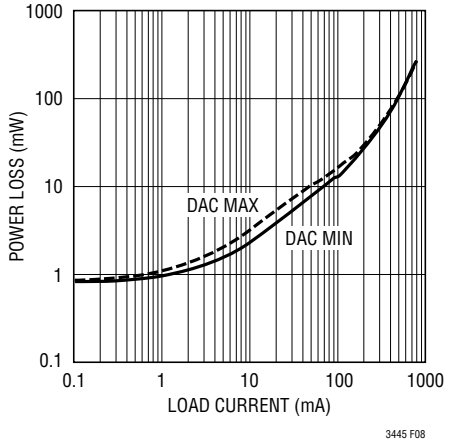


Figure 8. Power Loss vs Load Current, V_{CC1} = 3.6V

internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{CC1} to ground. The resulting dQ/dt is the current out of V_{CC1} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{CC1} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Charateristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal.

The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

LDO REGULATORS

The LDOs in the LTC3445 are 50mA low dropout regulators with low quiescent and shutdown currents. Each device is capable of supplying 50mA at a dropout voltage of 300mV. The LDOs are current limited to greater than 50mA but less than 75mA. The output voltages of the LDOs are set with external resistive dividers according to the following formula:

$$V_{LDOOUT1} = 0.6(1 + R1/R2) \quad (4)$$

$$V_{LDOOUT2} = 0.6(1 + R3/R4) \quad (5)$$

Output Capacitance and Transient Response

The LTC3445 LDOs are designed to be stable with a wide range of output capacitors. A minimum output capacitor of 2.2µF with an ESR of 3Ω or less is recommended to

APPLICATIONS INFORMATION

prevent oscillations. The LTC3445 LDOs are micropower devices and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes.

PowerPath CONTROLLER

The PowerPath circuitry in the LTC3445 is used to provide backup power from V_{BACKUP} to the V_{CC} BATT pin when V_{CC1} is low or disconnected. When V_{CC1} is below 2.8V, the PowerPath routes V_{BACKUP}, typically a coin cell, to the V_{CC} BATT pin. While V_{BACKUP} is selected there is no current limiting except for a small (<5Ω) resistance from the V_{BACKUP} input to the V_{CC} BATT output. The LTC3445 sinks less than 6.5µA from V_{BACKUP} when it is selected and sinks less than 0.1µA from V_{BACKUP} when it is not selected.

When V_{CC1} exceeds 2.8V, V_{BACKUP} is disconnected from V_{CC} BATT and an internal LDO regulates the V_{CC} BATT voltage to the minimum of V_{CC1} or typically 3V. The internal LDO is current limited to less than 50mA, but greater than 10mA. Capacitance on the V_{CC} BATT pin should be at least 2µF with an ESR less than 3Ω.

V_{BACKUP} will be routed to the V_{CC} BATT output when the main battery voltage falls below 2.4V. As the main battery, V_{CC1}, voltage drops from 3V to 2.4V, the LDO will be in dropout, V_{CC} BATT will follow V_{CC1} down, rebounding to V_{BACKUP} when V_{CC1} falls below 2.4V. If V_{CC1} is removed quickly, the capacitor on V_{CC} BATT will limit the V_{CC} BATT droop until V_{BACKUP} is switched in.

The V_{TRACK} input offers the capability of the V_{CC} BATT voltage to follow the voltage on V_{TRACK} up to V_{CC1}. In effect, V_{TRACK} overrides the internal reference of the LDO, resulting in the LDO output (V_{CC} BATT) having a gain of 1 relative to V_{TRACK} once V_{TRACK} exceeds a typical value of 3V. V_{CC} BATT will follow V_{TRACK} to within 200mV providing V_{TRACK} does not exceed the dropout voltage of the LDO, which is powered by V_{CC1}.

V_{BACKUP} should be present prior to V_{CC1} being connected. V_{BACKUP} provides power to the $\overline{\text{BATTFAULT}}$ driver which is used to detect an absent or low V_{CC1}. If V_{BACKUP} is not present, the LTC3445 will be unable to pull the $\overline{\text{BATTFAULT}}$ pin low to signal a V_{CC1} fault condition.

Output Capacitance and Transient Response

The LDO used LTC3445 PowerPath is designed to be stable with a wide range of output capacitors. A minimum output capacitor of 2.2µF with an ESR of 3Ω or less is recommended to prevent oscillations. The LTC3445 PowerPath LDO is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes.

THERMAL CONSIDERATIONS

In most applications the LTC3445 does not dissipate much heat due to its high efficiency. But, in applications where the LTC3445 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance. The remaining regulators will also turn off.

To ensure the LTC3445 doesn't exceed the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = \theta_{JA} \bullet (PD_{BUCK} + PD_{LDO1} + PD_{LDO2} + PD_{PowerPath})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

APPLICATIONS INFORMATION

As an example, consider the LTC3445 in dropout at an input voltage of 2.7V, an ambient temperature of 70°C, a buck load current of 600mA, LDO1 set to 1.3V with a load of 25mA, LDO2 set to 1.1V with a load of 15mA, and the PowerPath regulator at 2.5V with a load of 6µA. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 0.52Ω. Therefore, power dissipated by the part is:

$$P_{D(BUCK)} = I_{LOAD}^{2} \bullet R_{DS(ON)} = 180mW$$

$$P_{D(LDO1)} = (2.7 – 1.3)V \bullet 0.025A = 35mW$$

$$P_{D(LDO2)} = (2.7 – 1.1)V \bullet 0.015A = 24mW$$

$$P_{D(PowerPath)} = (2.7 – 2.5)V \bullet 6\mu A = 1.2\mu W$$

$$P_{D(TOTAL)} = 0.239W$$

For the QFN24 package, the θ_{JA} is 37°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 70°C + (0.239)(37) = 78.8°C$$

which is well below the maximum junction temperature of 125°C. Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

PC BOARD LAYOUT CHECKLIST

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3445. These items are also illustrated graphically in Figures 9 and 10. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace, the V_{CC1} trace and the V_{CC2} trace should be kept short, direct and wide.
2. Does the FB pin connect directly to the output voltage reference? Ensure that there is no load current running from the reference voltage and the FB pin.
3. Does the (+) plate of C_{IN1} connect to V_{CC1} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
4. Keep the switching node, SW, away from the sensitive FB node.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

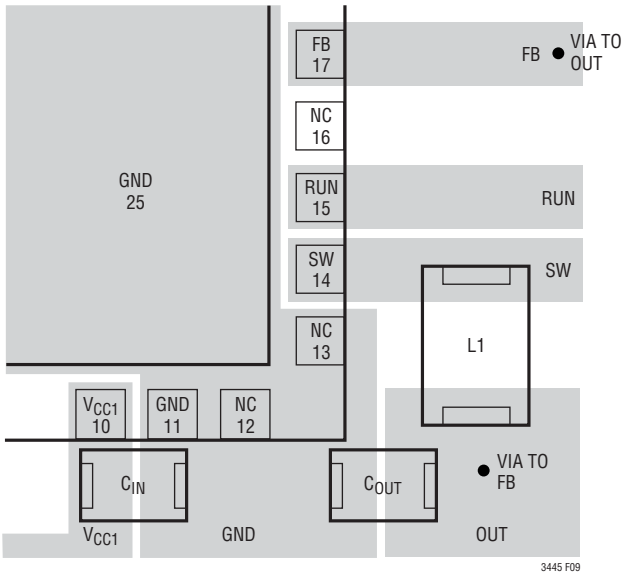


Figure 9

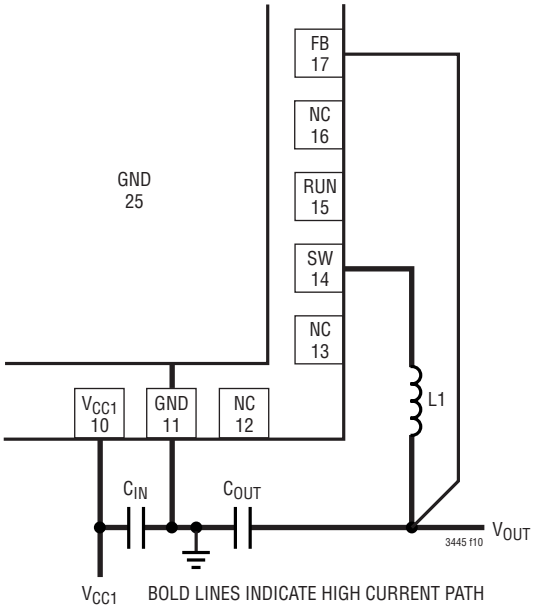


Figure 10

APPLICATIONS INFORMATION

DESIGN EXAMPLE

As a design example, assume the LTC3445 is used in a single lithium-ion battery-powered Intel PXA270 microprocessor application. The battery will be operating from a maximum of 4.2V down to about 2.7V. Also, the battery will be connected to all three power pins on the LTC3445.

The desired LDO outputs are 1.3V with a 23mA load and 1.1V with a 14mA load. Since both LDO's are the same, we will select LDO1 for the 1.3V output and LDO2 for the 1.1V output. Using Equations 4 and 5, and choosing R2 and R4 to be 604k, the values for R1 and R2 are 705k and 503k respectively. Also, selecting a 10µF output capacitor provides adequate stability and transient reponses.

The PXA270's V_{CC} BATT requirement can be readily handled by the LTC3445's PowerPath control circuits. By simply connecting a coin cell battery to V_{BACKUP}, the PowerPath control circuits regulate V_{CC} BATT within the PXA270's requirements.

The buck regulator's maximum load requirement for this application is 300mA. Although the default start-up voltage for the buck regulator is 1.35V, ripple current is greatest when the output voltage is programmed to 0.85V. For ripple currents of 200mA and the main battery at 4.2V, the required inductor value is 2.2µH (Equation 1). For best efficiency choose a 400mA or greater inductor with less than 0.3Ω series resistance. Choosing a 10µF output capacitor with an ESR of 0.25Ω will generate a ripple voltage of 52mV (Equation 3). In most cases, a ceramic capacitor's ESR will be less than 0.25Ω further reducing the output ripple (see Figure 11). Note that as V_{CC1} decreases or V_{OUT} increases, the ripple current and ripple voltage will decrease. The input capacitor, C_{IN}, will require an RMS current rating of at least 0.150A ≅ $I_{LOAD(MAX)}/2$ at temperature (Equation 2).

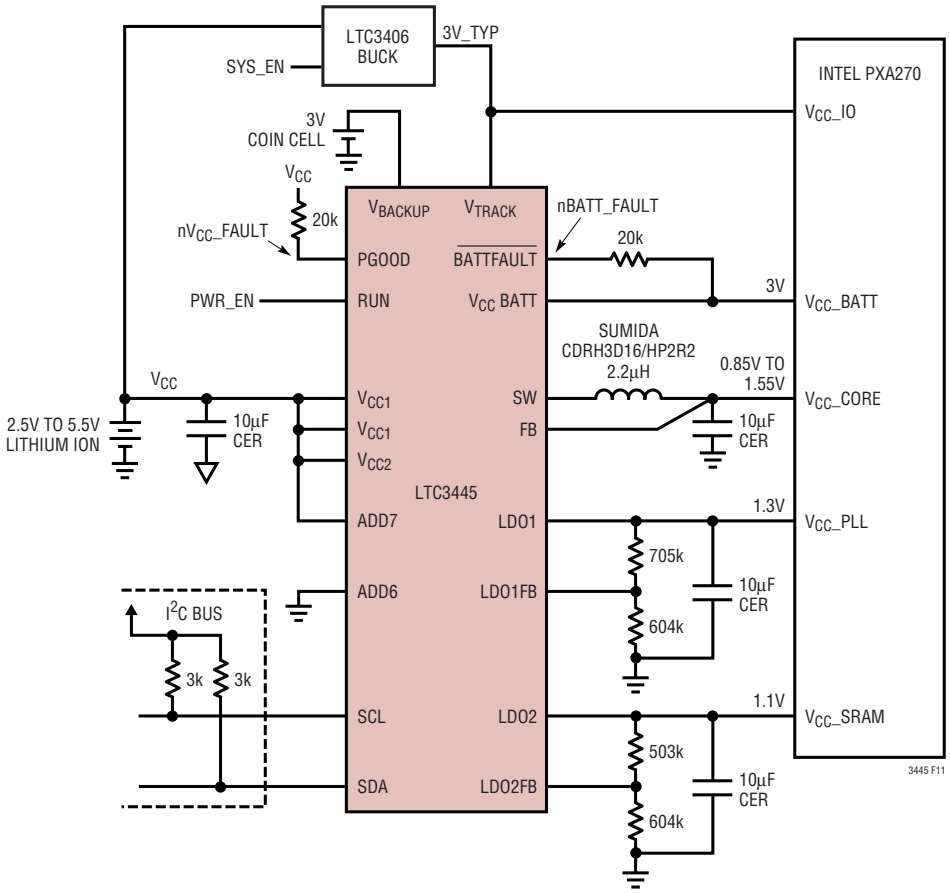
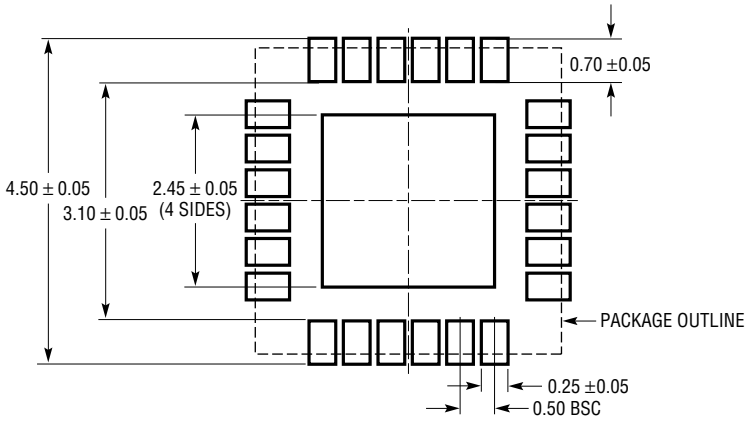


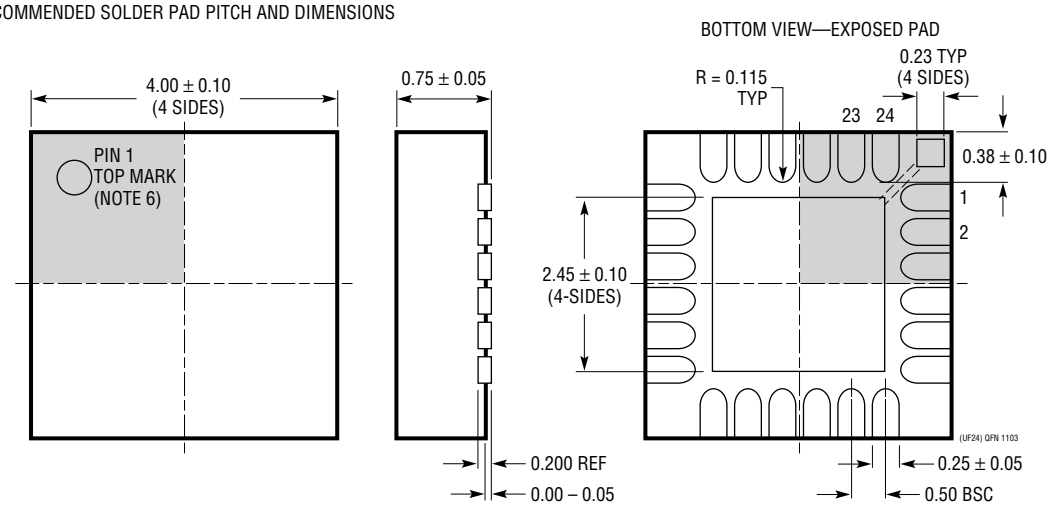
Figure 11. Design Example

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.30V, I_Q = 20µA, I_{SD} < 1µA, V_{OUT} = Adj, 1.5V, 1.8V, 2V, 2.5V, 2.8V, 3V, 3.3V, 5V, ThinSOT™ Package. Low Noise < 20µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors
LT1762	150mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.30V, I_Q = 25µA, I_{SD} < 1µA, V_{OUT} = Adj, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µ$V_{RMS(P-P)}$
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.30V, I_Q = 30µA, I_{SD} < 1µA, V_{OUT} = 1.5V, 1.8V, 2.5V, 3V, 3.3V, 5V, S8 Package. Low Noise < 20µ$V_{RMS(P-P)}$
LTC1844	150mA, Very Low Dropout LDO	V_{IN}: 6.5V to 1.6V, $V_{OUT(MIN)}$ = 1.25V, Dropout Voltage = 0.08V, I_Q = 40µA, I_{SD} < 1µA, V_{OUT} = Adj, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V, ThinSOT Package. Low Noise < 30µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, Dropout Voltage = 0.27V, I_Q = 30µA, I_{SD} < 1µA, V_{OUT} = 1.5V, 1.8V, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µ$V_{RMS(P-P)}$
LT3020	Low V_{IN} (0.9V) Low V_{OUT} (0.2V) VLDO™	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, Dropout Voltage = 0.15V, I_Q = 120µA, I_{SD} < 1µA, V_{OUT} = Adj, DFN Package
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407	Dual 600mA, 1.5MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E Package
LTC3411	1.25A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS10 Package
LTC3412	2.5A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP16E Package
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	V_{IN}: 3V to 5.5V, Seamless Transition Between Input Sources and Li-Ion Battery, USB, 5V Wall Adapter, QFN24 Package
LTC4055	USB Power Manager and Li-Ion Battery Charger	Standalone Charger, Automatic Switchover when Input Supply is Removed
LTC4411/LTC4412	PowerPath Controllers in ThinSOT	More Efficient than Diode ORing

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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