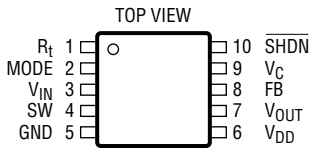
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT}, V_{DD} Voltages ..... –0.5V to 6V
SW Voltage ..... –0.5V to 6V
V_C, R_t Voltages ..... –0.5V to (V_{OUT} + 0.3V)
$\overline{SHDN}$, FB, MODE Voltages ..... –0.5V to 6V
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C
θ_{JA} = 130°C/W 1 LAYER BOARD
θ_{JA} = 100°C/W 4 LAYER BOARD

ORDER PART NUMBER
LTC3423EMS LTC3424EMS
MS PART MARKING
LTQM LTQN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{DD} = 3.3V, V_{OUT} = 1.8V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Input Voltage Range		●	2.7		5.5	V
V_{IN} Operating Voltage Range	(Note 4)	●	0.5		5.5	V
Output Voltage Adjust Range		●	1.5		5.5	V
Feedback Voltage		●	1.22	1.25	1.28	V
Feedback Input Current	V_{FB} = 1.25V			1	50	nA
Quiescent Current—Burst Mode Operation	V_C = 0V, MODE/SYNC = 3.3V (Note 3)			38	65	µA
Quiescent Current—$\overline{SHDN}$	$\overline{SHDN}$ = 0V, Not Including Switch Leakage			0.1	1	µA
Quiescent Current—Active	V_C = 0V, MODE/SYNC = 0V, R_t = 300k (Note 3)			440	800	µA
NMOS Switch Leakage				0.1	5	µA
PMOS Switch Leakage				0.1	10	µA
NMOS Switch On Resistance				0.16		Ω
PMOS Switch On Resistance				0.21		Ω
NMOS Current Limit	LTC3423 LTC3424	● ●	1 2	1.6 2.8		A A
Maximum Duty Cycle	R_t = 15k	●	80	85		%
Minimum Duty Cycle		●			0	%
Frequency Accuracy	R_t = 15k	●	1.6	2	2.4	MHz
MODE/SYNC Input High			1.4			V
MODE/SYNC Input Low					0.4	V
MODE/SYNC Input Current	$V_{MODE/SYNC}$ = 5.5V			0.01	1	µA
Error Amp Transconductance	ΔI = –5µA to 5µA, V_C = V_{FB}			85		µmhos

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{OUT} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Input High	$V_{\overline{SHDN}} = V_{IN} = V_{OUT}$		1			V
$\overline{SHDN}$ Input Low					0.4	V
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 5.5V			0.01	1	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

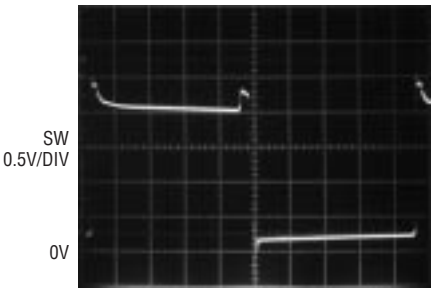
Note 2: The LTC3423/LTC3424 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current is measured into V_{DD} since the supply current is bootstrapped to the V_{DD} pin. The outputs are not switching.

Note 4: Once the output is started, the IC is not dependant upon the V_{IN} supply.

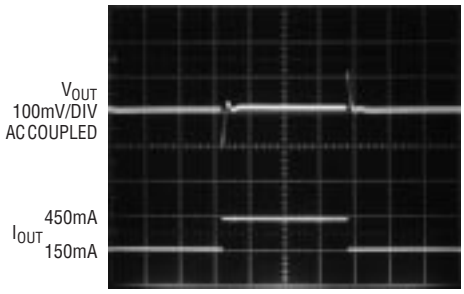
TYPICAL PERFORMANCE CHARACTERISTICS

Switching Waveform on SW Pin



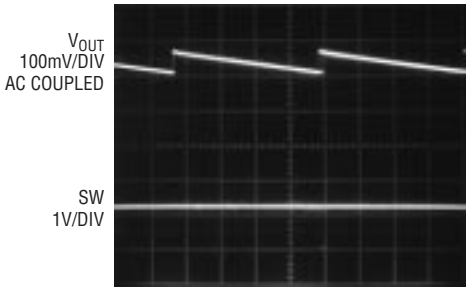
I_{LOAD} = 500mA 100ns/DIV 3423/24 G01
V_{OUT} 1.8V

Transient Response 150mA to 450mA



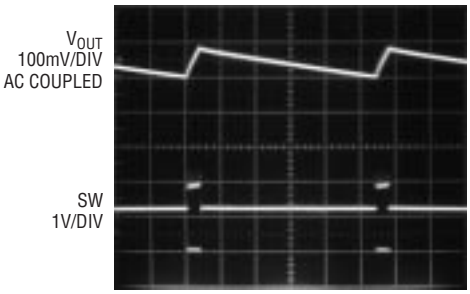
C_{OUT} = 44µF 200µs/DIV 3423/24 G02
L = 2.2µH
f_{OSC} = 1MHz

Burst Mode Operation at 500µA Load



V_{IN} = 1.2V 1ms/DIV 3423/24 G03
V_{OUT} = 1.8V
C_{OUT} = 44µF
MODE/SYNC PIN = HIGH

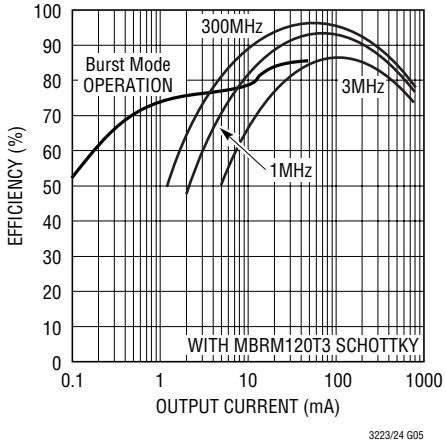
Burst Mode Operation at 10mA Load



V_{IN} = 1.2V 500µs/DIV 3423/24 G04
V_{OUT} = 1.8V
C_{OUT} = 44µF
MODE/SYNC PIN = HIGH

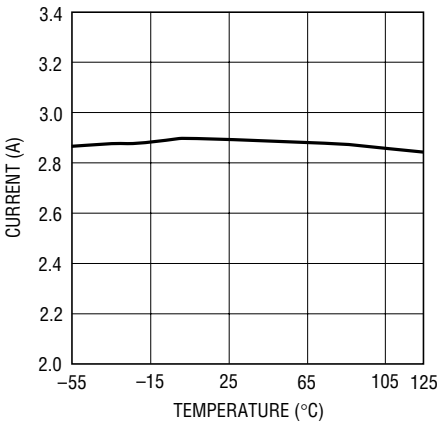
TYPICAL PERFORMANCE CHARACTERISTICS

Converter Efficiency 1.2V to 1.8V



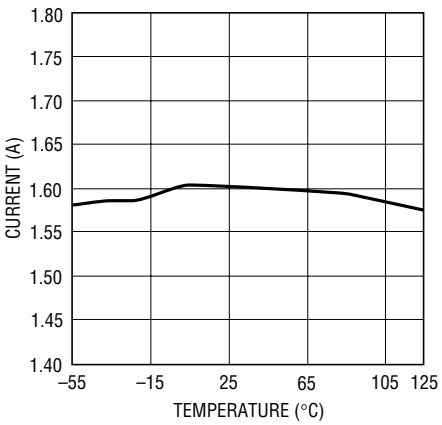
3223/24 G05

LTC3424 Current Limit



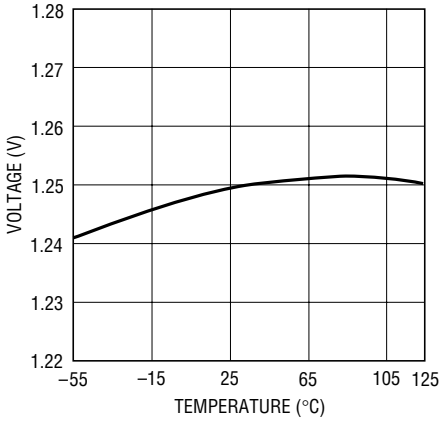
3423/24 G06

LTC3423 Current Limit



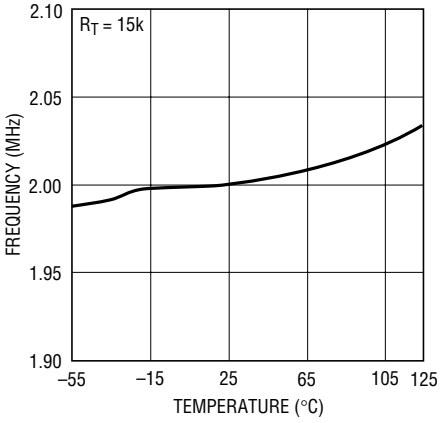
3423/24 G07

EA FB Voltage



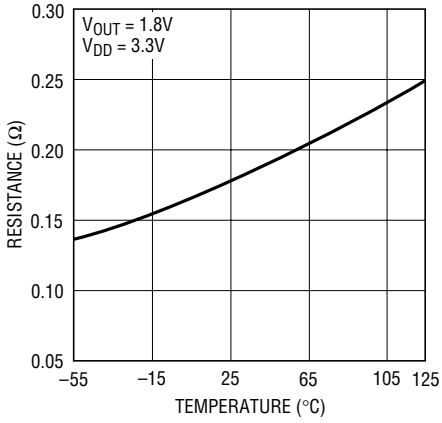
3423/24 G08

Oscillator Frequency Accuracy



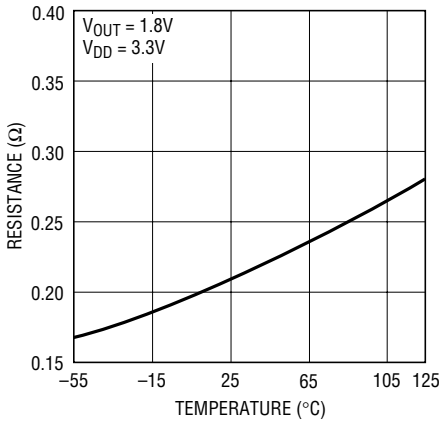
3423/24 G09

NMOS $R_{DS(ON)}$



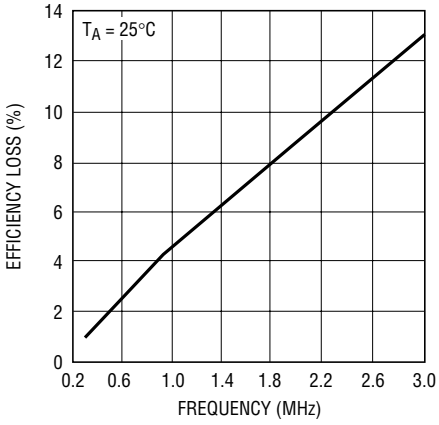
3423/24 G10

PMOS $R_{DS(ON)}$



3423/24 G11

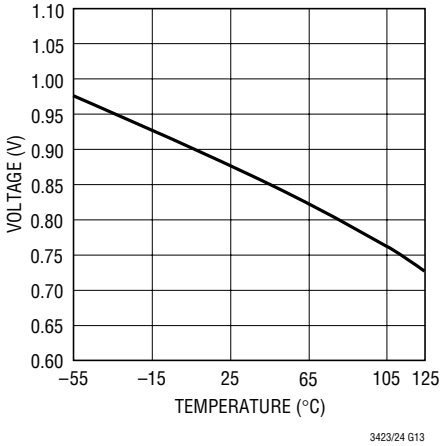
Efficiency Loss Without Schottky vs Frequency



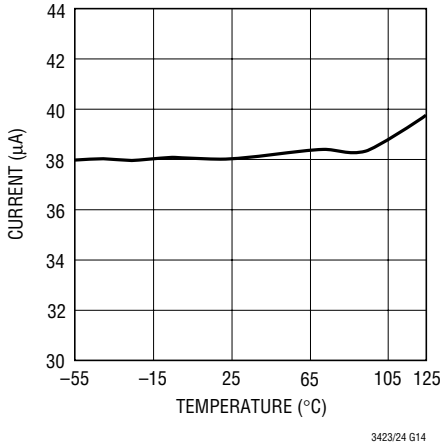
3423/24 G12

TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Threshold



Burst Mode Operation Current



PIN FUNCTIONS

R_t (Pin 1): Timing Resistor to Program the Oscillator Frequency.

$$f_{OSC} = \frac{3 \bullet 10^{10}}{R_t} \text{ Hz}$$

MODE/SYNC (Pin 2): Burst Mode Select and Oscillator Synchronization.

MODE/SYNC = High. Enable Burst Mode operation. The inductor peak inductor current will be 400mA and return to zero current on each cycle. During Burst Mode operation the operation is variable frequency, providing a significant efficiency improvement at light loads. It is recommended the Burst Mode operation only be entered once the part has started up.

MODE/SYNC = Low. Disable Burst Mode operation and maintain low noise, constant frequency operation.

MODE/SYNC = External CLK. Synchronization of the internal oscillator and Burst Mode operation disable. A clock pulse width of 100ns to 2µs is required to synchronize.

V_{IN} (Pin 3): Voltage Sense for Internal Circuitry.

SW (Pin 4): Switch Pin. Connect inductor and optional Schottky diode here. Minimize trace length to keep EMI down.

GND (Pin 5): Signal and Power Ground for the IC.

V_{DD} (Pin 6): Power Source for the IC. Typically derived from a higher voltage power converter. Requires an input of 2.7V to 5.5V. A 2.2µF ceramic bypass capacitor is recommended as close to the pins as possible.

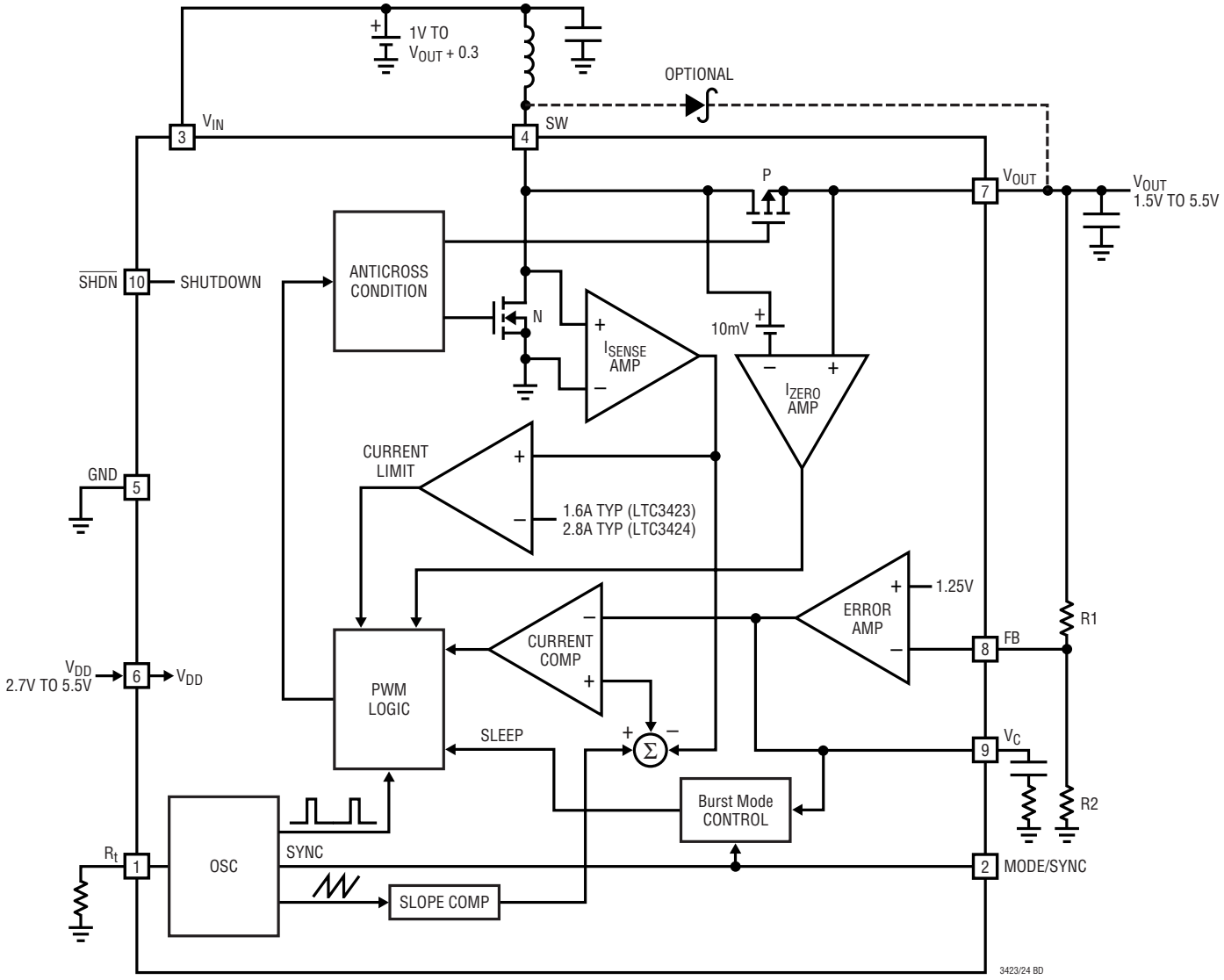
V_{OUT} (Pin 7): Output of the Synchronous Rectifier.

FB (Pin 8): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 1.5V to 5.5V. The feedback reference voltage is typically 1.25V.

V_C (Pin 9): Error Amp Output. A frequency compensation network is connected to this pin to compensate the loop. See the section "Compensating the Feedback Loop" for guidelines.

$\overline{SHDN}$ (Pin 10): Shutdown. Grounding this pin shuts down the IC. Tie to >1V to enable (V_{DD} or digital gate output). During shutdown the output voltage will hold up to V_{IN} minus a diode drop due to the body diode of the PMOS synchronous switch. If the application requires a complete disconnect during shutdown then refer to section "Output Disconnect".

BLOCK DIAGRAM



APPLICATIONS INFORMATION

DETAILED DESCRIPTION

The LTC3423/LTC3424 provides high efficiency, low noise power for applications such as portable instrumentation and are ideal for applications that require an output voltage between 1.5V and 2.6V from a single cell. These products are an addition to the LTC3401 and LTC3402 family of synchronous boost converters, with the differences being the omission of the power good function (PGOOD) and the addition of a V_{DD} input to provide internal power. The IC will not start up until the applied voltage on the V_{DD} pin is above 2.7V.

The current mode architecture with adaptive slope compensation provides ease of loop compensation with excellent transient load response. The low $R_{DS(ON)}$, low gate charge synchronous switches provides the pulse width modulation control at high efficiency.

Low Noise Fixed Frequency Operation

Oscillator. The frequency of operation is set through a resistor from the R_t pin to ground where $f = 3 \bullet 10^{10}/R_t$. An internally trimmed timing capacitor resides inside the IC. The oscillator can be synchronized with an external clock inserted on the MODE/SYNC pin. When synchronizing the oscillator, the free running frequency must be set to approximately 30% lower than the desired synchronized frequency. Keeping the sync pulse width below 2µs will ensure that Burst Mode operation is disabled.

Current Sensing. Lossless current sensing converts the peak current signal to a voltage to sum in with the internal slope compensation. This summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. The slope compensation in the IC is adaptive to the input and output voltage. Therefore, the converter provides the proper amount of slope compensation to ensure stability and not an excess causing a loss of phase margin in the converter.

Error Amp. The error amplifier is a transconductance amplifier with g_m = 85µmhos. A simple compensation network is placed from the V_C pin to ground.

Current Limit. The current limit amplifier will shut the NMOS switch off once the current exceeds its threshold. The current amplifier delay to output is typically 50ns.

Zero Current Amp. The zero current amplifier monitors the inductor current to the output and shuts off the synchronous rectifier once the current is below 50mA, preventing negative inductor current.

Burst Mode Operation

Burst Mode operation is when the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 38µA. In this mode, the output ripple has a variable frequency component with load current and the steady state ripple will be typically below 3%.

During the period where the device is delivering energy to the output, the peak current will be equal to 400mA and the inductor current will terminate at zero current for each cycle. In this mode the maximum output current is given by:

$$I_{OUT(MAXBURST)} \approx \frac{V_{IN}}{6 \bullet V_{OUT}} \text{ Amps}$$

Burst Mode operation is user controlled by driving the MODE/SYNC pin high to enable and low to disable. It is recommended that Burst Mode operation be entered after the part has started up.

COMPONENT SELECTION

Inductor Selection

The high frequency operation of the LTC3423/LTC3424 allows the use of small surface mount inductors. The minimum inductance value is proportional to the operating frequency and is limited by the following constraints:

$$L > \frac{k}{f}\mu H \text{ and } L > \frac{V_{IN(MIN)} \bullet \left(V_{OUT(MAX)} - V_{IN(MIN)}\right)}{f \bullet Ripple \bullet V_{OUT(MAX)}} H$$

where

k = 3 for LTC3423, 2 for LTC3424

f = Operating Frequency (Hz)

Ripple = Allowable Inductor Current Ripple (A)

$V_{IN(MIN)}$ = Minimum Input Voltage (V)

$V_{OUT(MAX)}$ = Maximum Output Voltage (V)

APPLICATIONS INFORMATION

The inductor current ripple is typically set to 20% to 40% of the maximum inductor current.

For high efficiency, choose an inductor with a high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses and must be able to handle the peak inductor current at full load without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. See Table 1 for a list of component suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEBSITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Coiltronics	(516) 241-7876	(516) 241-9339	www.coiltronics.com
Murata	(814) 237-1431 (800) 831-9172	(814) 238-0490	www.murata.com
Sumida USA: Japan:	 (847) 956-0666 81-3-3607-5111	 (847) 956-0702 81-3-3607-5144	 www.japanlink.com sumida

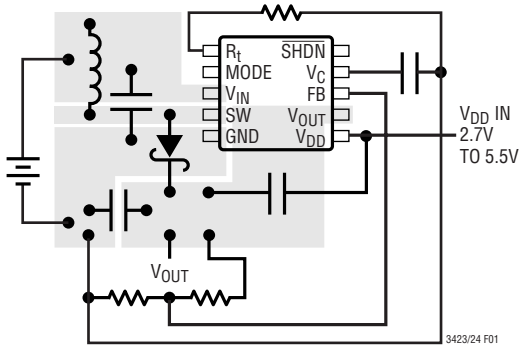


Figure 1. Recommended Component Placement. Traces Carrying High Current Are Direct. Trace Area FB and V_C Pins Are Kept Low. Lead Length to Battery Should be Kept Short

Output Capacitor Selection

The output voltage ripple has several components. The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The max ripple due to charge is given by:

$$VR_{BULK} = \frac{I_L \bullet V_{IN}(V_{OUT} - V_{IN})}{C_{OUT} \bullet V_{OUT} \bullet V_{OUT} \bullet f} \text{ Volts}$$

where

I_L = Average Inductor Current

I_P = Peak Inductor Current

The ESR is usually the most dominant factor for ripple in most power converters. The ripple due to capacitor ESR is simply given by:

$$VR_{CESR} = I_P \bullet R_{ESR} \text{ Volts}$$

where

R_{ESR} = Capacitor Series Resistance

Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, AVX TPS series tantalum capacitors and Sanyo POSCAP or Taiyo-Yuden ceramic capacitors are recommended. For through-hole applications Sanyo OS-CON capacitors offer low ESR in a small package size. See Table 2 for a list of component suppliers.

In some layouts it may be required to place a 1µF low ESR capacitor as close to the V_{OUT} and GND pins as possible.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEBSITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. In most applications a 3.3µF is sufficient.

Output Diode

The Schottky diode across the synchronous PMOS switch is not required, but provides a lower drop during the break-before-make time (typically 20ns) of the NMOS to PMOS transition. The addition of the Schottky diode will improve peak efficiency (see graph "Efficiency Loss Without Schottky vs Frequency"). Use of a Schottky diode such as a MBRM120T3, 1N5817 or equivalent. Since slow recovery times will compromise efficiency, do not use ordinary rectifier diodes.

APPLICATIONS INFORMATION

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is determining the sensitive frequency bands that cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz. In this case, converter frequencies up to 3MHz may be employed.

The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter caps go down in value and size. The trade off is in efficiency since the switching losses due to gate charge are going up proportional with frequency.

Another operating frequency consideration is whether the application can allow "pulse skipping." In this mode, the minimum on time of the converter cannot support the duty cycle, so the converter ripple will go up and there will be a low frequency component of the output ripple. In many applications where physical size is the main criterion then running the converter in this mode is acceptable. In applications where it is preferred not to enter this mode, then the maximum operating frequency is given by:

$$f_{MAX\_NOSKIP} = \frac{V_{OUT} - V_{IN}}{V_{OUT} \bullet t_{ON(MIN)}} Hz$$

where $t_{ON(MIN)}$ = minimum on time = 140ns

Reducing Output Capacitance with a Load Feed Forward Signal

In many applications the output filter capacitance can be reduced for the desired transient response by having the device commanding the change in load current, (i.e. system microcontroller), inform the power converter of the changes as they occur. Specifically, a "load feed forward" signal coupled into the V_C pin gives the inner current loop a head start in providing the change in output current. The transconductance of the LTC3423 converter at the V_C pin with respect to the inductor current is typically 130mA/100mV, and the LTC3424 is typically 170mA/100mV, so the amount of signal injected is proportional to the anticipated change of inductor current with load. The outer voltage loop performs the remainder of the correction, but because of the load feed forward signal, the range over which it must slew is greatly reduced. This results in an improved transient response. A logic level feed forward signal, V_{FF}, is coupled through components C5 and R6. The amount of feed forward signal is attenuated with resistor R6 and is given by the following relationship:

$$R6 \approx \left(\frac{V_{FF} \bullet R5 \bullet V_{IN} \bullet 1.5}{V_{OUT} \bullet \Delta I_{OUT}} \right) - R5$$

where ΔI_{OUT} = load current change.

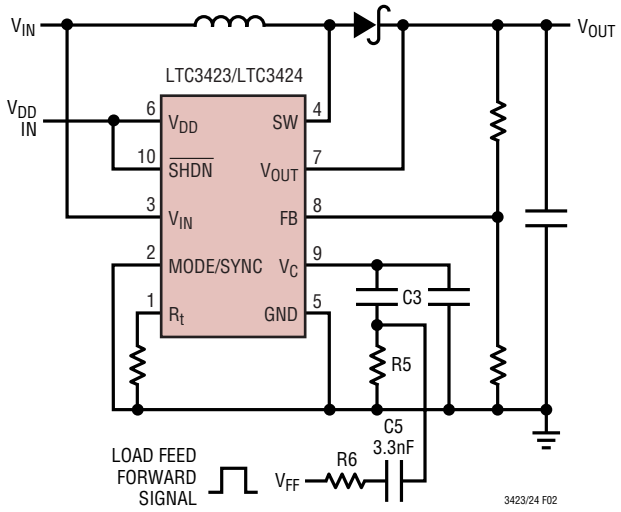


Figure 2

Closing the Feedback Loop

The LTC3423/LTC3424 uses current mode control with internal adaptive slope compensation. Current mode control eliminates the 2nd order filter due to the inductor and output capacitor exhibited in voltage mode controllers, and simplifies it to a single-pole filter response. The product of the modulator control to output DC gain plus the error amp open-loop gain equals the DC gain of the system.

APPLICATIONS INFORMATION

$$G_{DC} = G_{CONTROLOUTPUT} \bullet G_{EA}$$

$$G_{CONTROL} = \frac{2 \bullet V_{IN}}{I_{OUT}},\ G_{EA} \approx 2000$$

The output filter pole is given by:

$$f_{FILTERPOLE} = \frac{I_{OUT}}{\pi \bullet V_{OUT} \bullet C_{OUT}} Hz$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTERZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} Hz$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature of the boost regulator topology is the right half plane zero (RHP) and is given by:

$$f_{RHPZ} = \frac{V_{IN}^2 \bullet R_O}{2 \bullet \pi \bullet L \bullet V_O^2} Hz$$

At heavy loads this gain increase with phase lag can occur at a relatively low frequency. The loop gain is typically rolled off before the RHP zero frequency.

The typical error amp compensation is shown in Figure 3. The equations for the loop dynamics are as follows:

$$f_{POLE1} \approx \frac{1}{2 \bullet \pi \bullet 20 \bullet 10^6 \bullet C_{C1}} Hz$$

which is extremely close to DC

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C1}} Hz$$

$$f_{POLE2} \approx \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C2}} Hz$$

Refer to Application Note AN76 for more closed loop examples.

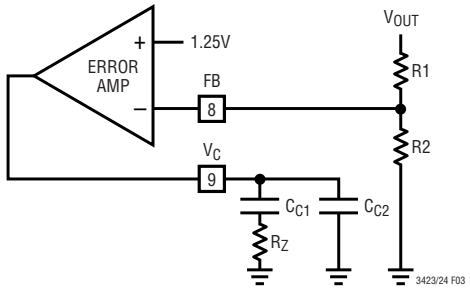
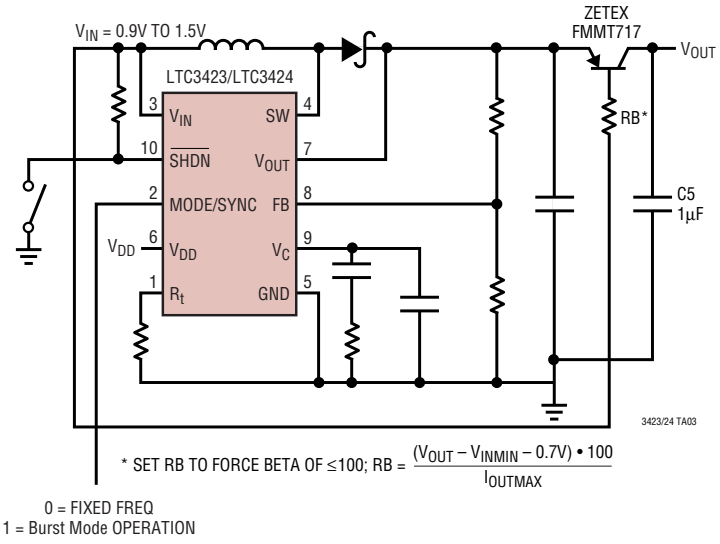


Figure 3

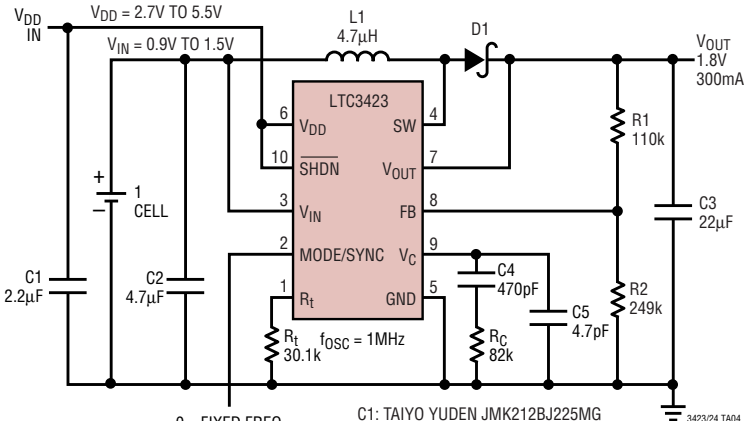
TYPICAL APPLICATION

Typical Application with Output Disconnect



TYPICAL APPLICATION

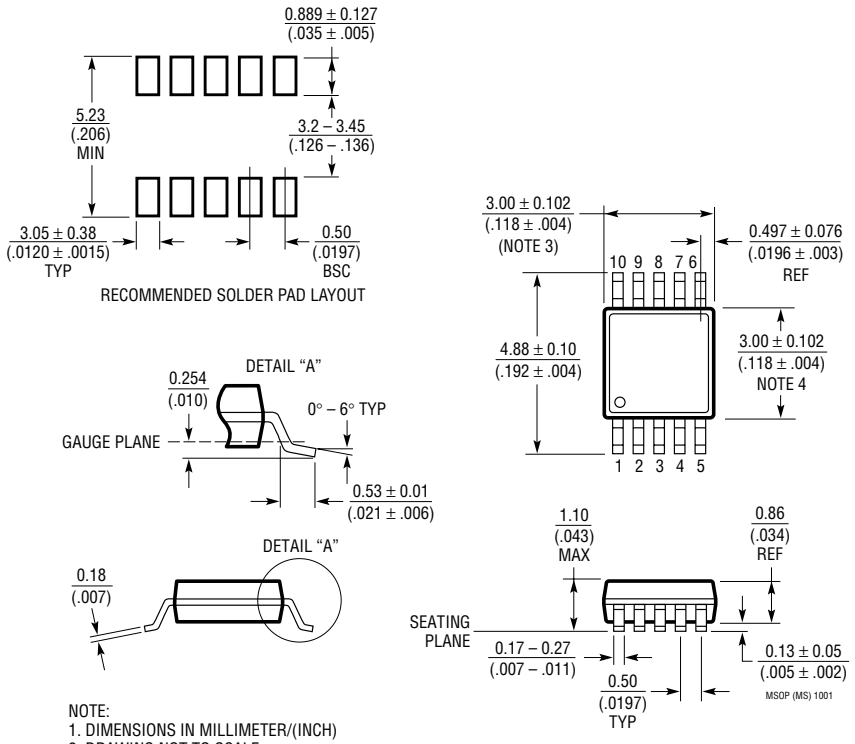
Single Cell to 1.8V at 300mA, 1.8mm High



C1: TAIYO YUDEN JMK212BJ225MG
C2: TAIYO YUDEN JMK212BJ475MM
C3: TAIYO YUDEN JMK325BJ226MM
D1: ON SEMICONDUCTOR MBRM120T3
L1: SUMIDA CDRH3D16-4R7M

PACKAGE DESCRIPTION

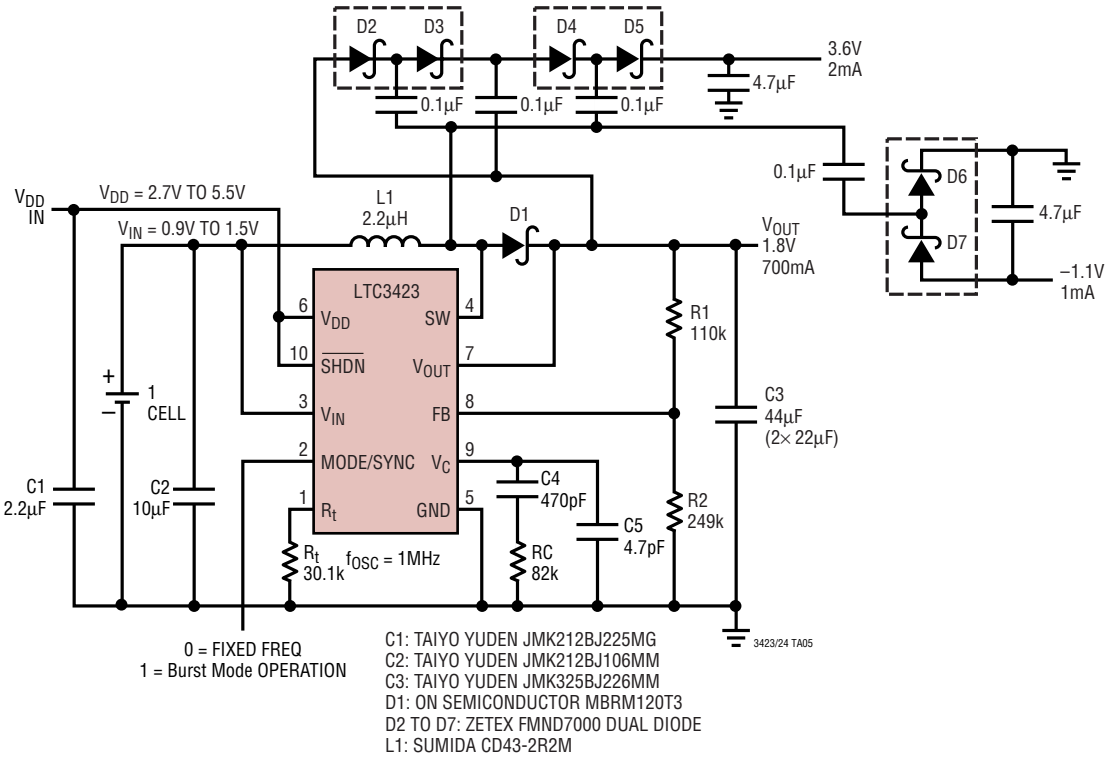
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Triple Output Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1306	Sync, Fixed Frequency, Step-Up DC/DC Converter	Internal 2A Switches, V_{IN} As Low As 1.8V
LT1308A/LT1308B	High Current, Micropower, Single Cell 600kHz DC/DC Converter	5V at 1A from Single Li-Ion Cell
LT1317/LT1317B	Micropower 600kHz PWM DC/DC Converter	V_{IN} As Low As 1.5V, I_Q = 100µA
LT1610	1.7MHz, Single Cell Micropower DC/DC Converter	3V at 30mA from 1V, 5V at 200mA from 3.3V
LT1613	1.4MHz, Single Cell DC/DC Converter in ThinSOT™	V_{IN} As Low As 1.1V, 3V at 30mA from Single Cell
LT1615	Micropower Step-Up DC/DC Converter in ThinSOT	I_Q = 20µA, 1µA Shutdown Current, V_{IN} As Low As 1V
LT1949	600kHz, 1A Switch PWM DC/DC Converter	1.1A, 0.5Ω/30V Internal Switch, V_{IN} As Low As 1.8V
LTC3400/LTC3400B	ThinSOT, 600mA, 1.2MHz Boost Converter	92% Efficiency, 0.85V ≤ V_{IN}, 2.6V ≤ V_{OUT} ≤ 5V
LTC3401	Single Cell, High Current (1A) Micropower, Synchronous 3MHz Step-Up DC/DC Converter	V_{IN} = 0.5V to 5.5V, Up to 97% Efficiency Synchronizable Oscillator from 100kHz to 3MHz
LTC3402	Single Cell, High Current (2A) Micropower, Synchronous 3MHz Step-Up DC/DC Converter	V_{IN} = 0.5V to 5.5V, Up to 97% Efficiency Synchronizable Oscillator from 100kHz to 3MHz

ThinSOT is a trademark of Linear Technology Corporation.

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