ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Input Voltages
- V_{INA}, V_{INB} ..... –0.3V to 140V
- PSA, PSB, RS1A, RS1B, RS2A, RS2B ..... –0.3V to 6V
- INHA, INHB, INLA, INLB ..... –0.3V to 6V

Output Voltages
- OUTA, OUTB ..... –0.3V to 140V

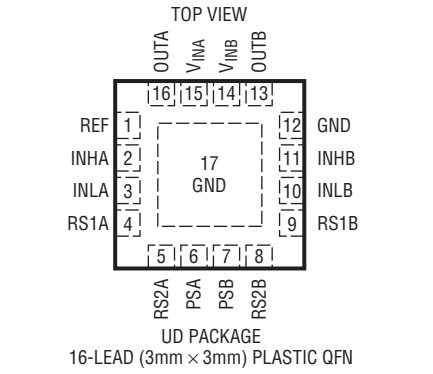
Average Currents
- V_{INA}, V_{INB} ..... –20mA
- OUTA, OUTB ..... ±5mA
- REF ..... ±5mA
- INHA, INHB, INLA, INLB ..... –1mA

Operating Ambient Temperature Range
- LTC2966C ..... 0°C to 70°C
- LTC2966I ..... –40°C to 85°C
- LTC2966H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

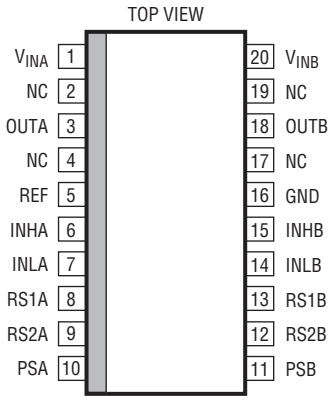
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN 17) PCB GND CONNECTION OPTIONAL



SW PACKAGE
20-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 35°C/W

ORDER INFORMATION http://www.linear.com/product/LTC2966#orderinfo

LEAD FREE FINISH

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2966CUD#PBF	LTC2966CUD#TRPBF	LGMG	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC2966IUD#PBF	LTC2966IUD#TRPBF	LGMG	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC2966HUD#PBF	LTC2966HUD#TRPBF	LGMG	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC2966CSW#PBF	LTC2966CSW#TRPBF	LTC2966SW	20-Lead Plastic Small Outline (Wide .300 Inch)	0°C to 70°C
LTC2966ISW#PBF	LTC2966ISW#TRPBF	LTC2966SW	20-Lead Plastic Small Outline (Wide .300 Inch)	–40°C to 85°C
LTC2966HSW#PBF	LTC2966HSW#TRPBF	LTC2966SW	20-Lead Plastic Small Outline (Wide .300 Inch)	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{INA} = V_{INB} = 12V, RS1/RS2 = GND, PS = GND, INH = 1.2V, INL = GND (Notes 1, 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Range	V_{INA} or V_{INB}	●	3.5		100	V
V_{MON}	V_{IN} Monitor Range	(Note 3)	●	1.75		98	V
I_{VA}	V_{INA} Input Supply Current	V_{INA} = 100V, V_{INB} = GND, 40x V_{INA} = GND, V_{INB} = 100V, 40x	● ●	3	7	15 ±50	µA nA
I_{VB}	V_{INB} Input Supply Current	V_{INB} = 100V, V_{INA} = GND, 40x V_{INB} = GND, V_{INA} = 100V, 40x V_{INB} = 100V, V_{INA} = 5V, 40x	● ● ●	3	7 2	15 ±50 4	µA nA µA
V_{UVLO}	Undervoltage Lockout	V_{INA} or V_{INB} Rising	●			3	V
	Undervoltage Lockout Hysteresis	V_{INA} and V_{INB} Falling			70		mV
Comparator Reference Input: INHA, INHB, INLA, INLB							
V_{CM}	Comparator Common Mode Voltage		●	0.35		2.45	V
V_{ERR}	V_{IN} Error Voltage at 96V	INH = V_{REF}, 40x 0.35V ≤ INH ≤ 2.4V, 40x	● ●		±250 ±250	±1360 ±400	mV mV
	V_{IN} Error Voltage at 48V	INH = V_{REF}, 20x 0.35V ≤ INH ≤ 2.4V, 20x	● ●		±100 ±100	±630 ±150	mV mV
	V_{IN} Error Voltage at 24V	INH = V_{REF}, 10x 0.35V ≤ INH ≤ 2.4V, 10x	● ●		±35 ±35	±315 ±75	mV mV
	V_{IN} Error Voltage at 12V	INH = V_{REF}, 5x 0.35V ≤ INH ≤ 2.4V, 5x	● ●		±15 ±15	±155 ±35	mV mV
V_{OS}	Comparator Offset Voltage	INH = 0.35V, 10x	●		±1.9	±3	mV
AV_{ERR}	Internal Resistive Divider Range Error	INH = 2.4V, Range = 5x, 10x, 20x, 40x	●			±0.4	%
V_{HYS}	Comparator Built-in Hysteresis	INH = GND, INL Rising INL = GND, INH Falling	● ●	14 –30	22 –22	30 –14	mV mV
V_{HYTH}	Built-in Hysteresis Enable Threshold		●	100		175	mV
t_{PD}	V_{IN} to OUT Comparator Propagation Delay	Overdrive = 10%, OUT Falling, 10x INH = GND, INL = 1.2V	●		40	80	µs
$I_{IN(LKG)}$	Input Leakage Current (INH, INL)	V = 1.2V, I-Grade V = 1.2V, H-Grade	● ●		±0.1 ±0.1	±1 ±10	nA nA
Reference: REF							
V_{REF}	Reference Output Voltage	I_{REF} ≤ 100µA, V_{IN} ≥ 3.5V	●	2.378	2.402	2.426	V
Noise	Reference Output Noise	100Hz to 100kHz			140		μV_{RMS}
Control Inputs: RS1A, RS2A, RS1B, RS2B, PSA, PSB							
V_{TH}	Select Input Threshold		●	0.4		1.4	V
I_{LKG}	Input Leakage Current	V = 2.4V	●			±100	nA
Status Outputs: OUTA, OUTB							
V_{OL}	Voltage Output Low	V_{IN} = 1.25V, I = 10µA V_{IN} = 3.5V, I = 500µA	● ●			100 400	mV mV
V_{OH}	Voltage Output High	V_{IN} = 3.5V, I = –1µA V_{IN} ≥ 4.5V, I = –1µA	● ●	2 2.5	2.375 3	2.75 4	V V
I_{OH}	Output Current High	V = GND, V_{IN} = 3.5V	●	–15	–7.5	–5	µA
$I_{O(LKG)}$	Leakage Current, Output High	V = 100V, V_{IN} = 6V	●			±250	nA

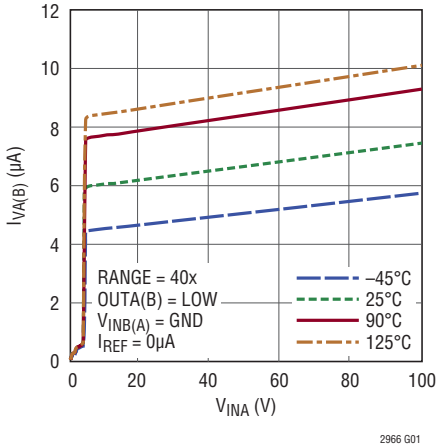
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

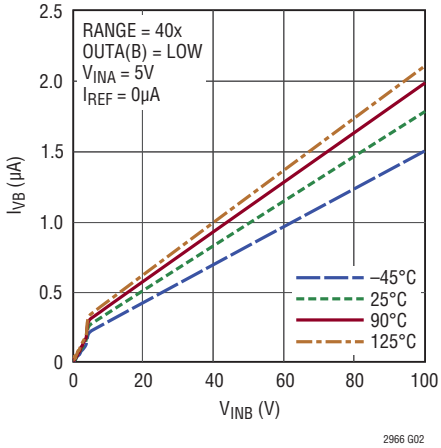
Note 3: Requires either V_{INA} or V_{INB} >3.5V.

TYPICAL PERFORMANCE CHARACTERISTICS

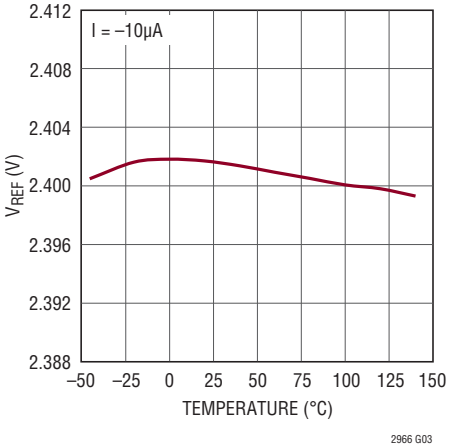
Supply Current vs $V_{INA(B)}$



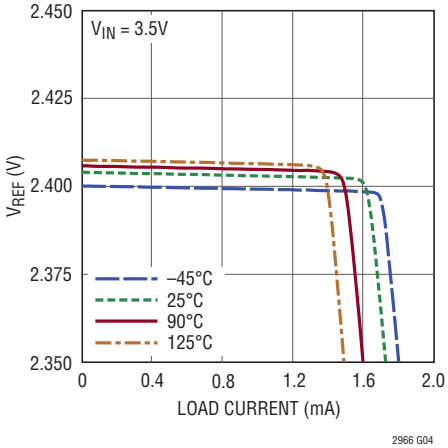
V_{INB} Pin Current vs V_{INB}



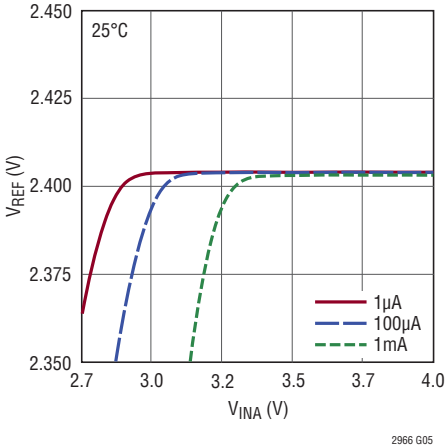
V_{REF} vs Temperature



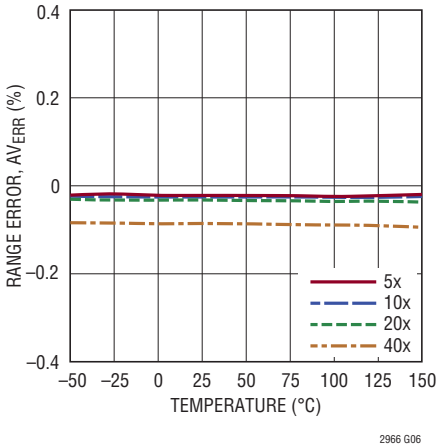
V_{REF} vs Load Current



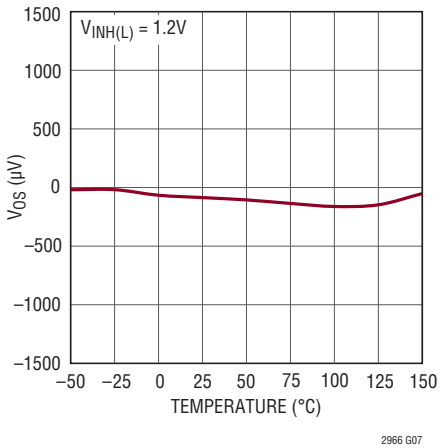
V_{REF} vs $V_{INA(B)}$



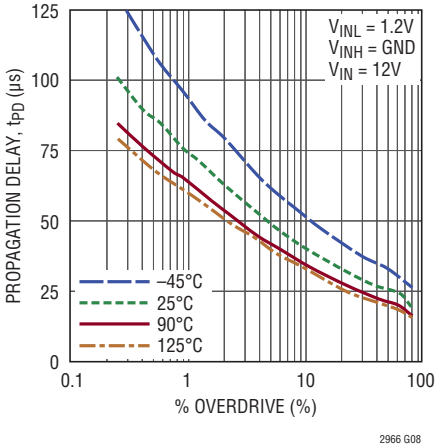
% Range Error vs Temperature



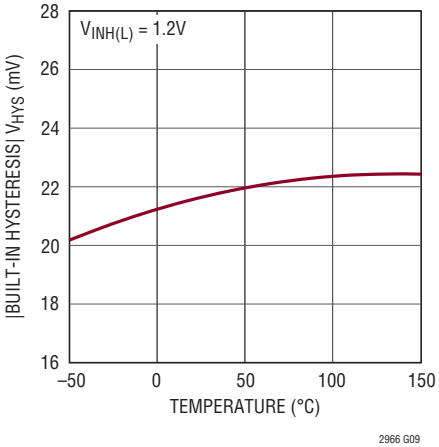
Comparator V_{OS} vs Temperature



V_{IN} Falling Propagation Delay vs % Overdrive

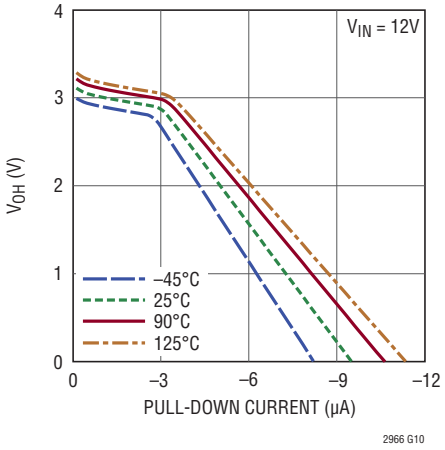


Built-In Hysteresis vs Temperature

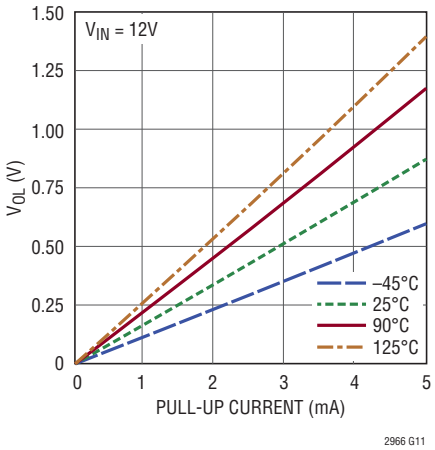


TYPICAL PERFORMANCE CHARACTERISTICS

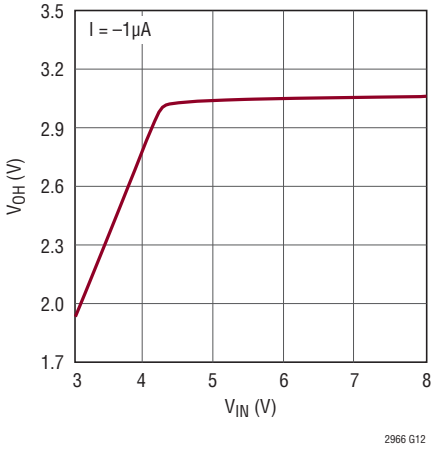
Voltage Output High vs Pull-Down Current (OUTA/OUTB)



Voltage Output Low vs Pull-Up Current (OUTA/OUTB)



Voltage Output High vs Input Voltage



PIN FUNCTIONS

Exposed Pad (UD16 Only): Exposed pad may be left floating or connected to device ground.

GND: Device Ground.

INHA: Channel A High Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the V_{INA} high or rising threshold. Keep within valid voltage range, V_{CM}, or tie to GND to configure built-in hysteresis where high threshold for V_{INA} becomes INLA + V_{HYS} scaled according to the RS pin configuration.

INHB: Channel B High Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the V_{INB} high or rising threshold. Keep within valid voltage range, V_{CM}, or tie to GND to configure built-in hysteresis where high threshold for V_{INB} becomes INLB + V_{HYS} scaled according to the RS pin configuration.

INLA: Channel A Low Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the V_{INA} low or falling threshold. Keep within valid voltage range, V_{CM}, or tie to GND to configure built-in hysteresis where low threshold becomes INHA – V_{HYS} scaled according to the RS pin configuration. Otherwise, INHA-INLA sets the hysteresis of the Channel A comparator. Oscillation will occur if INLA > INHA unless built-in hysteresis is enabled.

INLB: Channel B Low Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the V_{INB} low or falling threshold. Keep within valid voltage range, V_{CM}, or tie to GND to configure built-in hysteresis where low threshold becomes INHB – V_{HYS} scaled according to the RS pin configuration. Otherwise, INHB-INLB sets the hysteresis of the Channel B comparator. Oscillation will occur if INLB > INHB unless built-in hysteresis is enabled.

OUTA: Channel A Comparator Output. OUTA consists of a high voltage active pull-down and a gated, resistive (500kΩ) pull-up to an internally generated supply between 3.5V and 5V depending on input supply voltage. Blocking circuitry at the pin allows the pin to be resistively pulled up to voltages as high as 100V without back conducting onto the internal supply of the part. Polarity with respect to the V_{INA} pin is configured using the polarity select pin, PSA. OUTA pulls low when the part is in UVLO.

PIN FUNCTIONS

OUTB: Channel B Comparator Output. OUTB consists of a high voltage active pull-down and a gated, resistive (500kΩ) pull-up to an internally generated supply between 3.5V and 5V depending on input supply voltage. Blocking circuitry at the pin allows the pin to be resistively pulled up to voltages as high as 100V without back conducting onto the internal supply of the part. Polarity with respect to the V_{INB} pin is configured using the polarity select pin, PSB. OUTB pulls low when the part is in UVLO.

PSA: Channel A Polarity Selection. Connect to REF or a voltage >V_{TH} to configure comparator output to be inverting with respect to V_{INA}. Otherwise connect pin to GND to configure comparator output to be noninverting with respect to V_{INA}.

PSB: Channel B Polarity Selection. Connect to REF or a voltage >V_{TH} to configure comparator output to be inverting with respect to V_{INB}. Otherwise connect pin to GND to configure comparator output to be noninverting with respect to V_{INB}.

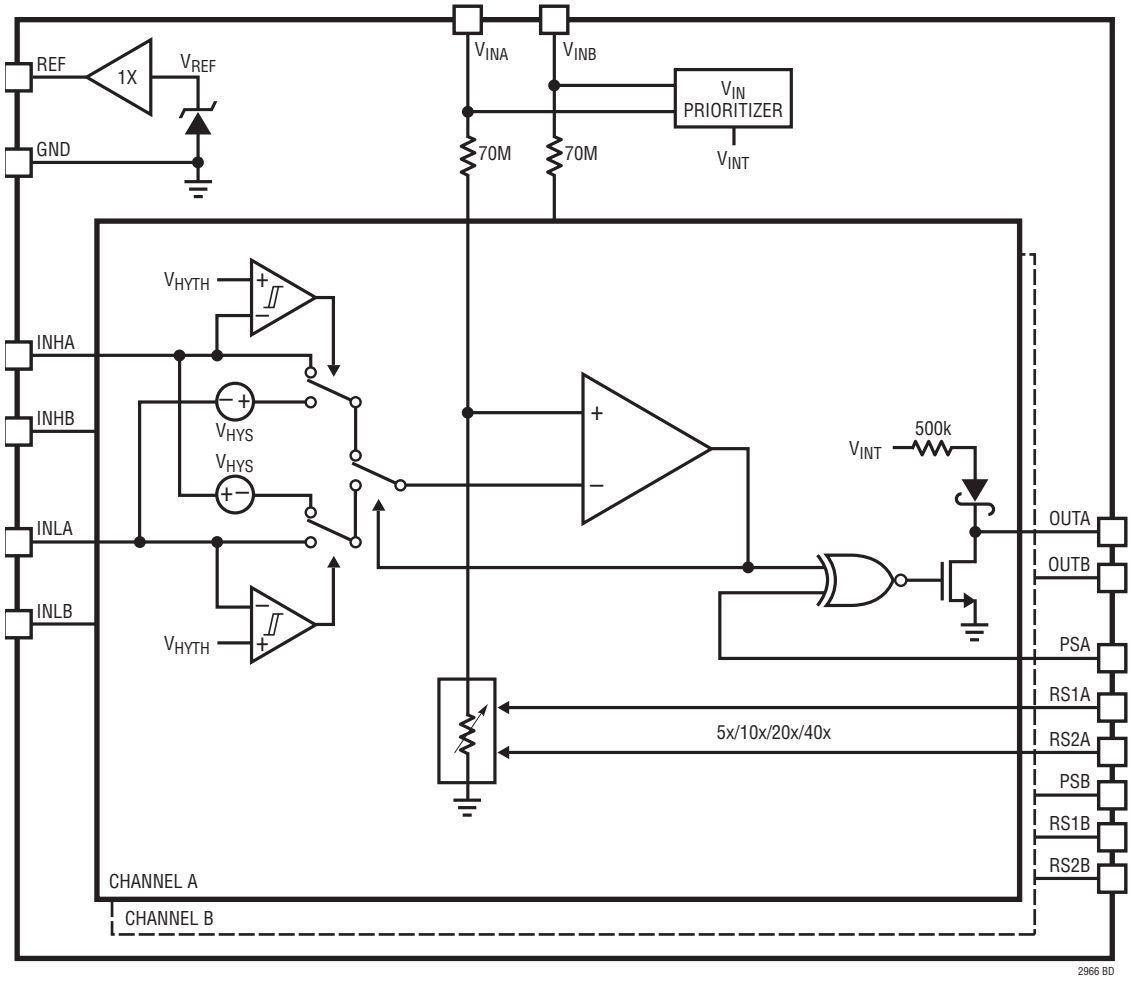
REF: Reference Output. V_{REF} with respect to GND. Use a maximum of 1nF to bypass unless damping resistor is used.

RS1A-RS2A: Channel A Range Select Input. RS1A-RS2A select 5x, 10x, 20x or 40x range for Channel A. Connect to REF or GND to configure the pin. (See Table 1)

RS1B-RS2B: Channel B Range Select Input. RS1B-RS2B select 5x, 10x, 20x or 40x range for Channel B. Connect to REF or GND to configure the pin. (See Table 1)

V_{INA}, V_{INB}: Voltage Monitor and Supply Inputs. An internal high value resistive divider is connected to the pin. The greater of V_{INA} and V_{INB} is used to generate an internal voltage rail with priority given to V_{INA}. If both V_{INA} and V_{INB} fall below the UVLO threshold minus hysteresis, the outputs are pulled low. If $V_{INB} < V_{INA} < 1.2V$, the logic state of the outputs cannot be guaranteed.

BLOCK DIAGRAM



OPERATION

The LTC2966 is a micropower dual channel voltage monitor with a 100V maximum operating voltage. Each channel is comprised of an internal high value resistive divider and a comparator with a high voltage output. A reference voltage is provided to allow the thresholds of each channel to be set independently. This configuration has the advantage of being able to monitor very high voltages with very little current draw while threshold configuration is done using low value resistors at low voltages.

The two channels of the LTC2966 provide independent monitoring capabilities for multiple voltages or work in conjunction to set up an undervoltage/overvoltage monitor. Integration of a resistive divider for high voltage sensing makes the LTC2966 a compact and low power solution for generating voltage status signals to a monitoring system.

A built-in buffered reference gives the monitor flexibility to operate independently from a high voltage supply without the requirement of additional low voltage biasing. The reference provides an accurate voltage from which a resistive divider to ground configures the threshold voltage for the internal comparators. In addition, the REF pin can be used as a logic high voltage for the range and polarity select pins.

The input voltage threshold at V_{IN} is determined by the voltage on the INH and INL pins which are scaled by the attenuation internal resistive divider. In the LTC2966 the attenuation of the internal divider is configured using two range select pins, RS1 and RS2 to select 5x, 10x, 20x or 40x for each channel. Use Table 1 to determine the correct configuration for a desired range setting. The polarity select pins, (PSA/PSB), configure the corresponding OUT pin to be inverting or noninverting with respect to V_{IN} allowing the part to be configured for monitoring overvoltage and undervoltage conditions with either polarity output.

Table 1.

V_{IN} MONITOR RANGE	RANGE SELECTION	RS1	RS2
1.75V* to 12.25V	5x	L	L
3.5V to 24.5V	10x	H	L
7V to 49V	20x	L	H
14V to 98V	40x	H	H

*Requires either V_{INA} or V_{INB} > 3.5V.

The INH pin determines the high or rising edge threshold for V_{IN} in each channel. If the monitored voltage connected to V_{INA} rises to the scaled INHA voltage then the OUT pin is pulled high assuming PSA is ground. Likewise, the INL pin determines the low or falling edge threshold for V_{IN} in each channel. If V_{INA} falls to the scaled INLA voltage then the OUT pin is pulled low assuming PSA is ground. The amount of hysteresis referred to V_{IN} is the difference in voltage between INH and INL scaled according to the RS pin configuration. INH and INL have an allowable voltage range, V_{CM}. Figure 1 shows the allowable monitor voltage at V_{IN} for each range as a function of comparator reference input voltage (INL, INH).

Typically, an external resistive divider biased from REF is used to generate the INH and INL pin voltages. A built-in hysteresis feature requiring only two resistors can be enabled on either the V_{IN} rising edge by grounding INH or on the falling edge by grounding INL. For example, it is appropriate to ground INH to activate rising edge hysteresis if an accurate falling voltage threshold is required for undervoltage detection. Conversely, it is appropriate to ground INL for falling edge built-in hysteresis if an accurate overvoltage threshold is required. Do not ground both INH and INL. Oscillation occurs if $V_{INL} > V_{INH}$ unless INH built-in hysteresis is enabled.

OPERATION

The high voltage OUT pins have the capability to be pulled up to a user defined voltage as high as 100V with an external resistor. The LTC2966 also includes an internal 500k pull-up resistor to an internal voltage between 3.5V and 5V depending on input supply voltage. (See V_{OH} in Electrical Characteristics) Wire-OR functionality is implemented by connecting OUTA and OUTB with appropriate monitor configuration.

Supply current is drawn from the higher of V_{INA} or V_{INB} with priority given to V_{INA}. If both V_{IN} pins fall below the UVLO threshold then both OUT pins are pulled low regardless of the PS pin state.

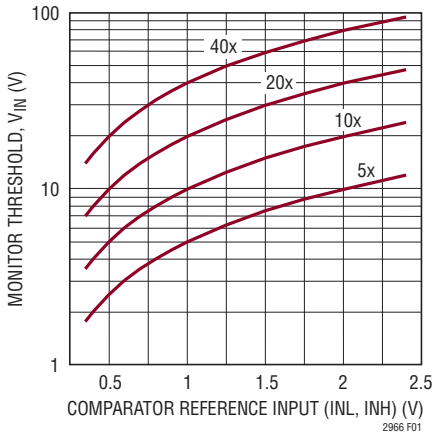


Figure 1. Monitor Threshold Threshold vs Comparator Reference Inputs

APPLICATIONS INFORMATION

Threshold Configuration

Each LTC2966 channel (A/B) monitors the voltage applied to the corresponding V_{IN} input. A comparator senses the V_{IN} pin on one of its inputs through the internal resistive divider. The other input is connected to INH/INL that is in turn biased with external resistive dividers off of the REF pin as shown in Figure 2a and 2b. The V_{IN} rising and falling thresholds are determined by:

$V_{IN(RISE)}$ = RANGE • V_{INH}

$V_{IN(FALL)}$ = RANGE • V_{INL}

Where RANGE is the configured range of the internal resistive divider. In order to set the threshold for the LTC2966, choose an appropriate range setting for the desired V_{IN} voltage threshold such that the INH and INL voltages are within the specified common mode range, V_{CM}. For example, if a falling threshold of 18V is desired for monitoring a 24V power supply then a range greater than 10x is allowed. However, to maximize the accuracy of the V_{IN} threshold the smallest acceptable range is used, 10x in this case. To implement 2V of hysteresis referred to V_{IN} this means:

V_{INH} = 2V, V_{INL} = 1.8V

With 10x range the V_{IN} thresholds are:

$V_{IN(RISE)}$ = 20V, $V_{IN(FALL)}$ = 18V

One possible way to configure the thresholds is by using three resistors to set the voltages on INH and INL. See Figure 2a. The solution for R1, R2 and R3 provides three equations and three unknowns. Maximum resistor size is governed by maximum input leakage current. The maximum input leakage current below 85°C is 1nA. For a maximum error of 1% due to both input currents, the resistive divider current should be at least 100 times the sum of the leakage currents, or 0.2µA.

If in this example, a leakage current error of 0.1% is desired then the total divider resistance is 1.2MΩ which results in a current of 2µA through this network. For R_{SUM} = 1.2MΩ

$$R_{SUM} = R1 + R2 + R3$$

$$R1 = \frac{(V_{INL} \bullet R_{SUM})}{V_{REF}} = \frac{(1.8V \bullet 1.2M\Omega)}{2.402V} = 899.5k\Omega$$

The closest 1% value is 909kΩ. R2 can be determined from:

$$R2 = \frac{(V_{INH} \bullet R_{SUM})}{V_{REF}} - R1$$

$$= \frac{(2V \bullet 1.2M\Omega)}{2.402V} - 909k\Omega = 90.2k\Omega$$

The closest 1% value is 90.9kΩ. R3 can be determined from R_{SUM}:

R3 = R_{SUM} – R1 – R2 = 1.2MΩ – 909kΩ – 90.9kΩ = 200.1kΩ

The closest 1% value is 200kΩ. Plugging the standard values back into the equations yields the design values for the V_{INH} and V_{INL} voltages:

V_{INH} = 2.001V, V_{INL} = 1.819V

The corresponding threshold voltages are:

$V_{IN(RISE)}$ = 20.01V, $V_{IN(FALL)}$ = 18.19V

Another possible way to configure the thresholds is with independent dividers using two resistors per threshold to set the voltages on INH and INL. See Figure 2b. Care must be taken such that the thresholds are not set too close to each other, otherwise the mismatch of the resistors may cause the voltage at INL to be greater than the voltage at INH which may cause the comparator to oscillate.

As in the previous example, if R_{SUM} = 1.2MΩ is chosen and the target for V_{INL} is 1.8V:

$$R_{SUM} = R1 + R2$$

$$R1 = \frac{(V_{INL} \bullet R_{SUM})}{V_{REF}} = \frac{(1.8V \bullet 1.2M\Omega)}{2.402V} = 899.5k\Omega$$

The closest 1% value is 909kΩ. R2 can be determined by:

$$R2 = (V_{REF} - V_{INL}) \bullet \frac{R1}{V_{INL}}$$

$$= (2.402V - 1.8V) \bullet \frac{(909k\Omega)}{1.8V} = 304k\Omega$$

APPLICATIONS INFORMATION

The closest 1% value is 301kΩ. Plugging the standard values back into the equation for V_{INL} yields the design voltage for V_{INL}:

$$V_{INL} = \frac{(R1 \bullet V_{REF})}{(R1+R2)} = \frac{(909k\Omega \bullet 2.402V)}{(301k\Omega + 909k\Omega)} = 1.804V$$

At this point in the independent divider example only the values required to set the voltage at INL have been found. Repeat the process for the INH input by substituting the above equations with V_{INH} for V_{INL}, R3 for R1, R4 for R2 and V_{INH} = 2.0V.

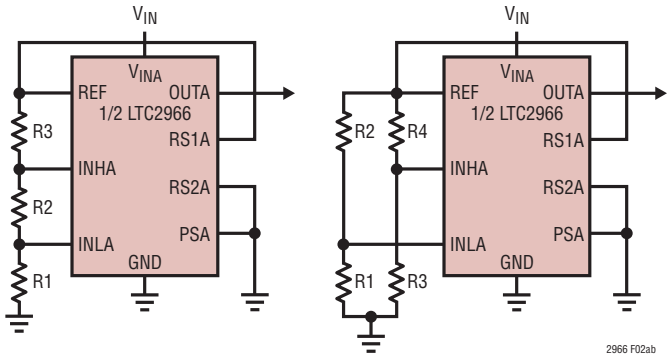


Figure 2a. Three-Resistor Threshold Configuration

Figure 2b. Two-Resistor Threshold Configuration

Using Built-In Hysteresis

The LTC2966 has the capability of simplifying the threshold configuration such that only two resistors per channel are required. The device pins can be configured to select a built-in hysteresis voltage, V_{HYS}, which can be applied to either the rising or falling threshold depending on whether the INH or INL pin is grounded. Note that the hysteresis voltage at each range setting remains at a fixed value. Figure 3 introduces examples of each configuration. For example, if INH is biased from an external divider and the INL pin is grounded, then hysteresis is enabled on the low or falling threshold. The low threshold is then $-V_{HYS}$ relative to the high threshold determined by INH. Figure 3a introduces built-in hysteresis on the rising edge because INH is pulled to ground. A two-resistor network, R1 and R2, is used to set the voltage on INL using:

$$\frac{R2}{R1} = \frac{V_{REF}}{V_{INL}} - 1$$

Using built-in hysteresis, the V_{IN} thresholds are:

$V_{IN(RISE)}$ = RANGE • (INL + V_{HYS})

$V_{IN(FALL)}$ = RANGE • INL

Figure 3b introduces built-in hysteresis on the falling edge because INL is pulled to ground. Similarly, a two-resistor network, R3 and R4, is used to set the voltage on INH using:

$$\frac{R4}{R3} = \frac{V_{REF}}{V_{INH}} - 1$$

Using built-in hysteresis the V_{IN} thresholds are:

$V_{IN(RISE)}$ = RANGE • INH

$V_{IN(FALL)}$ = RANGE • (INH – V_{HYS})

Consider V_{INH} = 2V with built-in hysteresis activated on the falling edge. For 10x range, 1.1% falling hysteresis is obtained. If a larger percentage of hysteresis is desired then V_{INH} is alternatively set to 1V and the range is selected to be 20x to obtain the same V_{IN} threshold but with 2.2% falling hysteresis. The amount of built-in hysteresis is scaled according to Table 2. If more hysteresis is needed then it is implemented in the external resistive divider as described in the Threshold Configuration section.

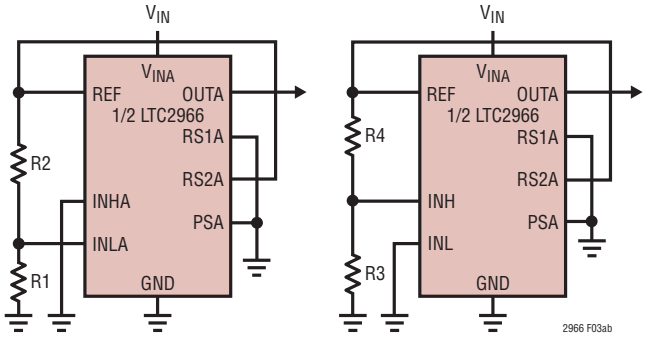


Figure 3a. Rising Edge Built-In Hysteresis by Grounding INH

Figure 3b. Falling Edge Built-In Hysteresis by Grounding INL

Table 2. Built-In Hysteresis Voltage vs Range

RANGE	V_{IN} REFERRED BUILT-IN HYSTERESIS
5x	110mV
10x	220mV
20x	440mV
40x	880mV

APPLICATIONS INFORMATION

Error Analysis

V_{IN} thresholds are subject to the following errors:

- REF Voltage Variation (ΔV_{REF})
- Comparator Offset (V_{OS})
- Internal Divider Range Error (A_{VERR})
- External Resistive Divider Error (A_{XERR})

The effect these errors have on the V_{IN} threshold is expressed by:

$$V_{ERR} = RANGE \bullet \left[\pm V_{OS} \pm \Delta V_{REF} \bullet \frac{V_{INH(L)}}{V_{REF}} \pm V_{INH(L)} \bullet A_{XERR} \right] \pm RANGE \bullet A_{VERR} \bullet V_{INH(L)}$$

$$A_{XERR} = 2 \bullet \frac{TOLERANCE}{100} \bullet \left(1 - \frac{V_{INH(L)}}{V_{REF}}\right)$$

External divider error is determined by the percentage tolerance values of the resistors. If 1% tolerance resistors are used in the external divider then there is a 2% worst-case voltage error associated with it. The effects of comparator offset and V_{REF} voltage are uncorrelated with each other. Therefore, a Root-Sum-Square can be applied to the error voltage referred to V_{IN}. Using the example from Threshold Configuration and assuming 1% resistors implement the external resistive divider, the falling V_{IN} threshold of approximately 18V has an error tolerance of:

$$V_{ERR(REF)} = (RANGE)\left(\pm \Delta V_{REF} \bullet \frac{V_{INL}}{V_{REF}}\right) = (10) \bullet \left(\pm 24mV \bullet \frac{1.8V}{2.402V}\right) = \pm 180mV$$

$$V_{ERR(EXT)} = (RANGE)\left(\pm V_{INL} \bullet 2 \bullet 0.01 \bullet \left(1 - \frac{V_{INL}}{V_{REF}}\right)\right) = (10) \bullet (\pm 1.8V \bullet 0.005) = \pm 90mV$$

$$V_{ERR(VOS)} = (RANGE)(\pm \Delta V_{OS}) = (10) \bullet (\pm 3mV) = \pm 30mV$$

$$V_{ERR(RS)} = (RANGE)(\pm A_{VERR})(\pm V_{INL}) = (10) \bullet (\pm 0.004) \bullet (1.8V) = \pm 72mV$$

$$V_{ERR} = \sqrt{V_{ERR(REF)}^2 + V_{ERR(EXT)}^2 + V_{ERR(VOS)}^2 + V_{ERR(RS)}^2} = \sqrt{(\pm 180mV)^2 + (\pm 90mV)^2 + (\pm 30mV)^2 + (\pm 72mV)^2} = \pm 216mV$$

The actual V_{IN} falling threshold has an error tolerance of ±216mV or ±1.2%.

Improving Threshold Accuracy

The biggest threshold error terms are:

- External Resistive Divider Accuracy
- REF Voltage Variation

Even using 1% tolerance resistors, external resistive divider accuracy still accounts for as much as ±2% threshold error while REF voltage variation accounts for ±1% threshold error. In order to minimize these threshold error terms, an external reference can be used to set the thresholds for INH/INL as shown in Figure 4. An LT6656-2.048 has an initial accuracy of 0.05% and provides bias via the 0.1% resistive divider network for INH and INL. It is biased off of the LTC2966 REF pin. The threshold error tolerance is calculated using the method described in the Typical Applications section with ΔV_{REF} = ±1.024mV given the initial accuracy of the LT6656 2.048V output and using 0.1% tolerance resistors for the external divider.

$$V_{ERR(REF)} = (RANGE)\left(\pm \Delta V_{REF} \bullet \frac{V_{INL}}{V_{REF}}\right) = (10) \bullet \left(\pm 1.024mV \bullet \frac{1.8V}{2.048V}\right) = \pm 9mV$$

$$V_{ERR(EXT)} = (RANGE)\left(\pm V_{INL} \bullet 2 \bullet 0.001 \bullet \left(1 - \frac{V_{INL}}{V_{REF}}\right)\right) = (10) \bullet (\pm 1.8V \bullet 0.0005) = \pm 9mV$$

$$V_{ERR(VOS)} = (RANGE)(\pm \Delta V_{OS}) = (10) \bullet (\pm 3mV) = \pm 30mV$$

$$V_{ERR(RS)} = (RANGE)(\pm A_{VERR})(\pm V_{INL}) = (10) \bullet (\pm 0.004) \bullet (1.8V) = \pm 72mV$$

$$V_{ERR} = \sqrt{V_{ERR(REF)}^2 + V_{ERR(EXT)}^2 + V_{ERR(VOS)}^2 + V_{ERR(RS)}^2} = \sqrt{(\pm 9mV)^2 + (\pm 9mV)^2 + (\pm 30mV)^2 + (\pm 72mV)^2} = \pm 79mV$$

The resulting V_{IN} threshold error is reduced to ±0.44% from ±1.2% in the previous error analysis example.

APPLICATIONS INFORMATION

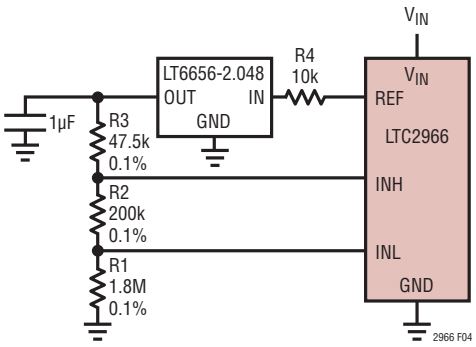


Figure 4. Reducing V_{IN} Threshold Error

Disabling a Channel

Figure 5 shows the proper technique for disabling a channel. Table 4 summarizes the correct connections. Correctly disabling an unused channel prevents its comparator output from chattering and introducing unwanted noise in the system.

Table 4. Disabling a Channel

PIN	CONNECT TO
V_{IN}	GND
INH	REF
INL	GND
RS1	GND or REF
RS2	GND or REF
PS	GND or REF
OUT	Open

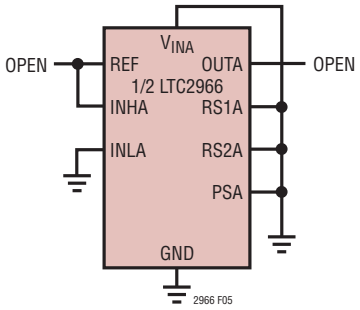


Figure 5. Disabling a Channel

Output Configuration with Polarity Selection

The OUT pin may be used with a wide range of user-defined voltages up to 100V with an external resistor. Select a resistor compatible with desired output rise time and load current specifications. When the status outputs are low, power is dissipated in the pull-up resistors. An internal pull-up is present if the OUT pins are left floating or if low power consumption is required. The internal pull-up resistor does not draw current if an external resistor pulls OUT up to a voltage greater than V_{OH}.

If PS is connected to ground, the comparator output is noninverting. This means that OUT pulls low when V_{IN} falls below the scaled INL voltage. OUT is released after V_{IN} rises above the scaled INH voltage. Likewise, if PS is connected to REF or a voltage $>V_{TH}$, the comparator output is inverting. This means that OUT pulls low when V_{IN} rises above the scaled INH voltage and is released when V_{IN} falls below the scaled INL voltage.

If both V_{IN} pins fall below the UVLO threshold minus hysteresis, the outputs are pulled to ground. The outputs are guaranteed to stay low for $V_{INA} \geq V_{INB} \geq 1.25V$ regardless of the output logic configuration.

It is recommended that circuit board traces associated with the OUT pin be located on a different layer than those associated with the INH/INL and REF pins where possible to avoid capacitive coupling.

Hot Swap Events

The LTC2966 can withstand high voltage transients up to 140V. However, when a supply voltage is abruptly connected to the input resonant ringing can occur as a result of series inductance. The peak voltage could rise to 2x the input supply, but in practice can reach 2.5x if a capacitor with a strong voltage coefficient is present. Circuit board trace inductances of as little as 10nH can produce significant ringing. Ringing beyond the absolute maximum specification can be destructive to the part and should be avoided whenever possible. One effective means to eliminate ringing seen at the V_{IN} pins and to protect the part is to include a 1kΩ to 5kΩ resistance between the monitored voltage and the V_{IN} pin as shown in Figure 6. This provides damping for the resonant circuit. If there is a decoupling capacitor on the V_{INA}/V_{INB} pins the time constant formed by the RC network should be considered.

APPLICATIONS INFORMATION

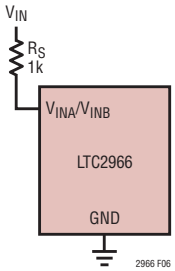


Figure 6. Hot Swap Protection

High Voltage Pin Creepage/Clearance Options

Appropriate spacing between component lead traces is critical to avoid flashover between conductors. There are multiple industry and safety standards that have different spacing requirements depending on factors such as operating voltage, presence of conformal coat, elevation, etc. The LTC2966 is available in a 20-lead SW package which offers pin-to-pin clearance of at least 0.76mm (0.03in) to satisfy high voltage external component lead specifications for standards such as the UL60950 and IPC2221. The package incorporates unconnected pins between all adjacent high voltage and low voltage pins to maximize PC board trace clearance. For voltages >30V the SW should be used, otherwise the smaller QFN is sufficient when clearance is not an issue. For more information, refer to the printed circuit board design standards described in IPC2221 and UL60950.

Voltage Reference

The REF pin is a buffered reference with a voltage of V_{REF} referenced to GND. A bypass capacitor up to 1000pF in value can be driven by the REF pin directly. Larger capacitances require a series resistance to dampen the transient response as shown in Figure 7A. If a resistive divider is already present then the bypass capacitor can be connected to the INH or INL pin as shown in Figure 7B. Figure 7C shows the resistor value required for different capacitor values to achieve critical damping. Bypassing the reference can help prevent false tripping of the comparators by preventing glitches on the INH/INL pins. Figure 8 shows the reference load transient response. Figure 9 shows the reference line transient response. If there is a decoupling capacitor on the INH/INL pin the time constant formed by the RC network should be considered. Use a capacitor with a compatible voltage rating.

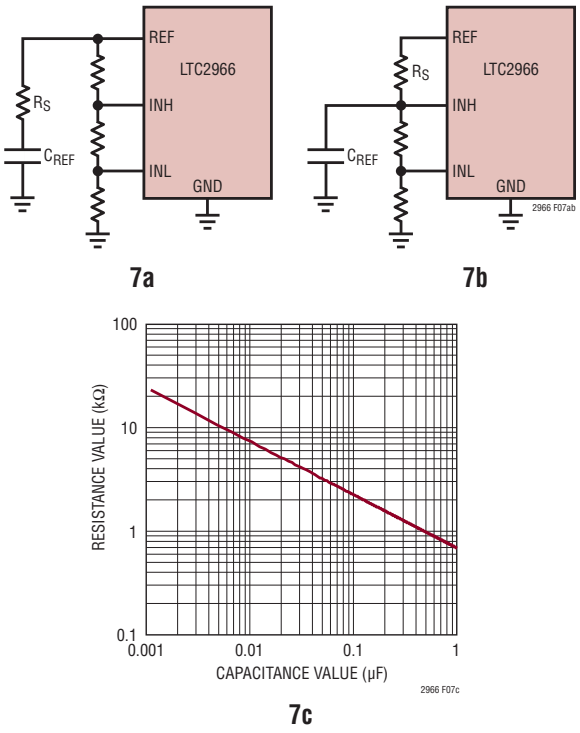


Figure 7. Using Series Resistance to Dampen REF Transient Response

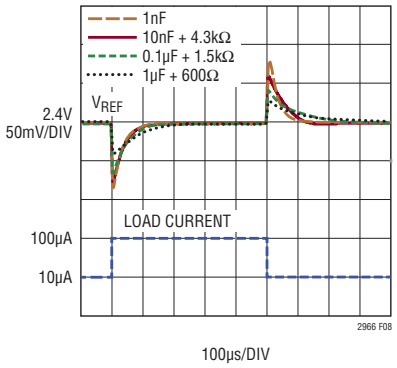


Figure 8. V_{REF} Load Transient

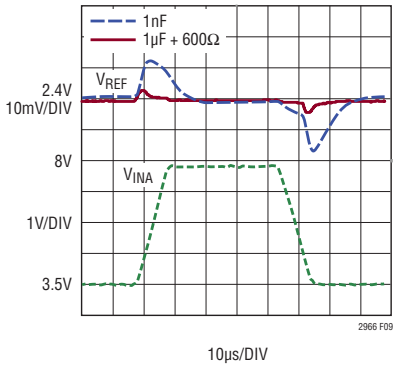


Figure 9. V_{REF} Line Transient

TYPICAL APPLICATIONS

48V UV/OV Monitor

The circuit in Figure 10 monitors a single 48V supply and is configured for UV/OV window detection. Channel A is used to monitor undervoltage conditions where the 36V threshold is determined by 1.8V at INLA scaled by 20x. Channel B is used to monitor overvoltage conditions where the 72V threshold is determined by the same 1.8V at INHB with 40x range. UV is pulled high to indicate an undervoltage condition when the supply drops below the UV threshold. Therefore PSA is pulled to REF to obtain the correct polarity on OUTA. OV is pulled high when the supply rises above the OV threshold which means PSB is pulled to ground to obtain the appropriate output polarity. Connecting INHA and INLB to ground enables internal hysteresis for each channel in the appropriate direction and reduces the number of external components.

±15V Undervoltage Monitor

The LTC2966 can be used to monitor a positive and a negative supply simultaneously. In the circuit shown in Figure 11, Channel B is used to monitor the –15V supply by connecting V_{INB}'s internal resistor divider to REF and configuring to 5x range. The voltage at the V_{IN} sensing input of the Channel B comparator is fixed at 480mV. When the –15V supply is undervoltage INHB > 480mV and OUTB is pulled low because PSB is connected to ground. As the negative supply comes into regulation the comparator monitors the INHB pin to detect when its voltage crosses 480mV corresponding to –14.3V. $\overline{UVB}$ is released indicating that there is no longer an undervoltage condition. As the negative supply drops out of regulation the comparator monitors the INLB pin to detect when its voltage crosses 480mV, corresponding to –13.6V due to the external divider

48V OV/UV MONITOR

CHANNEL	A	B
RISING THRESHOLD	36.6V	72.2V
FALLING THRESHOLD	36.0V	71.2V
HYSTERESIS	0.6V	1.0V
RANGE	20x	40x

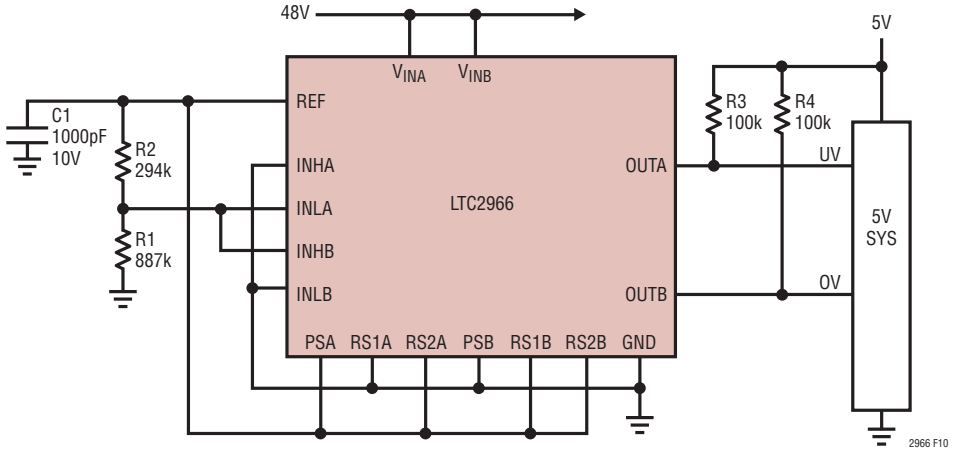


Figure 10. Use Range Selection and Built-In Hysteresis to Minimize External Components

TYPICAL APPLICATIONS

gain. $\overline{UVB}$ is pulled low after the comparator detects the threshold crossing to indicate an undervoltage condition. Channel A is configured to monitor for an undervoltage condition on the 15V supply by pulling $\overline{UVA}$ low when the positive supply drops below 13.6V.

–48V UV/OV Voltage Monitor

In the circuit shown in Figure 12, the LTC2966 is configured as a –48V UV/OV monitor by referencing the GND pin to the negative supply. R1 through R4 configure the UV and OV thresholds, where channel A and B are configured similarly to the 48V UV/OV monitor circuit in Figure 10. Hysteresis for each comparator is implemented by the external resistor network. High voltage OUT pins allow a pair of 4N25 opto-couplers to be used in translating the status signals for the 5V system. R5, R6, R7 and R8 set the maximum current through the optos to be approximately 4.2mA. If an exposed pad is present it should be tied to the GND pin or left open.

±15V UV MONITOR

CHANNEL	A	B
RISING THRESHOLD	14.3V	–14.4V
FALLING THRESHOLD	13.5V	–13.6V
HYSTERESIS	0.8V	–0.8V
RANGE	10x	5x

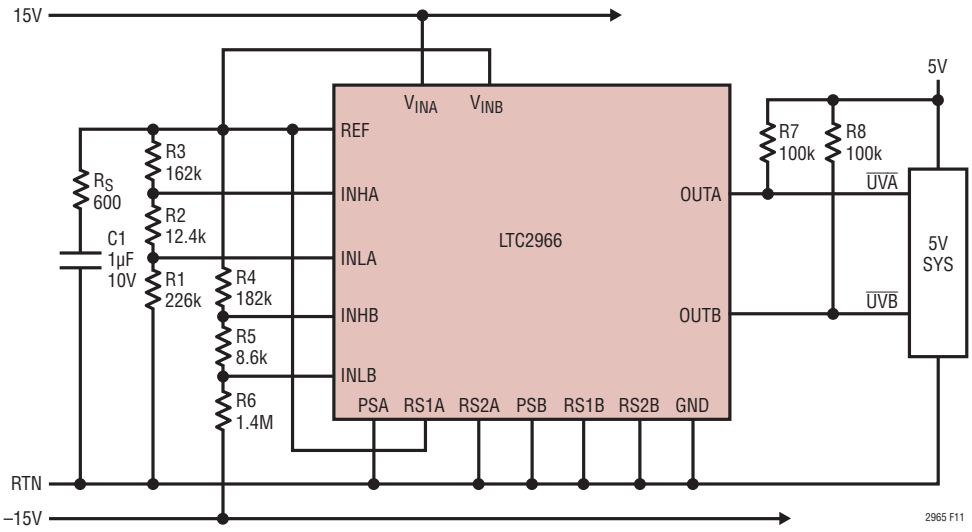
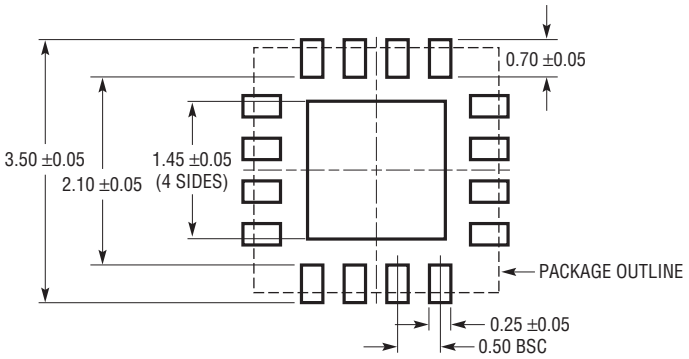


Figure 11. Dual Polarity Voltage Monitoring

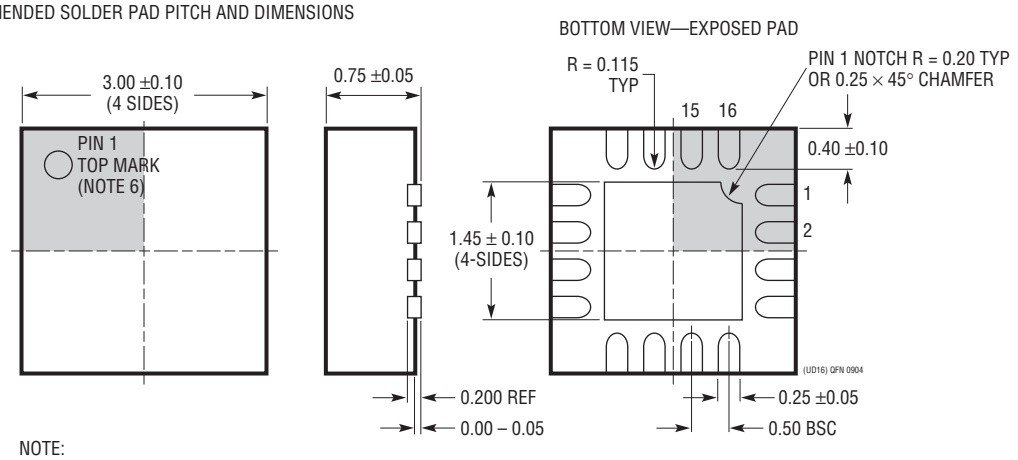
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2966#packaging for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

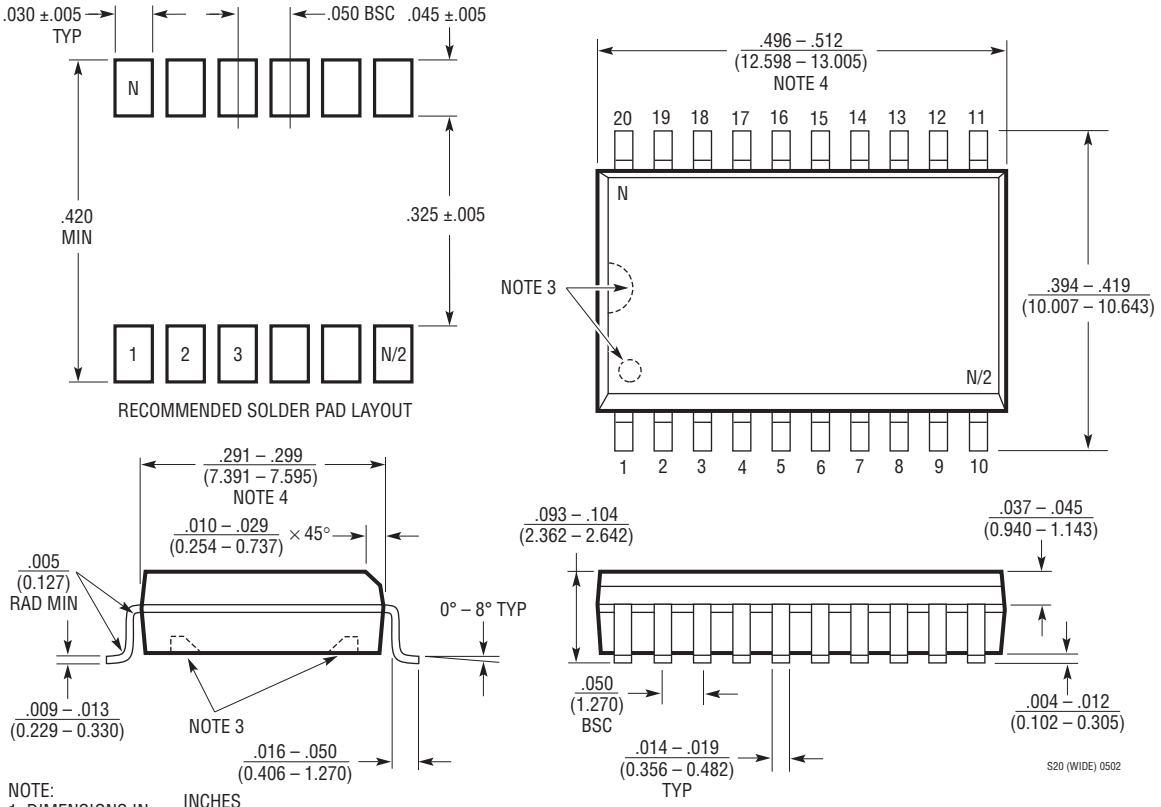


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2966#packaging for the most recent package drawings.

SW Package
20-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/15	Fixed typos	1, 3, 10, 11, 12, 15
B	03/16	Added ABS Max Rating for INHA, INHB, INLA and INLB pins	2
C	08/17	Corrected example error threshold calculations	12

TYPICAL APPLICATION

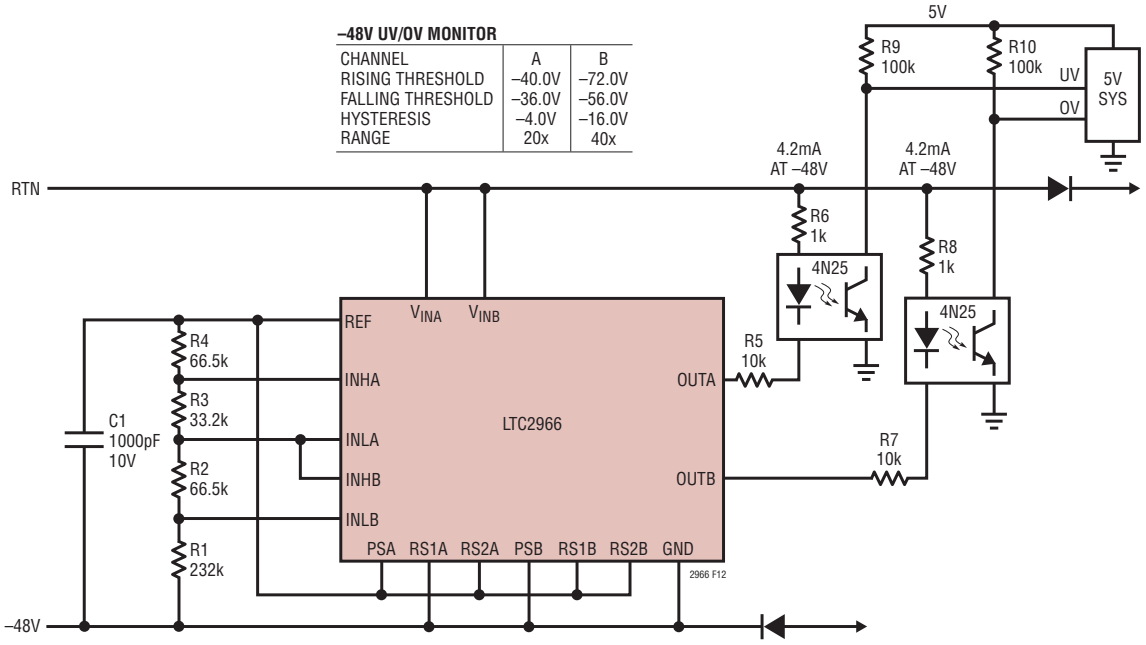


Figure 12. Monitoring Negative Voltage with Isolation

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1326	Micropower Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%) and ADJ
LTC1440/LTC1441/ LTC1442	Ultralow Power Single/Dual Comparator with Reference	Adjustable Hysteresis, 3mm × 3mm × 0.75mm DFN Package
LTC1726/LTC1727/ LTC1728	Micropower Triple Supply Monitor	Adjustable Reset and Watchdog Timeouts
LTC1985	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900/LTC2901/ LTC2902	Programmable Quad Supply Monitor	Adjustable Reset, Watchdog Timer and Tolerance, 10-Lead MSOP and DFN Packages
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 and DFN Packages
LTC2904/LTC2905/ LTC2906/LTC2907	Three-State Programmable Precision Dual Supply Monitor	8-Lead SOT-23 and DFN Packages
LTC2908	Precision Six-Supply Monitor (Four Fixed and Two Adjustable)	8-Lead TSOT-23 and DFN Packages
LTC2909/LTC2919	Precision Triple/Dual Input UV, OV and Negative Voltage Monitor	Shunt Regulated V_{CC} Pin, Adjustable Threshold and Reset
LTC2910	Octal Positive/Negative Voltage Monitor	Separate V_{CC} Pin, Eight Inputs, Up to Two Negative Monitors Adjustable Reset Timer, 16-Lead SSOP and DFN Packages
LTC2912/LTC2913/ LTC2914	Single/Dual/Quad UV and OV Voltage Monitors	Separate V_{CC} Pin, Adjustable Reset Timer
LTC2915/LTC2916/ LTC2917/LTC2918	Single Voltage Supervisors with 27 Pin-Selectable Thresholds	Manual Reset and Watchdog Functions, 8- and 10-Lead TSOT-23, MSOP and DFN Packages
LTC2965	100V Micropower Single Voltage Monitor	3.5V to 98V Monitoring Range, 3.5V to 100V Operating Range, 7µA Quiescent Current
LTC2960	36V Nano-Current Two Input Voltage Monitor	36V, 850nA Quiescent Current, 2mm × 2mm 8-Lead DFN and TSOT-23 Packages
LT6700	Micropower Dual Comparator with 400mV Reference	SOT-23, 2mm × 3mm DFN Package

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