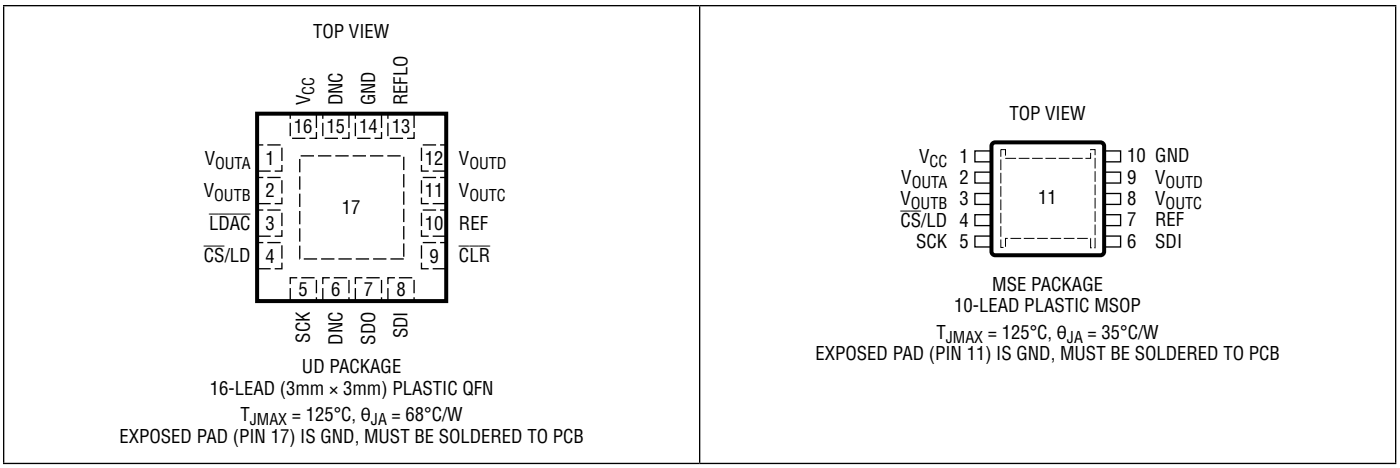
## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage ($V_{CC}$) ..... –0.3V to 6V
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, SDO, REFLO .. –0.3V to 6V
$V_{OUTA}$-$V_{OUTD}$ ..... –0.3V to Min ($V_{CC}$ + 0.3V, 6V)
REF ..... –0.3V to Min ($V_{CC}$ + 0.3V, 6V)
Operating Temperature Range
LTC2634C ..... 0°C to 70°C
LTC2634I ..... –40°C to 85°C
LTC2634H (Note 3) ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

## PIN CONFIGURATION




UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 68°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

MSE PACKAGE
10-LEAD PLASTIC MSOP
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 35°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION http://www.linear.com/product/LTC2634#orderinfo

**LTC2634 C UD -L Z 12 #TR PBF**

**LEAD FREE DESIGNATOR**
PBF = Lead Free

**TAPE AND REEL**
TR = 2,500-Piece Tape and Reel

**RESOLUTION**
12 = 12-Bit
10 = 10-Bit
8 = 8-Bit

**POWER-ON RESET**
MI = Reset to Mid-Scale in Internal Reference Mode
MX = Reset to Mid-Scale in External Reference Mode
Z = Reset to Zero-Scale in Internal Reference Mode

**FULL-SCALE VOLTAGE, INTERNAL REFERENCE MODE**
L = 2.5V
H = 4.096V

**PACKAGE TYPE**
UD = 16-Lead QFN
MSE = 10-Lead MSOP

**TEMPERATURE GRADE**
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)
H = Automotive Temperature Range (–40°C to 125°C)

**PRODUCT PART NUMBER**

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/ Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

# PRODUCT SELECTION GUIDE

| PART NUMBER | PART MARKING* QFN | PART MARKING* MSOP | $V_{FS}$ WITH INTERNAL REFERENCE | POWER-ON RESET TO CODE | POWER-ON REFERENCE MODE | RESOLUTION | $V_{CC}$ | MAXIMUM INL |
|---|---|---|---|---|---|---|---|---|
| LTC2634-LMI12 | LDQX | LTDRV | 2.5V • (4095/4096) | Mid-Scale | Internal | 12-Bit | 2.7V to 5.5V | ±2.5LSB |
| LTC2634-LMI10 | LDRF | LTDSC | 2.5V • (1023/1024) | Mid-Scale | Internal | 10-Bit | 2.7V to 5.5V | ±1LSB |
| LTC2634-LMI8 | LDRN | LTDSK | 2.5V • (255/256) | Mid-Scale | Internal | 8-Bit | 2.7V to 5.5V | ±0.5LSB |
| LTC2634-LMX12 | LDQW | LTDRT | 2.5V • (4095/4096) | Mid-Scale | External | 12-Bit | 2.7V to 5.5V | ±2.5LSB |
| LTC2634-LMX10 | LDRD | LTDSB | 2.5V • (1023/1024) | Mid-Scale | External | 10-Bit | 2.7V to 5.5V | ±1LSB |
| LTC2634-LMX8 | LDRM | LTDSJ | 2.5V • (255/256) | Mid-Scale | External | 8-Bit | 2.7V to 5.5V | ±0.5LSB |
| LTC2634-LZ12 | LDQV | LTDRS | 2.5V • (4095/4096) | Zero-Scale | Internal | 12-Bit | 2.7V to 5.5V | ±2.5LSB |
| LTC2634-LZ10 | LDRC | LTDRZ | 2.5V • (1023/1024) | Zero-Scale | Internal | 10-Bit | 2.7V to 5.5V | ±1LSB |
| LTC2634-LZ8 | LDRK | LTDSH | 2.5V • (255/256) | Zero-Scale | Internal | 8-Bit | 2.7V to 5.5V | ±0.5LSB |
| LTC2634-HMI12 | LDRB | LTDRY | 4.096V • (4095/4096) | Mid-Scale | Internal | 12-Bit | 4.5V to 5.5V | ±2.5LSB |
| LTC2634-HMI10 | LDRJ | LTDSG | 4.096V • (1023/1024) | Mid-Scale | Internal | 10-Bit | 4.5V to 5.5V | ±1LSB |
| LTC2634-HMI8 | LDRR | LTDSP | 4.096V • (255/256) | Mid-Scale | Internal | 8-Bit | 4.5V to 5.5V | ±0.5LSB |
| LTC2634-HMX12 | LDQZ | LTDRX | 4.096V • (4095/4096) | Mid-Scale | External | 12-Bit | 4.5V to 5.5V | ±2.5LSB |
| LTC2634-HMX10 | LDRH | LTDSF | 4.096V • (1023/1024) | Mid-Scale | External | 10-Bit | 4.5V to 5.5V | ±1LSB |
| LTC2634-HMX8 | LDRQ | LTDSN | 4.096V • (255/256) | Mid-Scale | External | 8-Bit | 4.5V to 5.5V | ±0.5LSB |
| LTC2634-HZ12 | LDQY | LTDRW | 4.096V • (4095/4096) | Zero-Scale | Internal | 12-Bit | 4.5V to 5.5V | ±2.5LSB |
| LTC2634-HZ10 | LDRG | LTDSD | 4.096V • (1023/1024) | Zero-Scale | Internal | 10-Bit | 4.5V to 5.5V | ±1LSB |
| LTC2634-HZ8 | LDRP | LTDSM | 4.096V • (255/256) | Zero-Scale | Internal | 8-Bit | 4.5V to 5.5V | ±0.5LSB |

*Above options are available in a 16-lead QFN package (LTC2634-UD) or 10-lead MSOP package (LTC2634-MSE).

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2634-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8 ($V_{FS}$ = 2.5V)**

| SYMBOL | PARAMETER | CONDITIONS | | LTC2634-8 MIN | LTC2634-8 TYP | LTC2634-8 MAX | LTC2634-10 MIN | LTC2634-10 TYP | LTC2634-10 MAX | LTC2634-12 MIN | LTC2634-12 TYP | LTC2634-12 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DC Performance** | | | | | | | | | | | | | |
| | Resolution | | ● | 8 | | | 10 | | | 12 | | | Bits |
| | Monotonicity | $V_{CC}$ = 3V, Internal Ref. (Note 4) | ● | 8 | | | 10 | | | 12 | | | Bits |
| DNL | Differential Nonlinearity | $V_{CC}$ = 3V, Internal Ref. (Note 4) | ● | | | ±0.5 | | | ±0.5 | | | ±1 | LSB |
| INL | Integral Nonlinearity | $V_{CC}$ = 3V, Internal Ref. (Note 4) | ● | | ±0.05 | ±0.5 | | ±0.2 | ±1 | | ±1 | ±2.5 | LSB |
| ZSE | Zero-Scale Error | $V_{CC}$ = 3V, Internal Ref., Code = 0 | ● | | 0.5 | 5 | | 0.5 | 5 | | 0.5 | 5 | mV |
| $V_{OS}$ | Offset Error | $V_{CC}$ = 3V, Internal Ref. (Note 5) | ● | | ±0.5 | ±5 | | ±0.5 | ±5 | | ±0.5 | ±5 | mV |
| $V_{OSTC}$ | $V_{OS}$ Temperature Coefficient | $V_{CC}$ = 3V, Internal Ref. | | | ±10 | | | ±10 | | | ±10 | | µV/°C |
| GE | Gain Error | $V_{CC}$ = 3V, Internal Ref. | ● | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | %FSR |
| $GE_{TC}$ | Gain Temperature Coefficient | $V_{CC}$ = 3V, Internal Ref. (Note 10)<br>C-Grade<br>I-Grade<br>H-Grade | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | <br>ppm/°C<br>ppm/°C<br>ppm/°C |
| | Load Regulation | Internal Ref., Mid-Scale<br>$V_{CC}$ = 3V ±10%, –5mA ≤ $I_{OUT}$ ≤ 5mA | ● | | 0.009 | 0.016 | | 0.035 | 0.064 | | 0.14 | 0.256 | LSB/mA |
| | | Internal Ref., Mid-Scale<br>$V_{CC}$ = 5V ±10%, –10mA ≤ $I_{OUT}$ ≤ 10mA | ● | | 0.009 | 0.016 | | 0.035 | 0.064 | | 0.14 | 0.256 | LSB/mA |
| $R_{OUT}$ | DC Output Impedance | Internal Ref., Mid-Scale<br>$V_{CC}$ = 3V ±10%, –5mA ≤ $I_{OUT}$ ≤ 5mA | ● | | 0.09 | 0.156 | | 0.09 | 0.156 | | 0.09 | 0.156 | Ω |
| | | Internal Ref., Mid-Scale<br>$V_{CC}$ = 5V ±10%, –10mA ≤ $I_{OUT}$ ≤ 10mA | ● | | 0.09 | 0.156 | | 0.09 | 0.156 | | 0.09 | 0.156 | Ω |

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | DAC Output Span | External Reference<br>Internal Reference | | | 0 to $V_{REF}$<br>0 to 2.5 | | V<br>V |
| PSR | Power Supply Rejection | $V_{CC}$ = 3V ±10% or 5V ±10% | | | –80 | | dB |
| $I_{SC}$ | Short-Circuit Output Current (Note 6)<br>Sinking<br>Sourcing | $V_{FS}$ = $V_{CC}$ = 5.5V<br>Zero-Scale; $V_{OUT}$ Shorted to $V_{CC}$<br>Full-Scale; $V_{OUT}$ Shorted to GND | <br>●<br>● | | <br>27<br>–27 | <br>48<br>–48 | <br>mA<br>mA |
| **Power Supply** | | | | | | | |
| $V_{CC}$ | Positive Supply Voltage | For Specified Performance | ● | 2.7 | | 5.5 | V |
| $I_{CC}$ | Supply Current (Note 7) | $V_{CC}$ = 3V, $V_{REF}$ = 2.5V, External Reference<br>$V_{CC}$ = 3V, Internal Reference<br>$V_{CC}$ = 5V $V_{REF}$ = 2.5V, External Reference<br>$V_{CC}$ = 5V, Internal Reference | ●<br>●<br>●<br>● | | 0.5<br>0.6<br>0.6<br>0.7 | 0.7<br>0.8<br>0.8<br>0.9 | mA<br>mA<br>mA<br>mA |
| $I_{SD}$ | Supply Current in Power-Down Mode (Note 7) | $V_{CC}$ = 5V, C-Grade, I-Grade<br>$V_{CC}$ = 5V, H-Grade | ●<br>● | | 0.5<br>0.5 | 20<br>30 | µA<br>µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2634-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8 ($V_{FS}$ = 2.5V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Reference Input** | | | | | | | |
| $V_{REF}$ | Input Voltage Range | | ● | 1 | | $V_{CC}$ | V |
| | Resistance | | ● | 120 | 160 | 200 | kΩ |
| | Capacitance | | | | 14 | | pF |
| $I_{REF}$ | Reference Current, Power-Down Mode | DAC Powered Down | ● | | 0.005 | 1.5 | µA |
| **Reference Output** | | | | | | | |
| | Output Voltage | | ● | 1.24 | 1.25 | 1.26 | V |
| | Reference Temperature Coefficient | | | | ±10 | | ppm/°C |
| | Output Impedance | | | | 0.5 | | kΩ |
| | Capacitive Load Driving | | | | 10 | | µF |
| | Short-Circuit Current | $V_{CC}$ = 5.5V, REF Shorted to GND | | | 2.5 | | mA |
| **Digital I/O** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | $V_{CC}$ = 3.6V to 5.5V<br>$V_{CC}$ = 2.7V to 3.6V | ●<br>● | 2.4<br>2.0 | | | V<br>V |
| $V_{IL}$ | Digital Input Low Voltage | $V_{CC}$ = 4.5V to 5.5V<br>$V_{CC}$ = 2.7V to 4.5V | ●<br>● | | | 0.8<br>0.6 | V<br>V |
| $V_{OH}$ | Digital Output High Voltage | Load Current = –100µA | ● | $V_{CC}$ – 0.4 | | | V |
| $V_{OL}$ | Digital Output Low Voltage | Load Current = 100µA | ● | | | 0.4 | V |
| $I_{LK}$ | Digital Input Leakage | $V_{IN}$ = GND to $V_{CC}$ | ● | | | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 8) | ● | | | 2.5 | pF |
| **AC Performance** | | | | | | | |
| $t_S$ | Settling Time | $V_{CC}$ = 3V (Note 9)<br>±0.39% (±1LSB at 8 Bits)<br>±0.098% (±1LSB at 10 Bits)<br>±0.024% (±1LSB at 12 Bits) | | | <br>3.3<br>3.8<br>4.2 | | <br>µs<br>µs<br>µs |
| | Voltage Output Slew Rate | | | | 1.0 | | V/µs |
| | Capacitive Load Driving | | | | 500 | | pF |
| | Glitch Impulse | At Mid-Scale Transition | | | 2.1 | | nV•s |
| | DAC-to-DAC Crosstalk | 1 DAC Held at FS, 1 DAC Switch 0 – FS | | | 2.1 | | nV•s |
| | Multiplying Bandwidth | External Reference | | | 320 | | kHz |
| $e_n$ | Output Voltage Noise Density | At f = 1kHz, External Reference<br>At f = 10kHz, External Reference<br>At f = 1kHz, Internal Reference<br>At f = 10kHz, Internal Reference | | | 180<br>160<br>200<br>180 | | nV/√Hz<br>nV/√Hz<br>nV/√Hz<br>nV/√Hz |
| | Output Voltage Noise | 0.1Hz to 10Hz, External Reference<br>0.1Hz to 10Hz, Internal Reference<br>0.1Hz to 200kHz, External Reference<br>0.1Hz to 200kHz, Internal Reference<br>$C_{REF}$ = 0.1µF | | | 35<br>40<br>680<br>730 | | $µV_{P-P}$<br>$µV_{P-P}$<br>$µV_{P-P}$<br>$µV_{P-P}$ |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2634-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8 ($V_{FS}$ = 2.5V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_1$ | SDI Valid to SCK Setup | | ● | 4 | | | ns |
| $t_2$ | SDI Valid to SCK Hold | | ● | 4 | | | ns |
| $t_3$ | SCK High Time | | ● | 9 | | | ns |
| $t_4$ | SCK Low Time | | ● | 9 | | | ns |
| $t_5$ | $\overline{CS}$/LD Pulse Width | | ● | 10 | | | ns |
| $t_6$ | LSB SCK High to $\overline{CS}$/LD High | | ● | 7 | | | ns |
| $t_7$ | $\overline{CS}$/LD Low to SCK High | | ● | 7 | | | ns |
| $t_8$ | $\overline{CLR}$ Pulse Width | | ● | 20 | | | ns |
| $t_9$ | $\overline{LDAC}$ Pulse Width | | ● | 15 | | | ns |
| $t_{10}$ | $\overline{CS}$/LD High to SCK Positive Edge | | ● | 7 | | | ns |
| | SCK Frequency | 50% Duty Cycle | ● | | | 50 | MHz |
| $t_{11}$ | $\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition | | ● | 200 | | | ns |
| $t_{12}$ | SDO Propagation Delay from SCK Falling Edge | $C_{LOAD}$ = 10pF | | | | | |
| | | $V_{CC}$ = 4.5V to 5.5V | ● | | | 20 | ns |
| | | $V_{CC}$ = 2.7V to 5.5V | ● | | | 45 | ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2634-HMI12/-HMI10/-HMI8/-HMX12/-HMX10/-HMX8/-HZ12/-HZ10/-HZ8 ($V_{FS}$ = 4.096V)**

| SYMBOL | PARAMETER | CONDITIONS | | LTC2634-8 MIN | LTC2634-8 TYP | LTC2634-8 MAX | LTC2634-10 MIN | LTC2634-10 TYP | LTC2634-10 MAX | LTC2634-12 MIN | LTC2634-12 TYP | LTC2634-12 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DC Performance** | | | | | | | | | | | | | |
| | Resolution | | ● | 8 | | | 10 | | | 12 | | | Bits |
| | Monotonicity | $V_{CC}$ = 5V, Internal Ref. (Note 4) | ● | 8 | | | 10 | | | 12 | | | Bits |
| DNL | Differential Nonlinearity | $V_{CC}$ = 5V, Internal Ref. (Note 4) | ● | | | ±0.5 | | | ±0.5 | | | ±1 | LSB |
| INL | Integral Nonlinearity | $V_{CC}$ = 5V, Internal Ref. (Note 4) | ● | | ±0.05 | ±0.5 | | ±0.2 | ±1 | | ±1 | ±2.5 | LSB |
| ZSE | Zero-Scale Error | $V_{CC}$ = 5V, Internal Ref., Code = 0 | ● | | 0.5 | 5 | | 0.5 | 5 | | 0.5 | 5 | mV |
| $V_{OS}$ | Offset Error | $V_{CC}$ = 5V, Internal Ref. (Note 5) | ● | | ±0.5 | ±5 | | ±0.5 | ±5 | | ±0.5 | ±5 | mV |
| $V_{OSTC}$ | $V_{OS}$ Temperature Coefficient | $V_{CC}$ = 5V, Internal Ref. | | | ±10 | | | ±10 | | | ±10 | | µV/°C |
| GE | Gain Error | $V_{CC}$ = 5V, Internal Ref. | ● | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | %FSR |
| $GE_{TC}$ | Gain Temperature Coefficient | $V_{CC}$ = 5V, Internal Ref. (Note 10)<br>C-Grade<br>I-Grade<br>H-Grade | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | <br>ppm/°C<br>ppm/°C<br>ppm/°C |
| | Load Regulation | $V_{CC}$ = 5V ±10%, Internal Ref., Mid-Scale, –10mA ≤ $I_{OUT}$ ≤ 10mA | ● | | 0.006 | 0.01 | | 0.022 | 0.04 | | 0.09 | 0.16 | LSB/mA |
| $R_{OUT}$ | DC Output Impedance | $V_{CC}$ = 5V ±10%, Internal Ref., Mid-Scale, –10mA ≤ $I_{OUT}$ ≤ 10mA | ● | | 0.09 | 0.156 | | 0.09 | 0.156 | | 0.09 | 0.156 | Ω |

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | DAC Output Span | External Reference<br>Internal Reference | | | 0 to $V_{REF}$<br>0 to 4.096 | | V<br>V |
| PSR | Power Supply Rejection | $V_{CC}$ = 5V ±10% | | | –80 | | dB |
| $I_{SC}$ | Short-Circuit Output Current (Note 6)<br>Sinking<br>Sourcing | $V_{FS}$ = $V_{CC}$ = 5.5V<br>Zero-Scale; $V_{OUT}$ Shorted to $V_{CC}$<br>Full-Scale; $V_{OUT}$ Shorted to GND | <br>●<br>● | | <br>27<br>–27 | <br>48<br>–48 | <br>mA<br>mA |
| **Power Supply** | | | | | | | |
| $V_{CC}$ | Positive Supply Voltage | For Specified Performance | ● | 4.5 | | 5.5 | V |
| $I_{CC}$ | Supply Current (Note 7) | $V_{CC}$ = 5V, $V_{REF}$ = 4.096V, External Reference<br>$V_{CC}$ = 5V, Internal Reference | ●<br>● | | 0.6<br>0.7 | 0.8<br>0.9 | mA<br>mA |
| $I_{SD}$ | Supply Current in Power-Down Mode (Note 7) | $V_{CC}$ = 5V, C-Grade, I-Grade<br>$V_{CC}$ = 5V, H-Grade | ●<br>● | | 0.5<br>0.5 | 20<br>30 | µA<br>µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2634-HMI12/-HMI10/-HMI8/-HMX12/-HMX10/-HMX8/-HZ12/-HZ10/-HZ8 ($V_{FS}$ = 4.096V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Reference Input** | | | | | | | |
| $V_{REF}$ | Input Voltage Range | | ● | 1 | | $V_{CC}$ | V |
| | Resistance | | ● | 120 | 160 | 200 | kΩ |
| | Capacitance | | | | 14 | | pF |
| $I_{REF}$ | Reference Current, Power-Down Mode | DAC Powered Down | ● | | 0.005 | 1.5 | µA |
| **Reference Output** | | | | | | | |
| | Output Voltage | | ● | 2.032 | 2.048 | 2.064 | V |
| | Reference Temperature Coefficient | | | | ±10 | | ppm/°C |
| | Output Impedance | | | | 0.5 | | kΩ |
| | Capacitive Load Driving | | | | 10 | | µF |
| | Short-Circuit Current | $V_{CC}$ = 5.5V, REF Shorted to GND | | | 4 | | mA |
| **Digital I/O** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | | ● | 2.4 | | | V |
| $V_{IL}$ | Digital Input Low Voltage | | ● | | | 0.8 | V |
| $V_{OH}$ | Digital Output High Voltage | Load Current = –100µA | ● | $V_{CC}$ – 0.4 | | | V |
| $V_{OL}$ | Digital Output Low Voltage | Load Current = 100µA | ● | | | 0.4 | V |
| $I_{LK}$ | Digital Input Leakage | $V_{IN}$ = GND to $V_{CC}$ | ● | | | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 8) | ● | | | 2.5 | pF |
| **AC Performance** | | | | | | | |
| $t_S$ | Settling Time | $V_{CC}$ = 5V (Note 9)<br>±0.39% (±1LSB at 8 Bits)<br>±0.098% (±1LSB at 10 Bits)<br>±0.024% (±1LSB at 12 Bits) | | | <br>3.8<br>4.2<br>4.8 | | <br>µs<br>µs<br>µs |
| | Voltage Output Slew Rate | | | | 1.0 | | V/µs |
| | Capacitive Load Driving | | | | 500 | | pF |
| | Glitch Impulse | At Mid-Scale Transition | | | 3.0 | | nV•s |
| | DAC-to-DAC Crosstalk | 1 DAC Held at FS, 1 DAC Switch 0 – FS | | | 2.4 | | nV•s |
| | Multiplying Bandwidth | External Reference | | | 320 | | kHz |
| $e_n$ | Output Voltage Noise Density | At f = 1kHz, External Reference<br>At f = 10kHz, External Reference<br>At f = 1kHz, Internal Reference<br>At f = 10kHz, Internal Reference | | | 180<br>160<br>250<br>230 | | nV/√Hz<br>nV/√Hz<br>nV/√Hz<br>nV/√Hz |
| | Output Voltage Noise | 0.1Hz to 10Hz, External Reference<br>0.1Hz to 10Hz, Internal Reference<br>0.1Hz to 200kHz, External Reference<br>0.1Hz to 200kHz, Internal Reference<br>$C_{REF}$ = 0.1µF | | | 35<br>50<br>680<br>750 | | $\mu V_{P-P}$<br>$\mu V_{P-P}$<br>$\mu V_{P-P}$<br>$\mu V_{P-P}$ |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2634-HMI12/-HMI10/-HMI8/-HMX12/-HMX10/-HMX8/-HZ12/-HZ10/-HZ8 ($V_{FS}$ = 4.096V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_1$ | SDI Valid to SCK Setup | | ● | 4 | | | ns |
| $t_2$ | SDI Valid to SCK Hold | | ● | 4 | | | ns |
| $t_3$ | SCK High Time | | ● | 9 | | | ns |
| $t_4$ | SCK Low Time | | ● | 9 | | | ns |
| $t_5$ | $\overline{CS}$/LD Pulse Width | | ● | 10 | | | ns |
| $t_6$ | LSB SCK High to $\overline{CS}$/LD High | | ● | 7 | | | ns |
| $t_7$ | $\overline{CS}$/LD Low to SCK High | | ● | 7 | | | ns |
| $t_8$ | $\overline{CLR}$ Pulse Width | | ● | 20 | | | ns |
| $t_9$ | $\overline{LDAC}$ Pulse Width | | ● | 15 | | | ns |
| $t_{10}$ | $\overline{CS}$/LD High to SCK Positive Edge | | ● | 7 | | | ns |
| | SCK Frequency | 50% Duty Cycle | ● | | | 50 | MHz |
| $t_{11}$ | $\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition | | ● | 200 | | | ns |
| $t_{12}$ | SDO Propagation Delay from SCK Falling Edge | $C_{LOAD}$ = 10pF<br>$V_{CC}$ = 4.5V to 5.5V | ● | | | 20 | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltages are with respect to GND.

**Note 3:** Operating at temperatures above 90°C and with $V_{CC}$ > 4V requires $V_{CC}$ slew rates to be no greater than 73mV/µs.

**Note 4:** Linearity and monotonicity are defined from code $k_L$ to code $2^N - 1$, where N is the resolution and $k_L$ is given by $k_L = 0.016 \bullet (2^N / V_{FS})$, rounded to the nearest whole code. For $V_{FS}$ = 2.5V and N = 12, $k_L$ = 26 and linearity is defined from code 26 to code 4,095. For $V_{FS}$ = 4.096V and N = 12, $k_L$ = 16 and linearity is defined from code 16 to code 4,095.

**Note 5:** Inferred from measurement at code 16 (LTC2634-12), code 4 (LTC2634-10) or code 1 (LTC2634-8), and at full-scale.

**Note 6:** This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 7:** Digital inputs at 0V or $V_{CC}$.

**Note 8:** Guaranteed by design and not production tested.

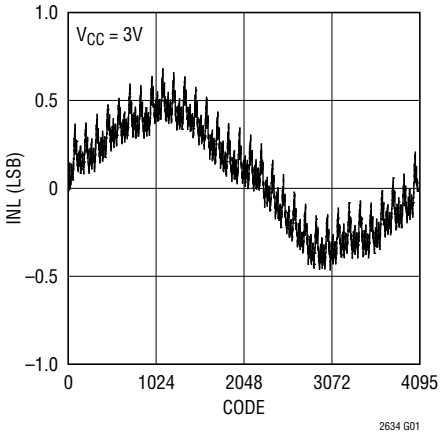
**Note 9:** Internal Reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 100pF to GND.

**Note 10:** Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

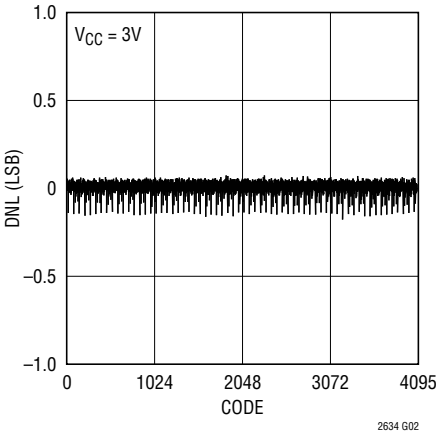
# TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted. LTC2634-L12 (Internal Reference, $V_{FS}$ = 2.5V)**

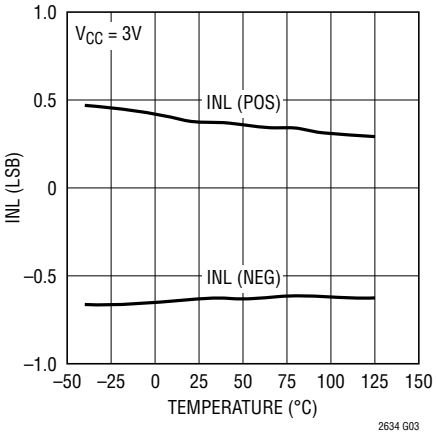
### Integral Nonlinearity (INL)



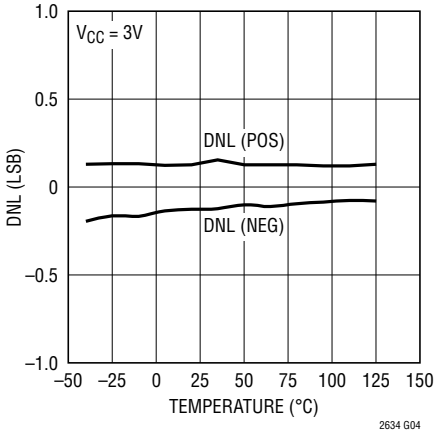

### Differential Nonlinearity (DNL)



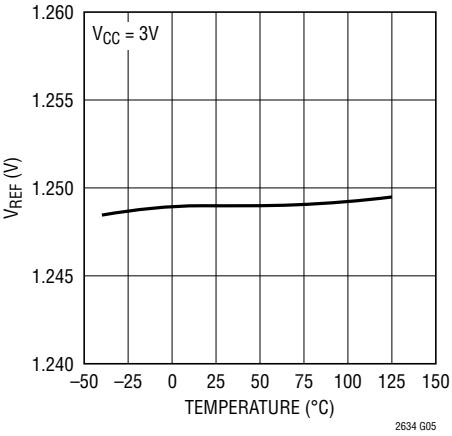

### INL vs Temperature



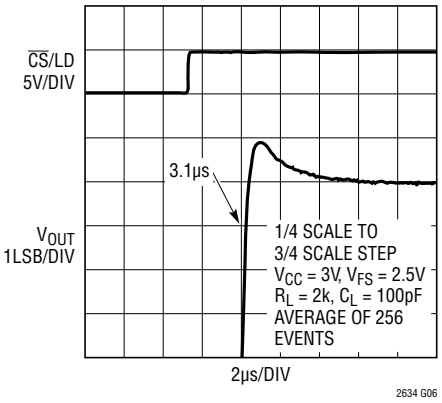

### DNL vs Temperature



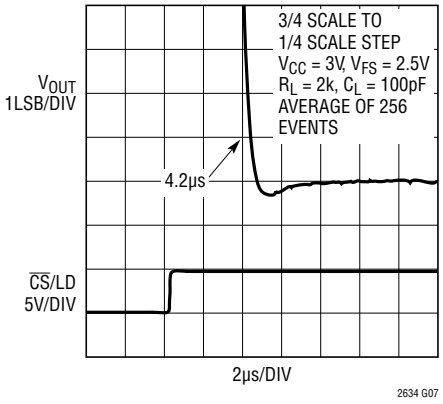

### Reference Output Voltage vs Temperature




### Settling to ±1LSB Rising



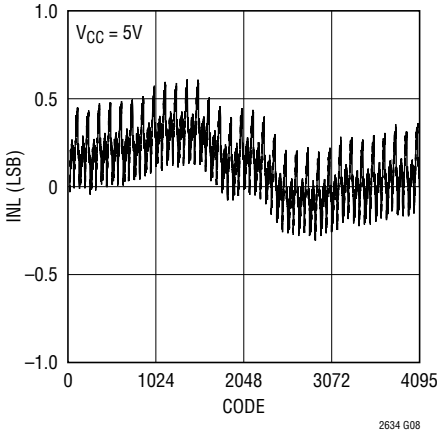

### Settling to ±1LSB Falling



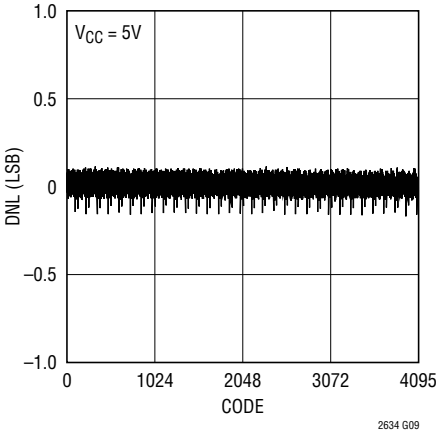
# TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted. LTC2634-H12 (Internal Reference, $V_{FS}$ = 4.096V)**

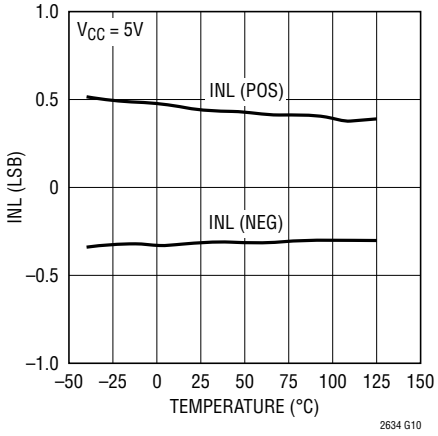
### Integral Nonlinearity (INL)



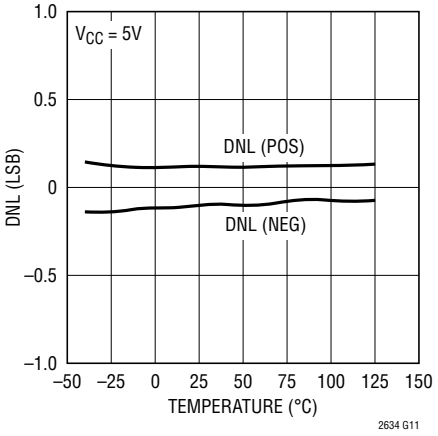

### Differential Nonlinearity (DNL)



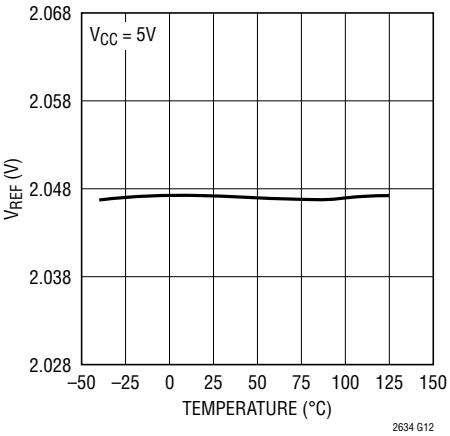

### INL vs Temperature



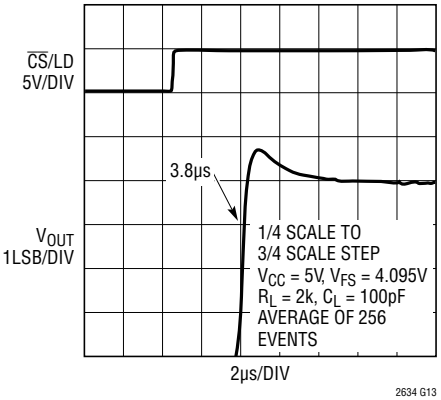

### DNL vs Temperature



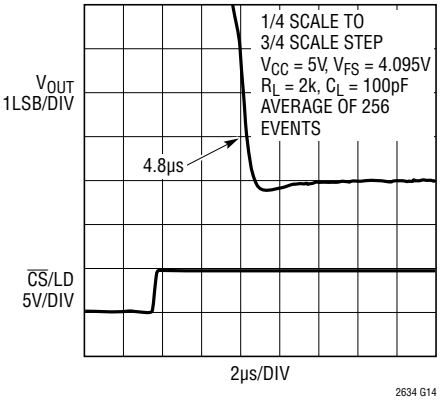

### Reference Output Voltage vs Temperature




### Settling to ±1LSB Rising



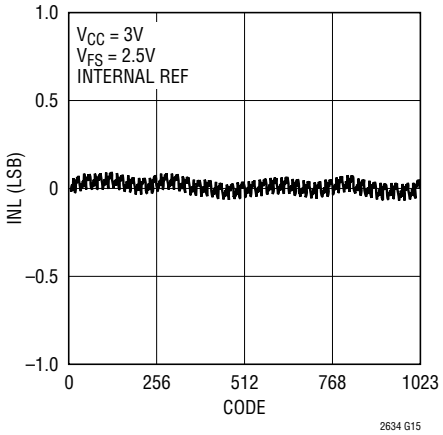

### Settling to ±1LSB Falling



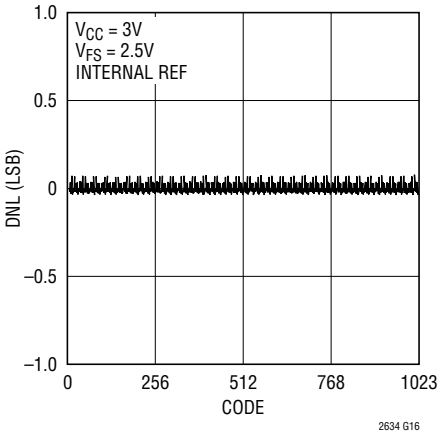
# TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted

## LTC2634-10

### Integral Nonlinearity (INL)

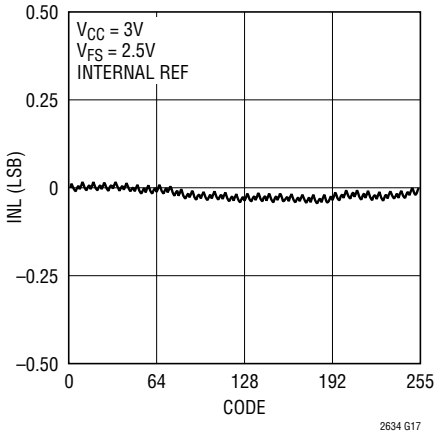



### Differential Nonlinearity (DNL)

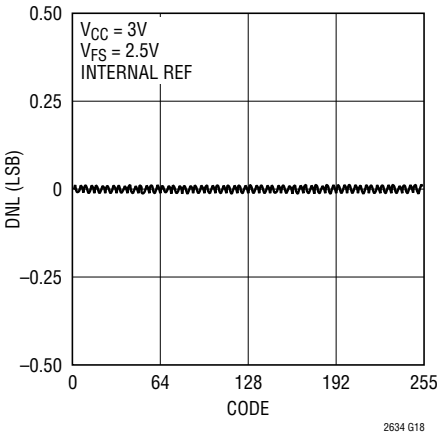



## LTC2634-8

### Integral Nonlinearity (INL)

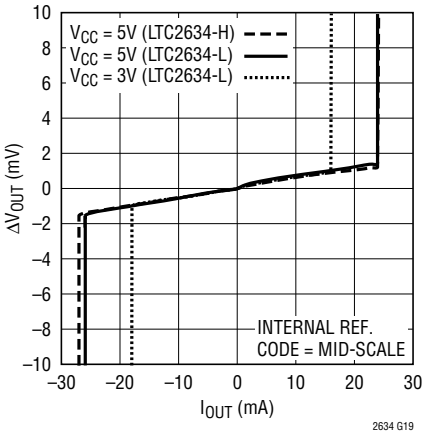



### Differential Nonlinearity (DNL)

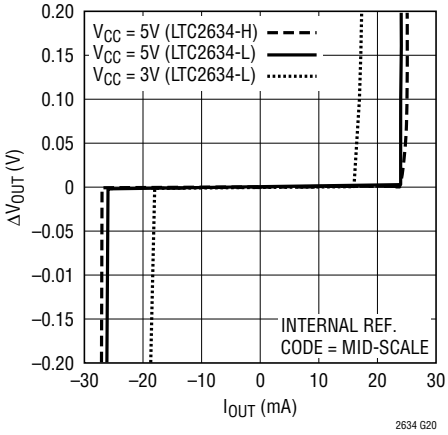



## LTC2634

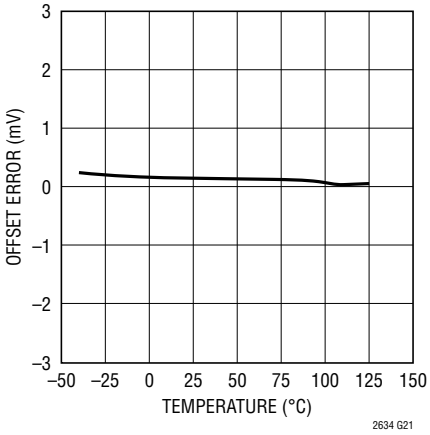
### Load Regulation




### Current Limiting



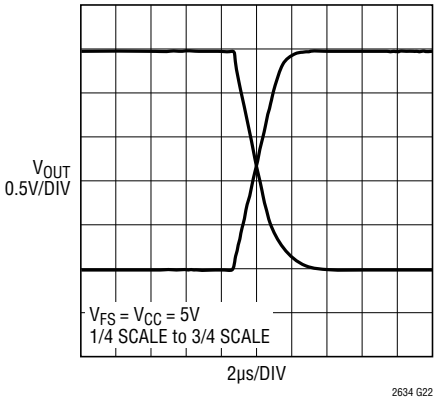

### Offset Error vs Temperature



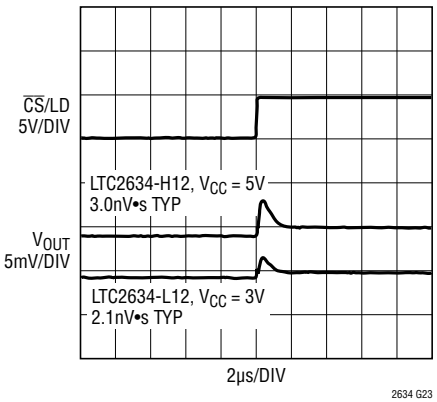
# TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted

**LTC2634**

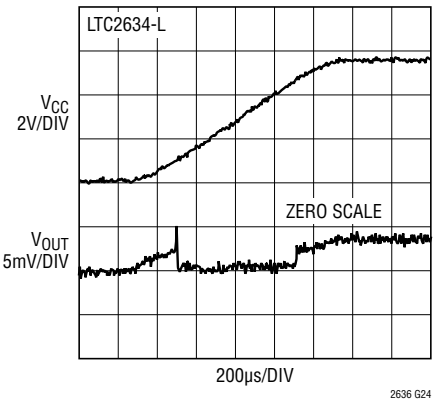
### Large-Signal Response



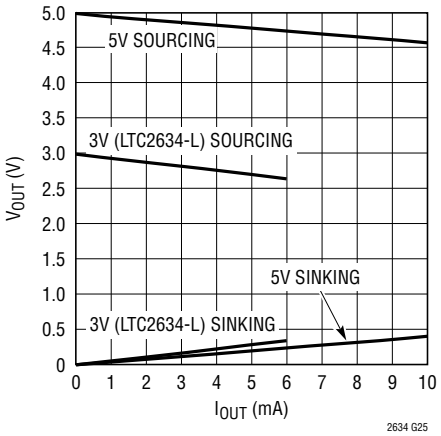

### Mid-Scale Glitch Impulse



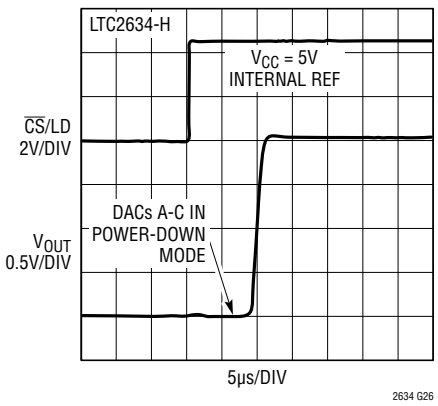

### Power-On Reset Glitch



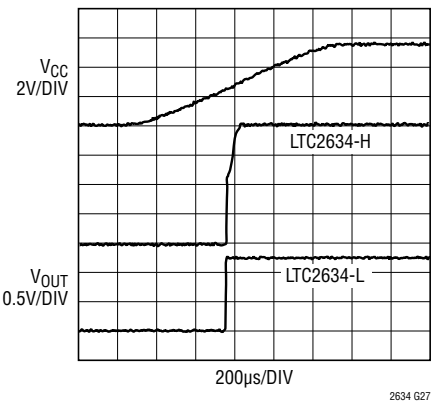

### Headroom at Rails vs Output Current



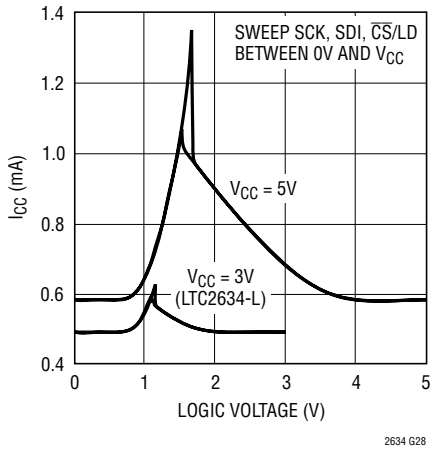

### Exiting Power-Down to Mid-Scale



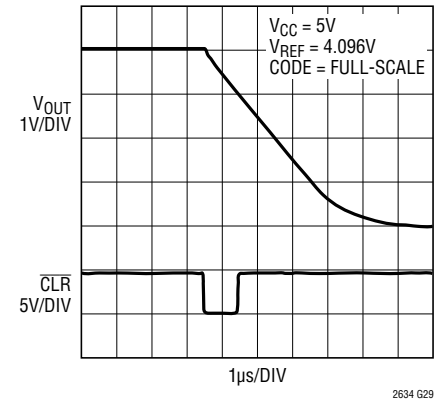

### Power-On Reset to Mid-Scale



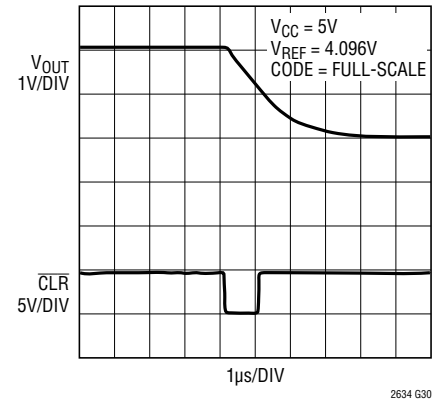

### Supply Current vs Logic Voltage




### Hardware $\overline{CLR}$



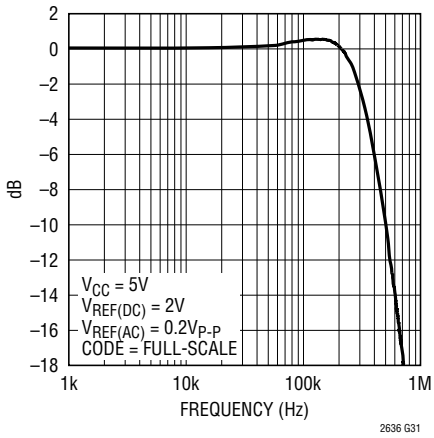

### Hardware $\overline{CLR}$ to Mid-Scale



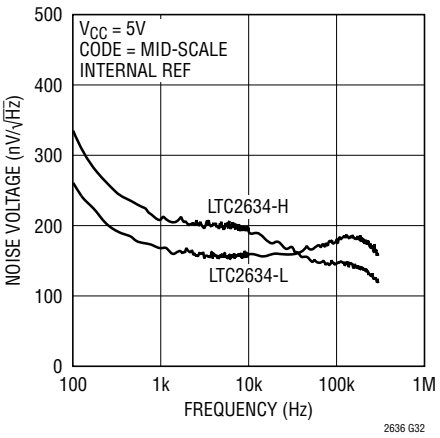
# TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted

**LTC2634**

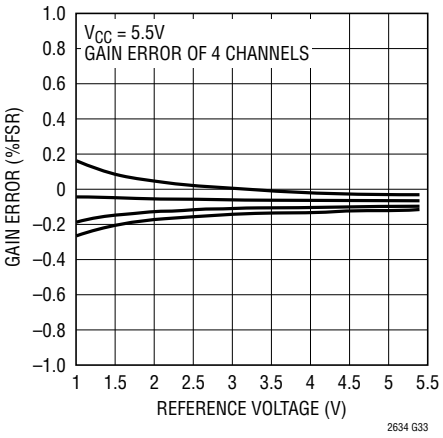
### Mulitplying Bandwidth



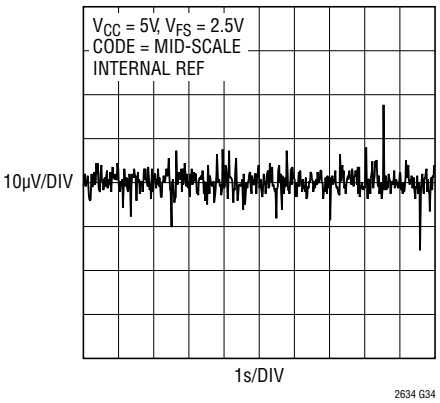

### Noise Voltage vs Frequency



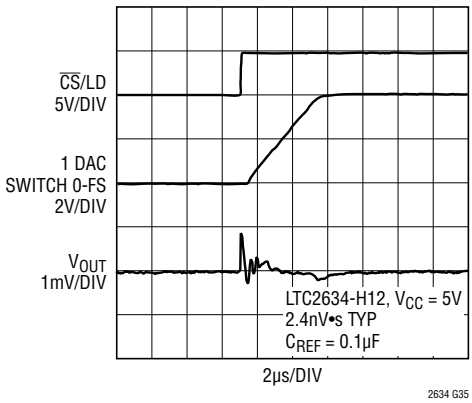

### Gain Error vs Reference Input



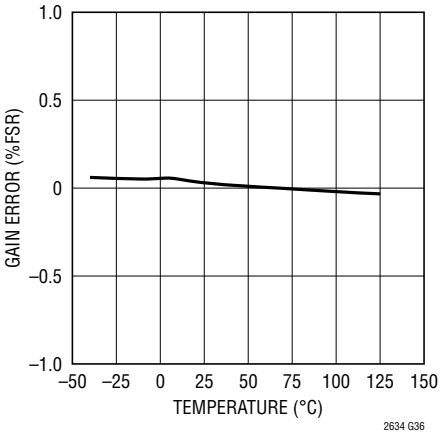

### 0.1Hz to 10Hz Voltage Noise




### DAC-to-DAC Crosstalk (Dynamic)




### Gain Error vs Temperature



## PIN FUNCTIONS (QFN/MSOP)

**$V_{OUTA}$ to $V_{OUTD}$ (Pins 1-2, 11-12/Pins 2-3, 8-9):** DAC Analog Voltage Outputs.

**$\overline{LDAC}$ (Pin 3, QFN Only):** Asynchronous DAC Update Pin. If $\overline{CS}$/LD is high, a falling edge on $\overline{LDAC}$ immediately updates the DAC registers with the contents of the input registers (similar to a software update). If $\overline{CS}$/LD is low when $\overline{LDAC}$ goes low, the DAC registers are updated after $\overline{CS}$/LD returns high. A low on the $\overline{LDAC}$ pin powers up the DACs. A software power-down command is ignored if $\overline{LDAC}$ is low.

**$\overline{CS}$/LD (Pin 4/Pin 4):** Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the 32-bit shift register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

**SCK (Pin 5/Pin 5):** Serial Interface Clock Input. CMOS and TTL compatible.

**DNC (Pins 6, 15, QFN Only):** Do not connect these pins.

**SDO (Pin 7, QFN Only):** Serial Interface Data Output. The serial output of the 32-bit shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. This pin is used for daisy-chain operation, it is always driven and never goes high impedance, even when $\overline{CS}$/LD is high. See the Daisy-Chain Operation section.

**SDI (Pin 8/Pin 6):** Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2634 accepts input word lengths of either 24 or 32 bits.

**$\overline{CLR}$ (Pin 9, QFN Only):** Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage output to reset to zero (LTC2634-Z) or mid-scale (LTC2634-MI/-MX). CMOS and TTL compatible.

**REF (Pin 10/Pin 7):** Reference Voltage Input or Output. When external reference mode is selected, REF is an input ($1V \le V_{REF} \le V_{CC}$) where the voltage supplied sets the full-scale DAC output voltage. When internal reference is selected, the 10ppm/°C 1.25V (LTC2634-L) or 2.048V (LTC2634-H) internal reference (half full-scale) is available at REF. This output may be bypassed to GND with up to 10µF and must be buffered when driving external DC load current.

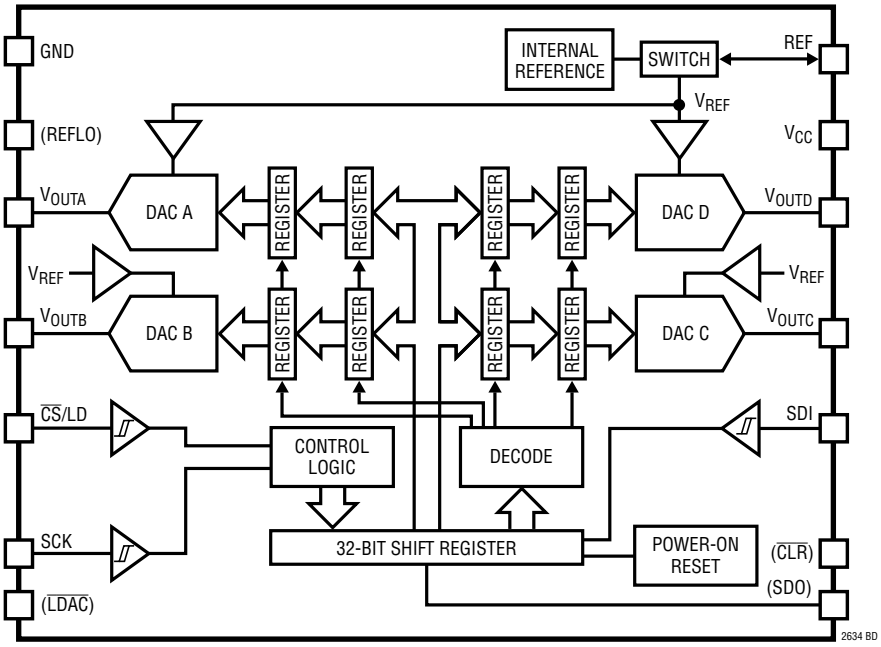
**REFLO (Pin 13, QFN only):** Reference Low Pin. The voltage at this pin sets the zero-scale voltage of all DACs. This pin must be tied to GND.

**GND (Pin 14/Pin 10):** Ground.

**$V_{CC}$ (Pin 16/Pin 1):** Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$ (LTC2634-L) or $4.5V \le V_{CC} \le 5.5V$ (LTC2634-H). Bypass to GND with a 0.1µF capacitor.

**Exposed Pad (Pin 17/Pin 11):** Ground. Must be soldered to PCB ground.

## BLOCK DIAGRAM




( ) QFN PACKAGE ONLY

## TIMING DIAGRAMS

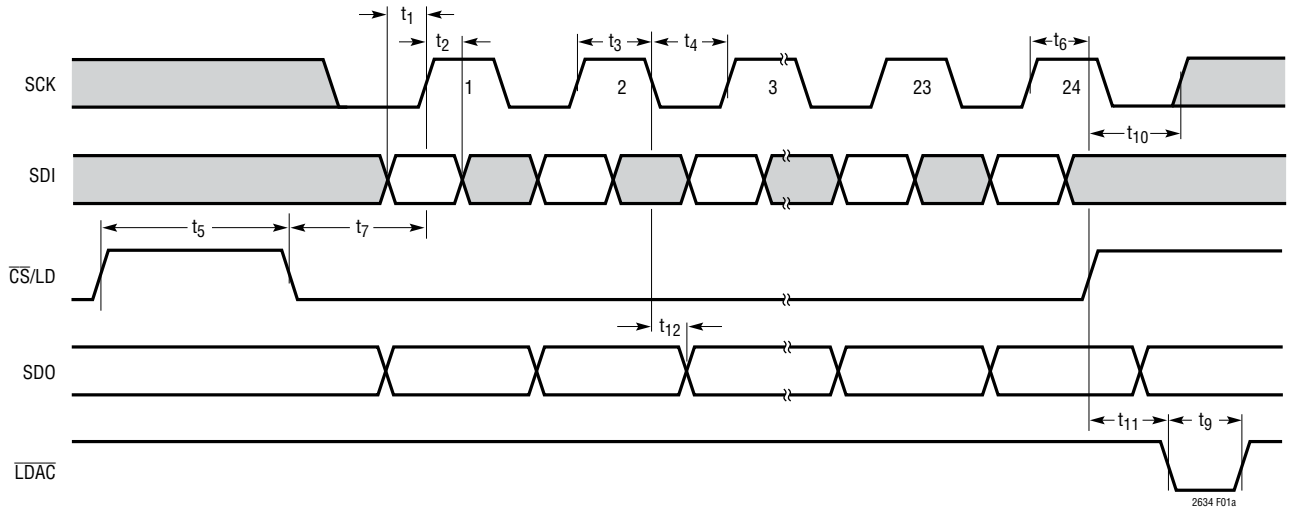



**Figure 1a**

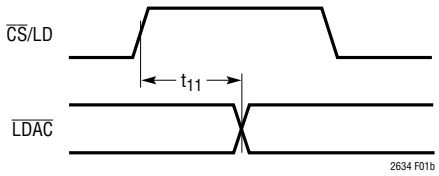



**Figure 1b**

## OPERATION

The LTC2634 is a family of quad voltage output DACs in 16-lead QFN and 10-lead MSOP packages. Each DAC can operate rail-to-rail using an external reference, or with its full-scale voltage set by an integrated reference. Eighteen combinations of accuracy (12-, 10- and 8-bit), power-on reset value (zero-scale, mid-scale in internal reference mode, or mid-scale in external reference mode), and full-scale voltage (2.5V or 4.096V) are available. The LTC2634 is controlled using a 3-wire SPI/MICROWIRE compatible interface.

### Power-On Reset

The LTC2634-HZ/LTC2634-LZ clear the output to zero-scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2634 contains circuitry to reduce the power-on glitch: the analog output typically rises less than 5mV above zero-scale during power on. In general, the glitch amplitude decreases as the power supply ramp time is increased. See “Power-On Reset Glitch” in the Typical Performance Characteristics section.

The LTC2634-HMI/LTC2634-HMX/LTC2634-LMI/LTC2634-LMX provide an alternative reset, setting the output to mid-scale when power is first applied. The LTC2634-LMI and LTC2634-HMI power up in internal reference mode, with the output set to a mid-scale voltage of 1.25V and 2.048V, respectively. The LTC2634-LMX and LTC2634-HMX power up in external reference mode, with the output set to mid-scale of the external reference. Default reference mode selection is described in the Reference Modes section.

### Power Supply Sequencing

The voltage at REF (Pin 10, QFN/Pin 7, MSOP) must be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at $V_{CC}$ is in transition.

### Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)(V_{REF} - V_{REFLO}) + V_{REFLO}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution, and $V_{REF}$ is either 2.5V (LTC2634-LMI/LTC2634-LMX/LTC2634-LZ) or 4.096V (LTC2634-HMI/LTC2634-HMX/LTC2634-HZ) when in internal reference mode, and the voltage at REF when in external reference mode. The resulting DAC output span is 0V to $V_{REF}$, as it is necessary to tie REFLO to GND.

### Serial Interface

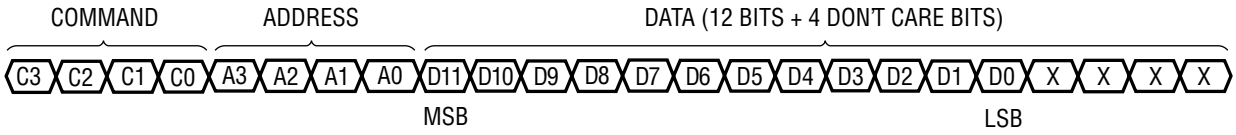
The $\overline{CS}$/LD input is level-triggered. When this input is taken low, it acts as a chip-select signal, enabling the SDI and SCK buffers and the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 12-, 10- or 8-bit input code, ordered MSB to LSB, followed by 4, 6 or 8 don’t-care bits (LTC2634-12/LTC2634-10/LTC2634-8 respectively; see Figure 2). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low, beginning on the first rising edge of SCK. SCK may be high or low at the falling edge

## OPERATION

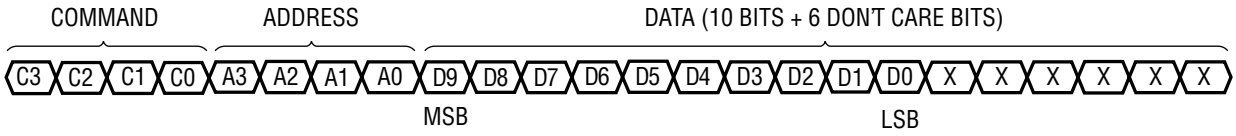
of $\overline{CS}$/LD. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to execute the command specified in the 24-bit input sequence. The complete sequence is shown in Figure 3a.

The command (C3-C0) and address (A3-A0) assignments are shown in Tables 1 and 2. The first four commands in Table 1 consist of write and update operation. A write operation loads a 16-bit data word from the 24-bit shift register into the input register of the selected DAC, n. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 12-, 10- or 8-bit input code, and is converted to an analog voltage at the DAC output. Write to and update combines the first two commands. The update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

**Input Word (LTC2634-12)**




**Input Word (LTC2634-10)**




**Input Word (LTC2634-8)**

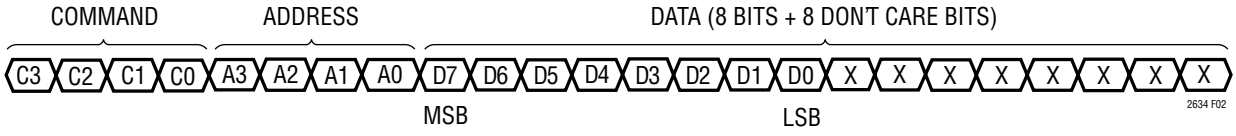



**Figure 2. Command and Data Input Format**

**Table 1. Command Codes**

| COMMAND* | | | | |
|---|---|---|---|---|
| **C3** | **C2** | **C1** | **C0** | |
| 0 | 0 | 0 | 0 | Write to Input Register n |
| 0 | 0 | 0 | 1 | Update (Power Up) DAC Register n |
| 0 | 0 | 1 | 0 | Write to Input Register n, Update (Power Up) All |
| 0 | 0 | 1 | 1 | Write to and Update (Power Up) DAC Register n |
| 0 | 1 | 0 | 0 | Power-Down DAC n |
| 0 | 1 | 0 | 1 | Power-Down Chip (All DACs and Reference) |
| 0 | 1 | 1 | 0 | Select Internal Reference (Power-Up Reference) |
| 0 | 1 | 1 | 1 | Select External Reference (Power-Down Internal Reference) |
| 1 | 1 | 1 | 1 | No Operation |

*Command codes not shown are reserved and should not be used.

**Table 2. Address Codes**

| ADDRESS (n)* | | | | |
|---|---|---|---|---|
| **A3** | **A2** | **A1** | **A0** | |
| 0 | 0 | 0 | 0 | DAC A |
| 0 | 0 | 0 | 1 | DAC B |
| 0 | 0 | 1 | 0 | DAC C |
| 0 | 0 | 1 | 1 | DAC D |
| 1 | 1 | 1 | 1 | All DACs |

* Address codes not shown are reserved and should not be used.

## OPERATION

While the minimum input sequence is 24 bits, it may optionally be extended to 32 bits to accommodate microprocessors that have a minimum word width of 16 bits (2 bytes). To use the 32-bit width, 8 don't care bits must be transferred to the device first, followed by the 24-bit sequence described. Figure 3b shows the 32-bit sequence.

The 16-bit data word is ignored for all commands that do not include a write operation.

### Daisy-Chain Operation (QFN Package)

The serial output of the shift register appears at the SDO pin on the QFN package. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge, therefore, daisy chaining multiple LTC2634 DACs requires 32-bit data write cycles.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a "daisy-chain" series is configured by connecting SDO of each upstream device to SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series. Figure 5 shows a block diagram for daisy-chain operation.

In use, $\overline{CS}$/LD is first taken low. Then the concatenated input data is transferred to the chain, using SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the no-operation command (1111) for the other devices in the chain.

### Reference Modes

For applications where an accurate external reference is either not available, or not desirable due to limited space, the LTC2634 has a low noise, user-selectable, integrated reference. The integrated reference voltage is internally amplified by 2x to provide the full-scale DAC output voltage range. The LTC2634-LMI/LTC2634-LMX/LTC2634-LZ provides a full-scale DAC output of 2.5V. The LTC2634-HMI/LTC2634-HMX/LTC2634-HZ provides a full-scale DAC output of 4.096V. The internal reference can be useful in applications where the supply voltage is poorly regulated. Internal Reference mode can be selected by using command 0110b, and is the power-on default for LTC2634-HZ/LTC2634-LZ, as well as for LTC2634-HMI/LTC2634-LMI.

The 10ppm/°C, 1.25V (LTC2634-LMI/LTC2634-LMX/LTC2634-LZ) or 2.048V (LTC2634-HMI/LTC2634-HMX/LTC2634-HZ) internal reference is available at the REF pin. Adding bypass capacitance to the REF pin will improve noise performance; 0.1µF is recommended, and up to 10µF can be driven without oscillation. The REF output must be buffered when driving an external DC load current.

Alternatively, the DAC can operate in external reference mode using command 0111b. In this mode, an input voltage supplied externally to the REF pin provides the reference ($1V \leq V_{REF} \leq V_{CC}$) and the supply current is reduced. The external reference voltage supplied sets the full-scale DAC output voltage. External reference mode is the power-on default for LTC2634-HMX/LTC2634-LMX.

The reference mode of LTC2634-HZ/LTC2634-LZ/LTC2634-HMI/LTC2634-LMI (internal reference power-on default), can be changed by software command after power up. The same is true for LTC2634-HMX/-LMX (external reference power-on default).

The LTC2634's QFN package offers a REFLO pin for the negative reference. REFLO must be connected to GND.

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### Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than four DAC outputs are needed. When in power down, the buffer amplifiers, bias circuits, and integrated reference circuits are disabled, and draw essentially zero current. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to ground through individual 200k resistors. Input- and DAC-register contents are not disturbed during power down.

Any DAC channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address, (n). The supply current is reduced approximately 20% for each DAC powered down. The integrated reference is automatically powered down when external reference is selected using command 0111b. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using power-down chip command 0101b. When the integrated reference and all DAC channels are in power-down mode, the REF pin becomes high impedance (typically > 1GΩ). For all power-down commands the 16-bit data word is ignored.

Normal operation resumes after executing any command that includes a DAC update, (as shown in Table 1) or pulling the asynchronous $\overline{\text{LDAC}}$ pin low. The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than four DACs are in a powered-down state prior to the update command, the power-up delay time is 10µs. However, if all four DACs and the integrated reference are powered down, then the main bias generation circuit block has been automatically shut down in addition to the DAC amplifiers and reference buffers. In this case, the power-up delay time is 12µs. The power-up of the integrated reference depends on the command that powered it down. If the reference is powered down using the select external reference command (0111b), then it can only be powered back up using select internal reference command (0110b). However, if the reference was powered down using power-down chip command (0101b), then in addition to select internal reference command (0110b), any command (in software or using the $\overline{\text{LDAC}}$ pin) that powers up the DACs will also power up the integrated reference.

### Voltage Output

The LTC2634's integrated rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to ohms. The amplifier's DC output impedance is 0.1Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50Ω typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50Ω • 1mA, or 50mV). See the graph "Headroom at Rails vs Output Current" in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

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### Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit for the lowest codes as shown in Figure 4b. Similarly, limiting can occur near full-scale when the REF pin is tied to $V_{CC}$. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at $V_{CC}$, as shown in Figure 4c. No full-scale limiting can occur if $V_{REF}$ is less than $V_{CC} – FSE$.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

### Board Layout

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2634 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1Ω). Note that the LTC2634 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2634 is sinking large currents, this current flows out the ground pin and directly to the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

## OPERATION

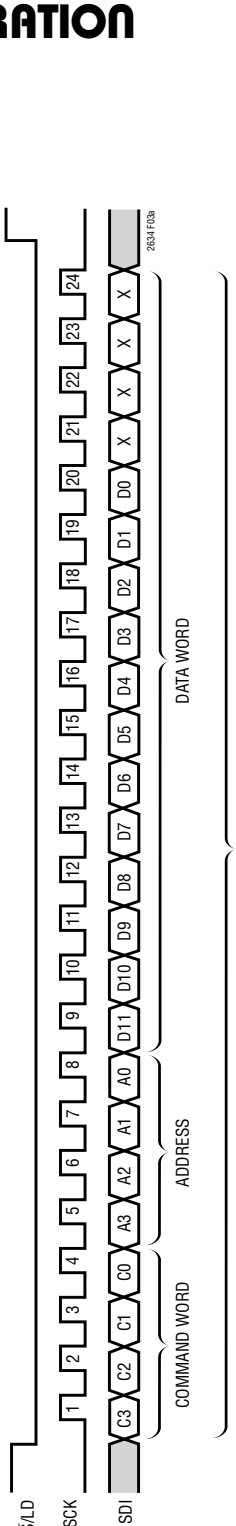



**Figure 3a. LTC2634-12 24-Bit Load Sequence (Minimum Input Word)**
**LTC2634-10 SDI Data Word: 10-Bit Input Code + 6 Don't Care Bits**
**LTC2634-8 SDI Data Word: 8-Bit Input Code + 8 Don't Care Bits**

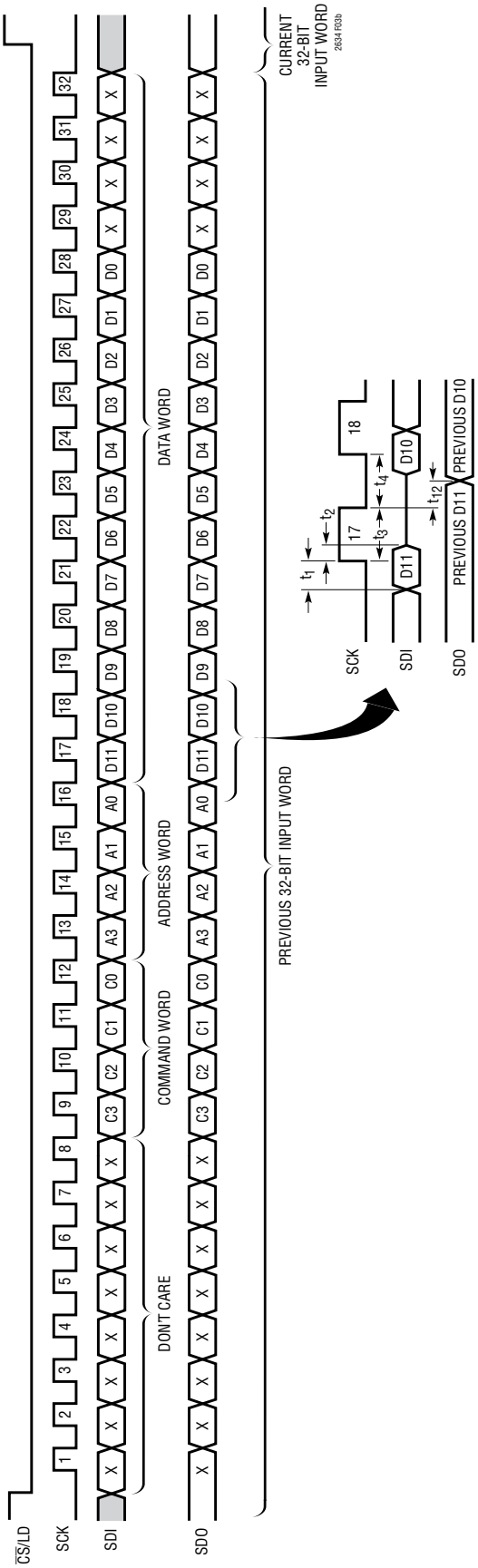



**Figure 3b. LTC2634-12 32-Bit Load Sequence (Required for Daisy-Chain Operation)**
**LTC2634-10 SDI Data Word: 10-Bit Input Code + 6 Don't Care Bits**
**LTC2634-8 SDI Data Word: 8-Bit Input Code + 8 Don't Care Bits**

## OPERATION

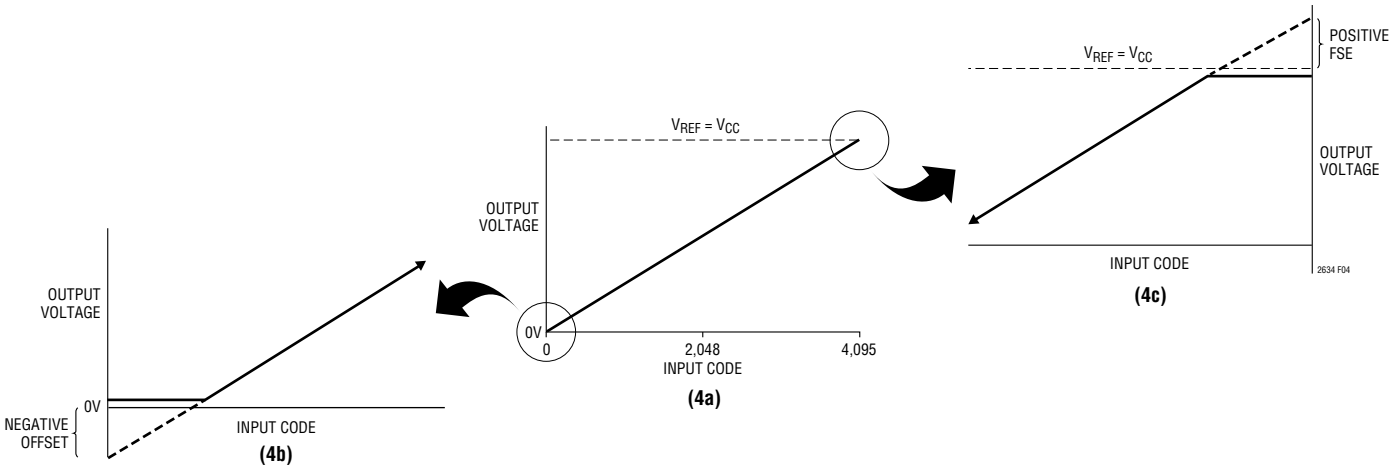



**Figure 4. Effects of Rail-to-Rail Operation on a DAC Transfer Curve (Shown in 12 Bits)**
**(4a) Overall Transfer Function**
**(4b) Effect of Negative Offset for Codes Near Zero**
**(4c) Effect of Postitive Full-Scale Error for Codes Near Full-Scale**

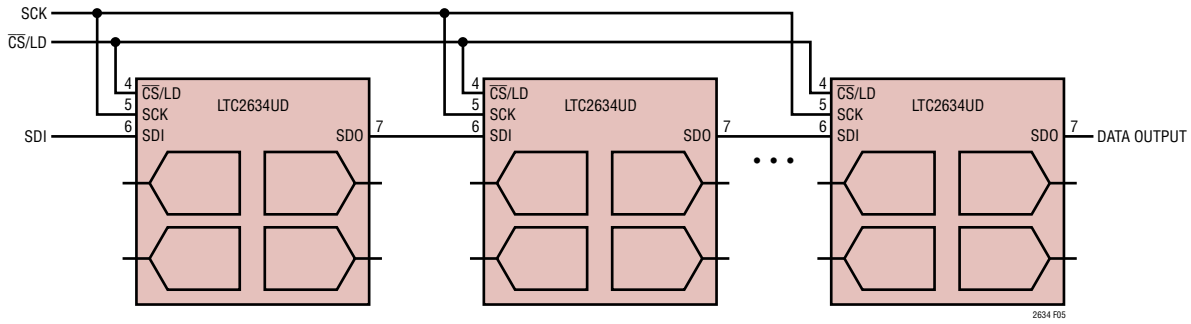
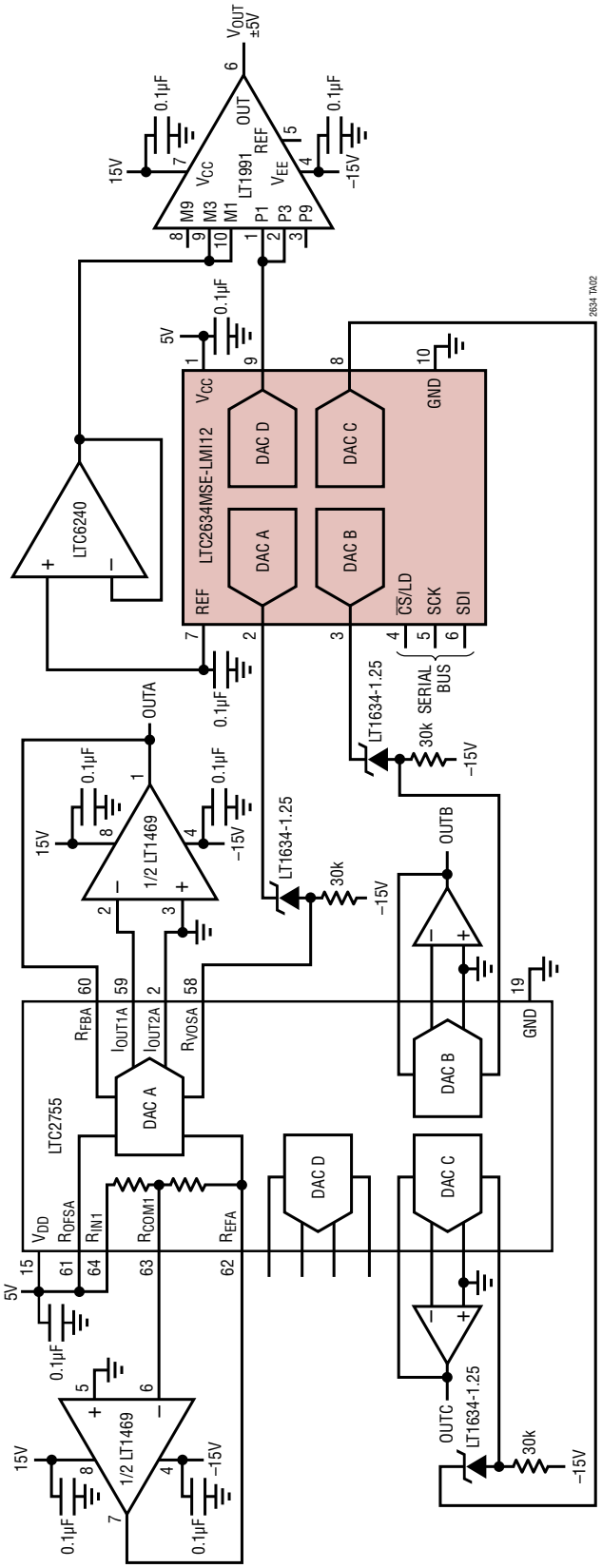



**Figure 5. Daisy-Chain Operation (QFN Only)**

## TYPICAL APPLICATION

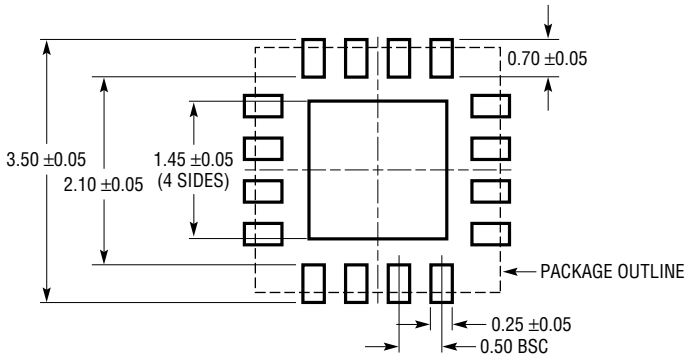
LTC2634 DACs Adjusts LTC2755-16 Offsets, Amplified with LT®1991 PGA to ±5V



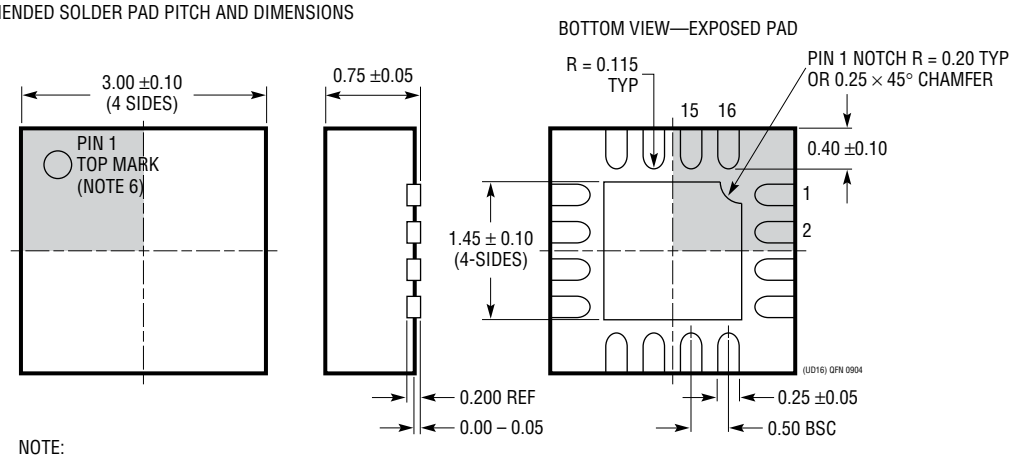
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC2634#packaging for the most recent package drawings.**

**UD Package**
**16-Lead Plastic QFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1691 Rev Ø)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

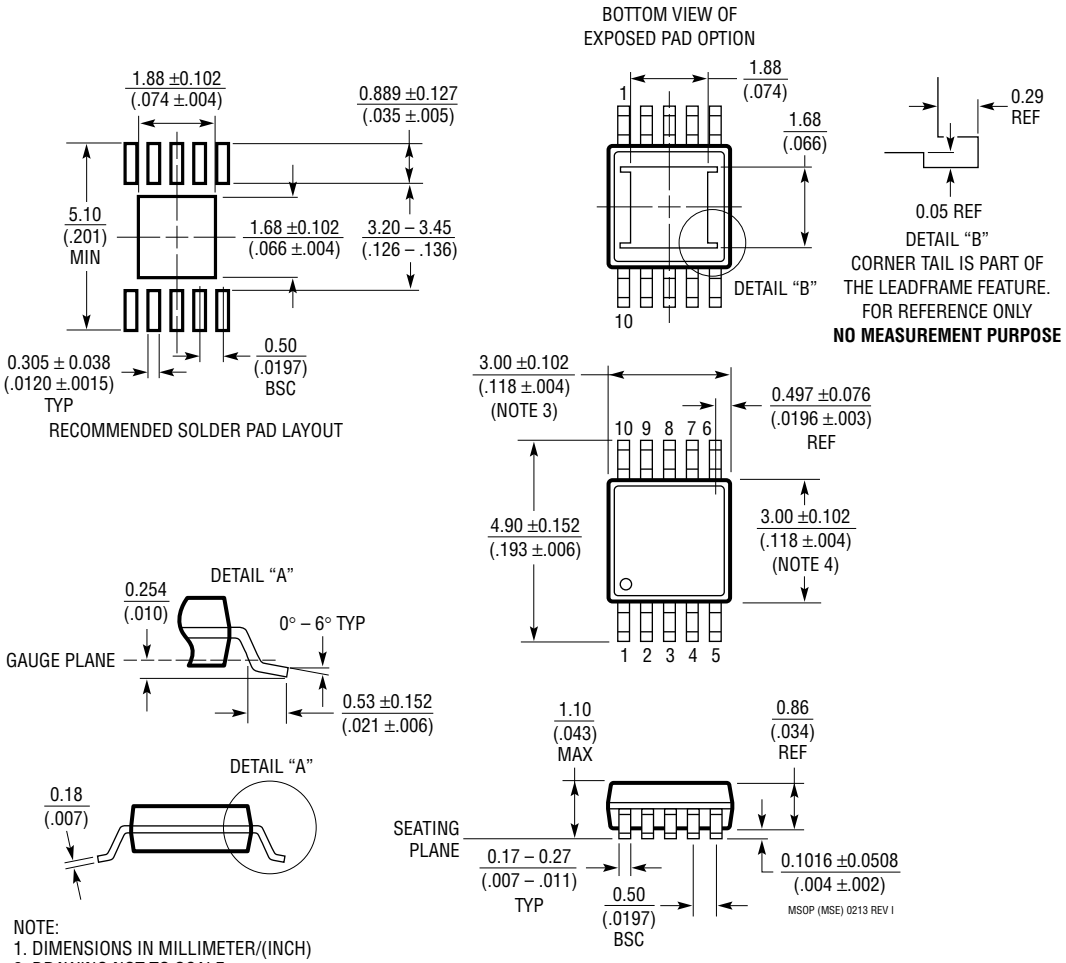



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC2634#packaging for the most recent package drawings.**

**MSE Package**
**10-Lead Plastic MSOP, Exposed Die Pad**
(Reference LTC DWG # 05-08-1664 Rev I)



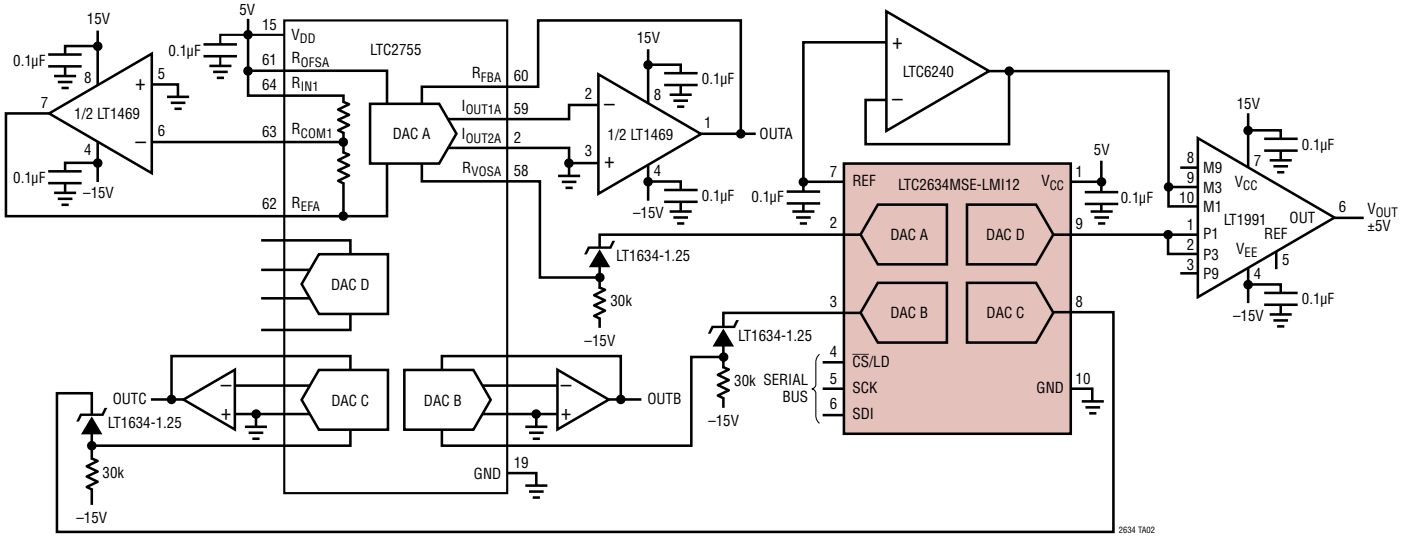

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 10/09 | Changes to Electrical Characteristics maximum limits. | 5, 6, 8, 9 |
| B | 12/09 | Change pin name to DNC. | 2, 16 |
| C | 06/10 | Revised Note 3 in the Electrical Characteristics section.<br>Added Typical Application and replaced Related Parts list. | 10<br>30 |
| D | 04/18 | Edits to Note 3. | 10 |

## TYPICAL APPLICATION

**LTC2634 DACs Adjusts LTC2755-16 Offsets, Amplified with LT1991 PGA to ±5V**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC2654/LTC2655 | Quad 16-/12 Bit, SPI/I²C $V_{OUT}$ DACs with 10ppm/°C Maximum Reference | ±4LSB INL Maximum at 16 Bits and ±2mV Offset Error, Rail-to-Rail Output, 20-Lead 4mm × 4mm QFN and 16-Lead Narrow SSOP Packages |
| LTC2604/ LTC2614/LTC2624 | Quad 16-/14-/12-Bit, SPI $V_{OUT}$ DACs with External Reference | 250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, 16-Lead SSOP Package |
| LTC2609/ LTC2619/LTC2629 | Quad 16-/14-/12-Bit $V_{OUT}$ DACs with I²C Interface | 250µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output with Separate $V_{REF}$ Pins for Each DAC |
| LTC2635 | Quad 12-/10-/8-Bit I²C $V_{OUT}$ DACs with 10ppm/°C Reference | ±2.5LSB INL, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, 16-Pin 3mm × 3mm QFN and 10-Lead MSOP Packages |
| LTC2656/LTC2657 | Octal 16-/12 Bit, SPI/I²C $V^{OUT}$ DACs with 10ppm/°C Maximum Reference | ±4LSB INL Maximum at 16 Bits and ±2mV Offset Error, Rail-to-Rail Output, 20-Lead 4mm × 5mm QFN and 16-Lead TSSOP Packages |
| LTC2636/LTC2637 | Octal 12-/10-/8-Bit, SPI/I²C $V_{OUT}$ DACs with 10ppm/°C Reference | 125µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 14-Lead 4mm × 3mm DFN and 16-Lead MSOP Packages |
| LTC2630/LTC2631 | Single 12-/10-/8-Bit, SPI/ I²C $V_{OUT}$ DACs with 10ppm/°C Reference | 180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Rail-to-Rail Output, SC70 (LTC2630)/ThinSOT™ (LTC2631) Packages |
| LTC2640 | Single 12-/10-/8-Bit, SPI $V_{OUT}$ DACs with 10ppm/°C Reference | 180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, ThinSOT Package |
| LTC1664 | Quad 10-Bit, Serial $V_{OUT}$ DAC | $V_{CC}$ = 2.7V to 5.5V, Micropower, Rail-to-Rail Output in 16-Pin Narrow SSOP |
| **Amplifiers** | | |
| LT1991 | Precision, 100µA Gain Selectable Amplifier | Gain Accuracy of 0.04%, Gains from –13 to 14, 100µA precision Op Amp |
| LT1469 | Dual 90MHz, 22V/µs 16-Bit Accurate Operational Amplifier | 90MHz Gain Bandwidth, 125µV Offset, 900ns, 22V/µs Slew Rate Precision Op Amp |