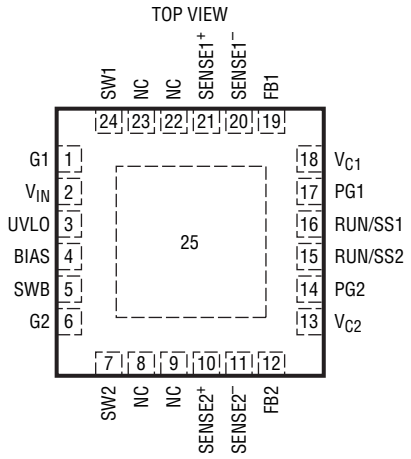
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 30V
UVLO Voltage 30V
PG1, PG2 Voltage 30V
SWB, BIAS Voltage 40V
SENSE1+, SENSE2+ Voltage 30V
SENSE1–, SENSE2– Voltage 30V
RUN/SS1, RUN/SS2 Voltage 6V
FB1, FB2 Voltage 6V
V_{C1}, V_{C2} Voltage 6V
Junction Temperature ..... 125°C
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 36°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3742EUF#PBF	LT3742EUF#TRPBF	3742	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C (Note 2)

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Input Voltage	V_{UVLO} = 1.5V	●		3.5	4.0	V
Quiescent Current	$V_{RUN/SS1}$ = $V_{RUN/SS2}$ = V_{FB1} = V_{FB2} = 1V			5.0	7.0	mA
Shutdown Current	$V_{RUN/SS1}$ = $V_{RUN/SS2}$ = 0V			20	35	µA
UVLO Pin Threshold	UVLO Pin Voltage Rising	●	1.20	1.25	1.28	V
UVLO Pin Hysteresis Current	V_{UVLO} = 1V, Current Flows Into Pin		1.8	3	4	µA
RUN/SS Pin Threshold			0.2	0.5		V
RUN/SS Pin Charge Current	$V_{RUN/SS}$ = 0V		0.5	1	1.5	µA
FB Pin Voltage		●	0.788	0.800	0.812	V
FB Pin Voltage Line Regulation	V_{IN} = 5V to 30V			0.01		%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise specified.

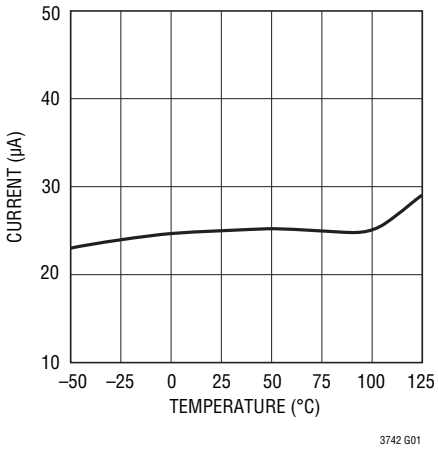
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB Pin Bias Current	V_{FB} = 0.8V, V_C = 0.4V			50	200	nA
FB Pin Voltage Matching			–4	0	4	mV
Error Amplifier Transconductance				250		µmho
Error Amplifier Voltage Gain				500		V/V
V_C Pin Source Current	V_{FB} = 0.6V			15		µA
V_C Pin Sink Current	V_{FB} = 1V			15		µA
Controller Switching Frequency			440	500	560	kHz
Switching Phase				180		Deg
Maximum Current Sense Voltage	V_{SENSE^-} = 3.3V	●	50	60	70	mV
Current Sense Matching	Between Controllers			±5		%
Current SENSE Pins Total Current	$SENSE^-$, $SENSE^+$ = 0V $SENSE^-$, $SENSE^+$ = 3.3V			–1.0 40		mA µA
Gate Rise Time	C_{LOAD} = 3300pF			40		ns
Gate Fall Time	C_{LOAD} = 3300pF			60		ns
Gate On Voltage (V_G – V_{SW})	V_{BIAS} = 12V		6.0	6.7	7.0	V
Gate Off Voltage (V_G – V_{SW})	V_{BIAS} = 12V			0.4	0.75	V
PG Pin Voltage Low	I_{PG} = 100µA			0.20	0.5	V
Lower PG Trip Level (Relative to V_{FB})	V_{FB} Increasing		–7	–10	–13	%
Lower PG Trip Level (Relative to V_{FB})	V_{FB} Decreasing		–10	–13	–16	%
Upper PG Trip Level (Relative to V_{FB})	V_{FB} Increasing		7	10	13	%
Upper PG Trip Level (Relative to V_{FB})	V_{FB} Decreasing		4	7	10	%
PG Pin Leakage Current	V_{PG} = 2V			0.1		µA
PG Pin Sink Current	V_{PG} = 0.5V		200	500		µA
Bias Pin Voltage			V_{IN} + 6.6	V_{IN} + 7	V_{IN} + 7.7	V
SWB Pin Current Limit			250	340	500	mA
SWB Pin Leakage Current	V_{SWB} = 12V			0.01	1	µA
Bias Supply Switching Frequency			0.88	1.0	1.12	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

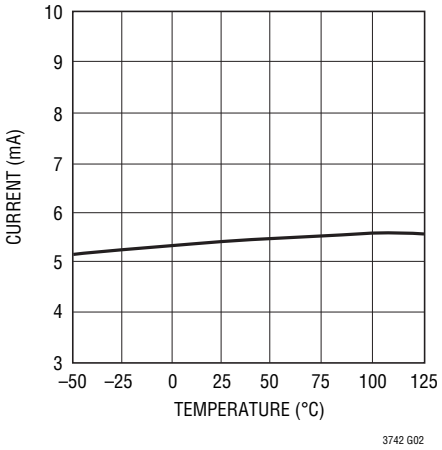
Note 2: The LT3742E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature range. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

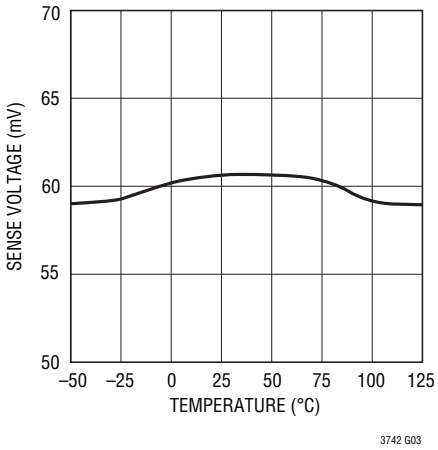
I_Q-SHDN vs Temperature



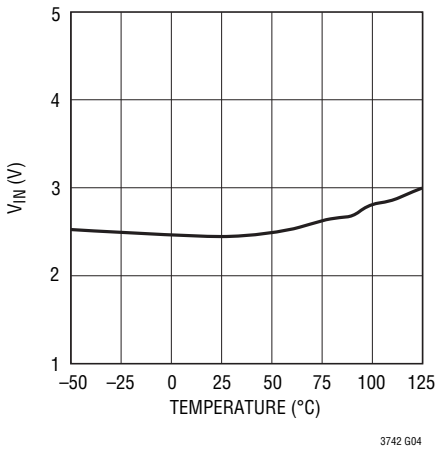
I_Q-Running vs Temperature



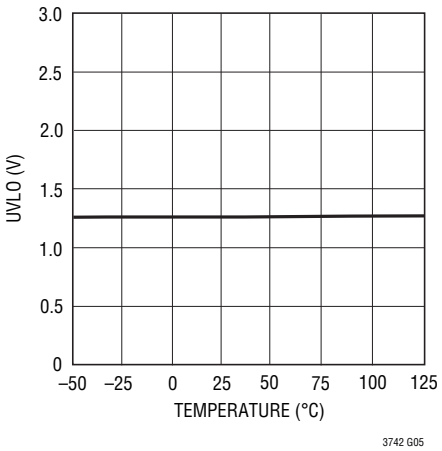
Controller Current Sense Voltage vs Temperature



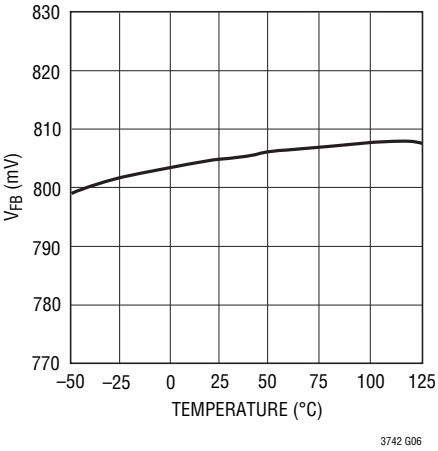
Internal UVLO vs Temperature



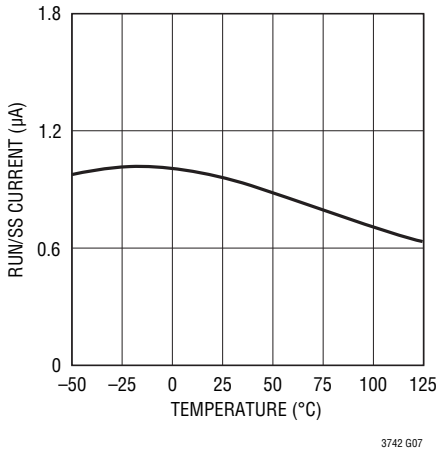
UVLO Threshold vs Temperature



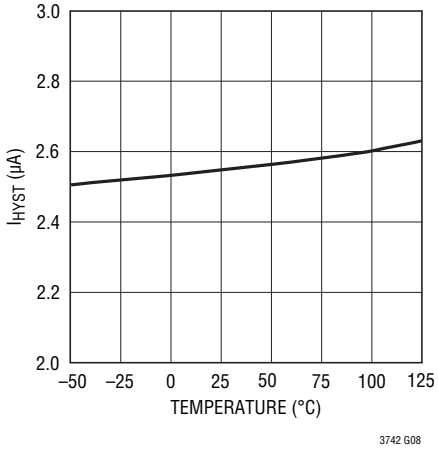
V_{FB} vs Temperature



RUN/SS Current vs Temperature

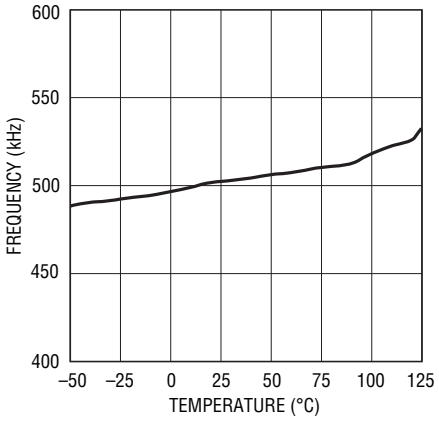


UVLO I_{HYST} vs Temperature

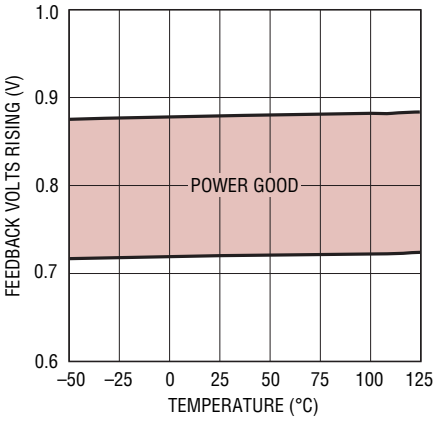


TYPICAL PERFORMANCE CHARACTERISTICS

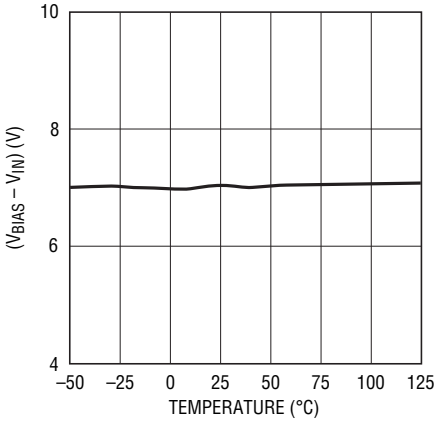
Controller Frequency vs Temperature



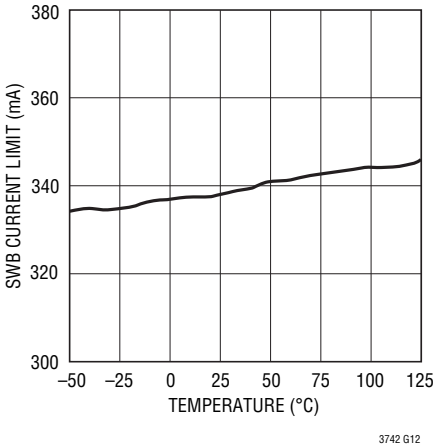
PG Threshold vs Temperature



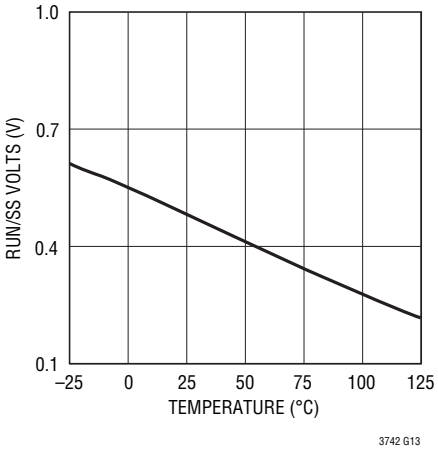
$V_{BIAS} – V_{IN}$ vs Temperature



SWB Current Limit vs Temperature



RUN/SS Threshold vs Temperature



PIN FUNCTIONS

G1, G2 (Pins 1, 6): Gate Drives. These pins provide high current gate drive for the external N-channel MOSFETs. These pins are the outputs of floating drivers whose voltage swings between the BIAS and SW pins.

V_{IN} (Pin 2): Input Voltage. This pin supplies current to the internal circuitry of the LT3742. This pin must be locally bypassed with a capacitor.

UVLO (Pin 3): Undervoltage Lockout. *Do not leave this pin open*; connect it to V_{IN} if not used. A resistor divider connected to V_{IN} is tied to this pin to program the minimum input voltage at which the LT3742 will operate. When this pin is less than 1.25V, the controllers are disabled (the RUN/SS pins are still used to turn on each switching regulator). Once this pin drops below 1.25V, a 3µA current sink draws current into the pin to provide programmable hysteresis for UVLO.

BIAS (Pin 4): Bias for Gate Drive. This pin provides a bias voltage higher than the input voltage to drive the external N-channel MOSFETs. The voltage on this pin is regulated to V_{IN} + 7V.

SWB (Pin 5): Bias Regulator Switch. This is the collector of an internal NPN switch used to generate the bias voltage to provide gate drive for the external N-channel MOSFETs.

RUN/SS1, RUN/SS2 (Pins 16, 15): Run/Soft-Start Pins. These pins are used to shut down each controller. They also provide a soft-start function with the addition of an external capacitor. To shut down any regulator, pull the RUN/SS pin to ground with an open-drain or open-collector device. If neither feature is used, leave these pins unconnected.

PG1, PG2 (Pins 17, 14): Power Good. These pins are open-collector outputs of internal comparators. PG remains low until the FB pin is within 90% of the final regulation voltage. As well as indicating output regulation, the PG pins can be used to sequence the switching regulators. The PG outputs are valid when V_{IN} is greater than 4V and either of the RUN/SS pins is high. The power good comparators are disabled in shutdown. If not used, these pins should be left unconnected.

V_{C1}, V_{C2} (Pins 18, 13): Control Voltage and Compensation Pins for Internal Error Amplifiers. Connect a series RC from these pins to ground to compensate each switching regulator loop.

FB1, FB2 (Pins 19, 12): Feedback Pins. The LT3742 regulates these pins to 800mV. Connect the feedback resistors to this pin to set the output voltage for each switching regulator.

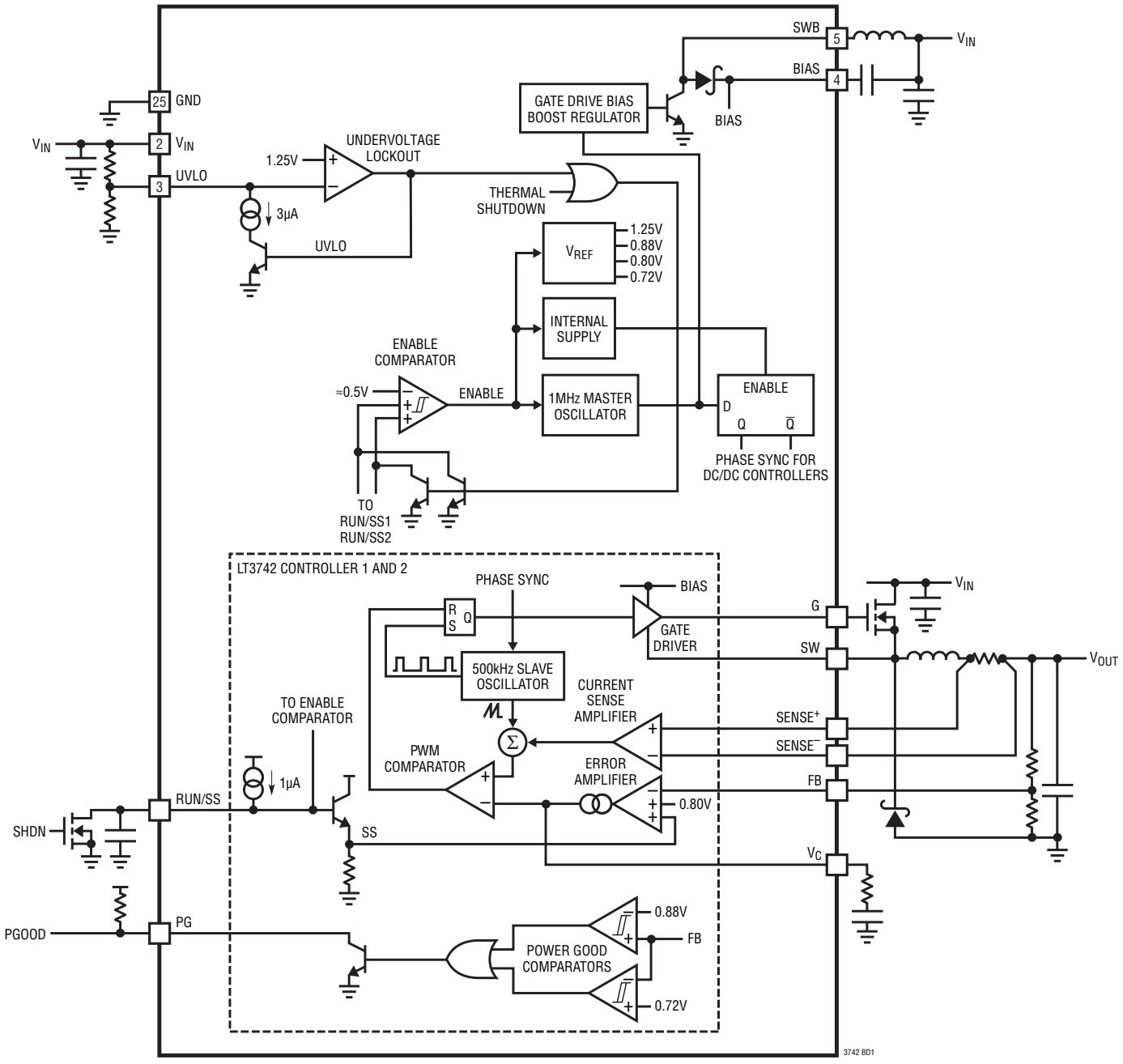
SENSE1$^-$, SENSE2$^-$ (Pins 20, 11): Negative Current Sense Inputs. These pins (along with the SENSE$^+$ pins) are used to sense the inductor current for each switching regulator.

SENSE1$^+$, SENSE2$^+$ (Pins 21, 10): Positive Current Sense Inputs. These pins (along with the SENSE$^-$ pins) are used to sense the inductor current for each switching regulator.

SW1, SW2 (Pins 24, 7): Switch Nodes. These pins connect to the source of the external N-channel MOSFETs and to the external inductors and diodes.

Exposed Pad (Pin 25): Ground. The Exposed Pad of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The Exposed Pad must be soldered to the circuit board to ensure proper operation.

BLOCK DIAGRAM



OPERATION

The LT3742 is a dual, constant frequency, current mode DC/DC step-down controller. The two controllers in each device share some common circuitry including protection circuitry, the internal bias supply, voltage reference, master oscillator and the gate drive boost regulator. The Block Diagram shows the shared common circuitry and the independent circuitry for both DC/DC controllers.

Important protection features included in the LT3742 are undervoltage lockout and thermal shutdown. When either of these conditions exist, the gate drive bias regulator and both DC/DC controllers are disabled and both RUN/SS pins are discharged to 0.5V to get ready for a new soft-start cycle. Undervoltage lockout (UVLO) is programmed using two external resistors. When the UVLO pin drops below 1.25V, a 3µA current sink is activated to provide programmable hysteresis for the UVLO function. A separate, less accurate, internal undervoltage lockout will disable the LT3742 when V_{IN} is less than 2.5V.

The gate drive boost regulator is enabled when all internal fault conditions have been cleared. This regulator uses both an internal NPN power switch and Schottky diode to generate a voltage at the BIAS pin that is 7V higher than the input voltage. Both DC/DC controllers are disabled until the BIAS voltage has reached ~90% of its final regulation voltage. This ensures that sufficient gate drive to fully enhance the external MOSFETs is present before the driver is allowed to turn on.

The master oscillator runs at 1MHz and clocks the gate drive boost regulator at this frequency. The master oscillator also generates two 500kHz clocks, 180° out of phase, for the DC/DC controllers.

A power good comparator pulls the PG pin low whenever the FB pin is not within ±10% of the 800mV internal reference voltage. PG is the open-collector output of an NPN that is off when the FB pin is in regulation, allowing an external resistor to pull the PG pin high. This power good indication is valid only when the device is enabled (RUN/SS is high) and V_{IN} is 4V or greater.

The LT3742 enables each controller independently when its RUN/SS pin is above 0.5V and each controller generates its own soft-start ramp. During start-up, the error amplifier compares the FB pin to the soft-start ramp instead of the precision 800mV reference, which slowly raises the output voltage until it reaches its resistor programmed regulation point. Control of the inductor current is strictly maintained until the output voltage is reached. The LT3742 is ideal for applications where both DC/DC controllers need to operate separately.

A pulse from the 500kHz oscillator sets the RS flip-flop and turns on the external N-channel MOSFET. Current in the switch and the external inductor begins to increase. When this current reaches a level determined by the control voltage (V_C), the PWM comparator resets the flip-flop, turning off the MOSFET. The current in the inductor then flows through the external Schottky diode and begins to decrease. This cycle begins again at the next set pulse from the slave oscillator. In this way, the voltage at the V_C pin controls the current through the inductor to the output. The internal error amplifier regulates the output voltage by continually adjusting the V_C pin voltage. Direct control of the peak inductor current on a cycle-by-cycle basis is managed by the current sense amplifier. Because the inductor current is constantly monitored, the devices inherently provide excellent output short-circuit protection.

APPLICATIONS INFORMATION

Soft-Start and Shutdown

The RUN/SS (Run/Soft-Start) pins are used to enable each controller independently, and to provide a user-programmable soft-start function that reduces the peak input current and prevents output voltage overshoot during start-up. To disable either controller, pull its RUN/SS pin to ground with an open-drain or open-collector device. If both RUN/SS pins are pulled to ground, the LT3742 is placed in shutdown mode, and quiescent current is reduced to 20µA. Internal 1µA current sources pull up on each RUN/SS pin, and when either pin reaches 0.5V, that controller is enabled, along with the internal bias supply, gate drive boost regulator, voltage reference and master oscillator. If both outputs are always enabled together, one soft-start capacitor can be used with both RUN/SS pins tied together.

The Benefits of Soft-Start

When a capacitor is tied from the RUN/SS pin to ground, the internal 1µA pull-up current source generates a voltage ramp on this pin. During start-up, the error amplifier compares the FB pin to this ramp instead of to the 800mV reference; this slowly and smoothly increases the output voltage to its final value, while maintaining control of the inductor current. Always check the inductor current and output voltage waveforms to ensure that the programmed soft-start time is long enough. A new soft-start cycle will be initiated whenever V_{IN} drops low enough to trigger undervoltage lockout (programmed using the UVLO pin), or the LT3742 die temperature exceeds thermal shutdown. A typical value for the soft-start capacitor is 1nF.

Soft-start is strongly recommended for all LT3742 applications, as it provides the least amount of stress on the external power MOSFET and catch diode. Without soft-start, both of these components will see the maximum current limit every start-up cycle. Figures 1a and 1b show start-up waveforms with and without soft-start for the circuit on the front page. Notice the large inductor current spike and the output voltage overshoot when soft-start is not used. While this may be acceptable for some systems, the addition of a single capacitor dramatically improves the start-up behavior of each DC/DC controller.

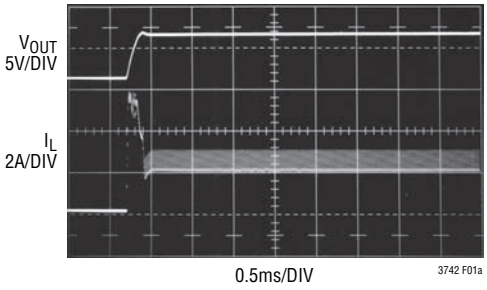


Figure 1a. Start-Up Waveforms Without Soft-Start

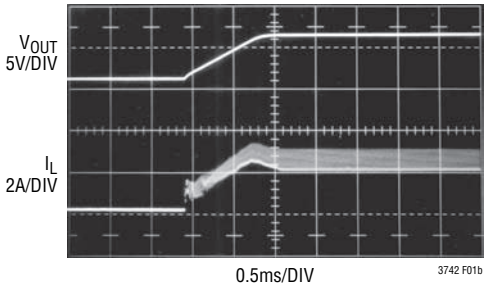


Figure 1b. Start-Up Waveforms with 1nF Soft-Start Capacitor

APPLICATIONS INFORMATION

Power Good Indicators

The PG pin is the open-collector output of an internal window comparator that is pulled low whenever the FB pin is not within ±10% of the 800mV internal reference voltage. Tie the PG pin to any supply less than 30V with a pull-up resistor that will supply less than 200µA. This pin will be open when the LT3742 is placed in shutdown mode regardless of the voltage at the FB pin. The power good indication is valid only when the LT3742 is enabled (RUN/SS is high) and V_{IN} is 4V or greater.

Output Sequencing and Tracking

The RUN/SS and PG pins can be used together to sequence the two outputs of the LT3742. Figure 3 shows three circuits to do this. For the first two cases, controller 1 starts first.

In Figure 2a, controller 2 turns on only after controller 1 has reached within 10% of its final regulation voltage. A larger value for the soft-start capacitor on RUN/SS2 will provide additional delay between the outputs. One

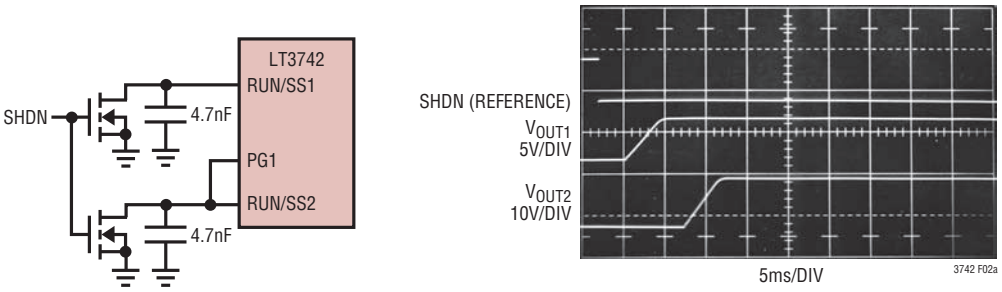


Figure 2a. Supply Sequencing with Controller 2 Delayed Until After Controller 1 is in Regulation

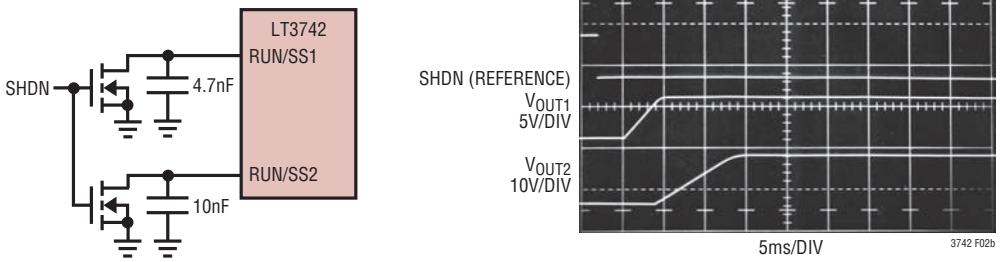


Figure 2b. Supply Sequencing with Controller 2 Having a Fixed Delay Relative to Controller 1

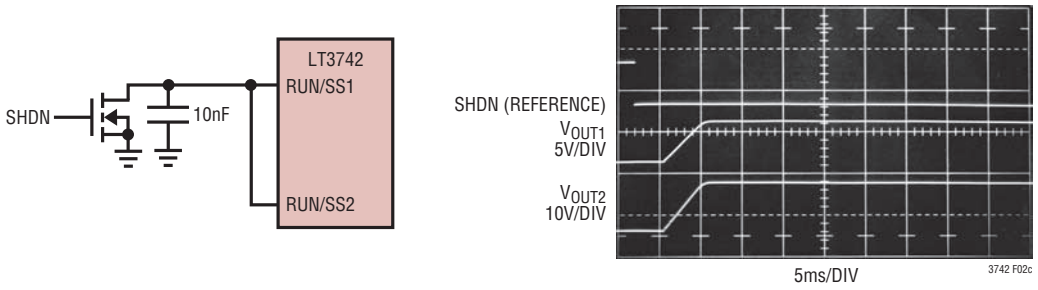


Figure 2c. Both Conditions Start Up Together with Ratiometic Tracking

APPLICATIONS INFORMATION

characteristic to notice about this method is that if the output of controller 1 goes out of regulation enough to trip the power good comparator, controller 2 will be disabled.

In Figure 2b, a slightly larger capacitor on RUN/SS2 delays the turn-on of controller 2 with respect to controller 1. The start-up waveforms for this method look very similar to the one shown in Figure 6a, but here controller 2 is not disabled if controller 1 goes out of regulation.

In Figure 2c, both RUN/SS pins share a single capacitor and start up at the same time. By sharing the same soft-start signal, this method provides ratiometric tracking of the two outputs.

Undervoltage Lockout (UVLO)

An external resistor divider can be used to accurately set the minimum input voltage at which the LT3742 will operate. Figure 3 shows the basic UVLO operation. Once the UVLO pin drops below 1.25V, an undervoltage lockout event is signaled, turning on a 3µA current source to provide hysteresis.

During a UVLO event, both controllers and the gate drive boost regulator are disabled. For the LT3742, all RUN/SS pins are discharged to get ready for a new soft-start cycle. For each controller that is enabled, it's RUN/SS pin will be held to 500mV until the input voltage rises above the upper UVLO trip voltage. The UVLO function is only active when one or more of the controllers are enabled using the RUN/SS pin. The UVLO pin can not be used to directly start the part. Do not leave the UVLO pin unconnected; tie it to V_{IN} if not used. A separate, less accurate, internal undervoltage lockout will disable the LT3742 when V_{IN} is less than 2.5V.

The UVLO resistor values are chosen to give the desired minimum operating voltage ($V_{IN(MIN)}$) and the desired amount of hysteresis (V_{HYST}). The LT3742 will turn on when the input voltage is above ($V_{IN(MIN)}$ + V_{HYST}), and once on, will turn off when V_{IN} drops below $V_{IN(MIN)}$. Select the value for R_{UV1} first, then select the value for R_{UV2}.

$$R_{UV1} = \frac{V_{HYST}}{3\mu A}$$

$$R_{UV2} = R_{UV1} \bullet \frac{1.25V}{V_{IN(MIN)} - 1.25V}$$

Input Voltage Range

The minimum input voltage is determined by either the LT3742's minimum operating voltage of 4V, UVLO or by the output voltages of a given application. The LT3742 can operate at 100% duty cycle, so if the input voltage drops close to or equal to one of the output voltages, the controller will go into low dropout operation (100% duty cycle). The duty cycle is the fraction of the time the N-channel MOSFET is on every switch cycle, and is determined by the input and output voltages:

$$DC = \left(\frac{V_{OUT} + V_D}{V_{IN} - V_{DS} + V_D} \right)$$

where V_D is the forward drop of the catch diode (~0.4V) and V_{DS} is the typical MOSFET voltage drop (~0.1V).

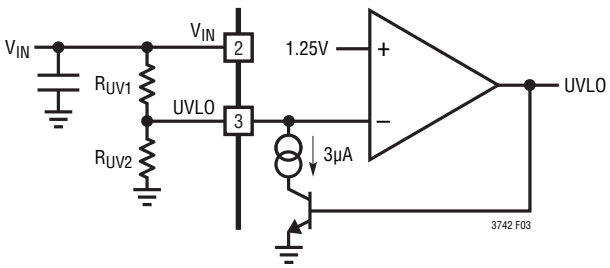


Figure 3. Undervoltage Lockout

APPLICATIONS INFORMATION

The maximum input voltage is determined by the absolute maximum ratings of the V_{IN} and BIAS pins (30V and 40V, respectively) and by the minimum duty cycle, DC_{MIN} = 15%.

$$V_{IN(MAX)} = \left(\frac{V_{OUT} + V_D}{DC_{MIN}}\right) + V_{SW} - V_D$$

The formula above calculates the maximum input voltage that allows the part to regulate without pulse-skipping, and is mainly a concern for applications with output voltages lower than 3.3V. For example, for a 2.5V output, the maximum input voltage is:

$$V_{IN(MAX)} = \left(\frac{2.5V + 0.4V}{0.15}\right) + 0.1V - 0.4V = 19V$$

If an input voltage higher than 19V is used, the 2.5V output will still regulate correctly, but the part must pulse-skip to do so. Pulse skipping does not damage the LT3742, but it will result in erratic inductor current waveforms and higher peak currents. Note that this is a restriction on the operating input voltage only for a specific output voltage; the circuit will tolerate inputs up to the absolute maximum rating.

The Benefits of 2-Phase Operation

Traditionally, dual controllers operate with a single phase. This means that both power MOSFETs are turned on at the same time, causing current pulses of up to twice the amplitude of those from a single regulator to be drawn from the input capacitor. These large amplitude pulses increase the RMS current flowing in the input capacitor, require the use of larger and more expensive input capacitors, increase EMI, and causes increased power losses in the input capacitor and input power supply.

The two controllers of the LT3742 are guaranteed by design to operate 180° out of phase. This assures that the current in each power MOSFET will never overlap, always presenting a significantly low peak and RMS current demand to the input capacitor. This allows the use of a smaller, less expensive input capacitor, improving EMI performance and real world operating efficiency.

Figure 4 shows example waveforms for a single phase dual controller versus a 2-phase LT3742 system. In this case, 5V and 3.3V outputs, each drawing a load current of 2A, are derived from a 12V supply. In this example, 2-phase

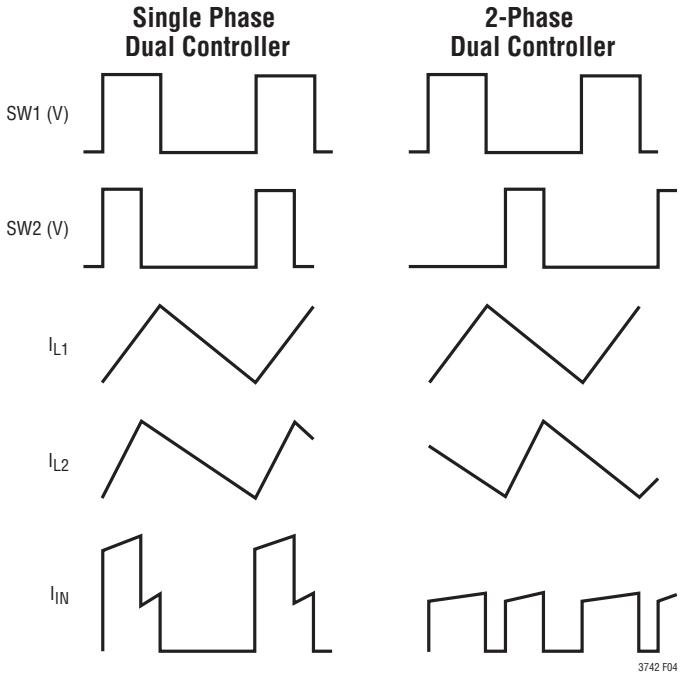


Figure 4. Example Waveforms for a Single Phase Dual Controller vs the 2-Phase LT3742

APPLICATIONS INFORMATION

operation would reduce the RMS input capacitor current from ~1.8A_{RMS} to ~0.8A_{RMS}. While this is an impressive reduction by itself, remember that power losses are proportional to I_{RMS}^2, meaning that the actual power wasted due to the input capacitor is reduced by a factor of ~4. Figure 5 shows the reduction in RMS ripple current for a typical application.

The reduced input ripple current also means that less power is lost in the input power path. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage. Significant cost and board footprint savings are also realized by being able to use smaller, less expensive, lower RMS current-rated input capacitors.

Of course, the improvement afforded by 2-phase operation is a function of the relative duty cycles of the two controllers, which in turn, are dependent upon the input voltage (DC ≈ V_{OUT}/V_{IN}).

It can be readily seen that the advantages of 2-phase operation are not limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

Inductor Value Selection

The inductor value directly affects inductor ripple current, I_{RIPPLE}, and maximum output current, $I_{OUT(MAX)}$. Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Too large of a value, however, will result in a physically large inductor. A good trade-off is to choose the inductor ripple current to be ~30% of the maximum output current. This will provide a good trade off between the inductor size, maximum output current, and the amount of ripple current. Note that the largest ripple current occurs at the highest the input voltage, so applications with a wide V_{IN} range should consider both $V_{IN(TYP)}$ and $V_{IN(MAX)}$ when calculating the inductor value:

$$L \geq \frac{V_{IN} - V_{OUT}}{0.3 \bullet I_{OUT(MAX)}} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \frac{1}{500kHz}$$

This equation provides a good starting point for picking the inductor value. Most systems can easily tolerate ripple currents in the range of 10% to 50%, so deviating slightly from the calculated value is acceptable for most applications. Pick a standard value inductor close to the

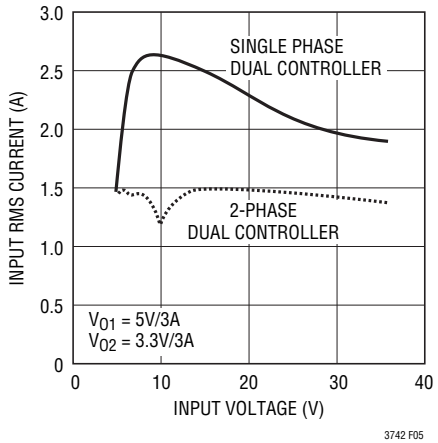


Figure 5. RMS Input Current Comparison

APPLICATIONS INFORMATION

value calculated above, and then recheck the amount of ripple current:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{L} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \frac{1}{500kHz}$$

The DC resistance (DCR) of the inductor can have a significant impact on total system efficiency, as it causes an I^2R_{DCR} power loss. Consider inductance value, DCR, and current rating when choosing an inductor. Table 1 shows several recommended inductor vendors. Each offers numerous devices in a wide variety of values, current ratings, and package sizes.

Table 1. Recommended Inductor Manufacturers

VENDOR	WEBSITE
Sumida	www.sumida.com
Toko	www.toko.com
Würth	www.we-online.com
NEC-Tokin	www.nec-tokinamerica.com
TDK	www.tdk.com

Maximum Output Current (R_{SENSE} Value Selection)

Maximum output current is determined largely by the values of the current sense resistor, RSENSE (which sets the inductor peak current), and the inductor (which sets the inductor ripple current). The LT3742 current comparator has a guaranteed minimum threshold of 50mV, which does not vary with duty cycle. The maximum output current is calculated:

$$I_{OUT(MAX)} = \frac{50mV}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

Rearranging the equation above to solve for RSENSE gives:

$$R_{SENSE} = \frac{50mV}{I_{OUT(MAX)} + \left(\frac{I_{RIPPLE}}{2}\right)}$$

Inductor, Catch Diode and MOSFET Current Rating

Once the inductor and R_{SENSE} values have been chosen, the current ratings of the inductor, catch diode and MOSFET can then be determined. The LT3742 current comparator has a guaranteed maximum threshold of 70mV, and there is a small amount of current overshoot resulting from the response time of the current sense comparator. The components should be rated to handle:

$$I_{RATED} \geq \frac{70mV}{R_{SENSE}} + \left(\frac{V_{IN}}{L} \bullet 100ns\right)$$

Schottky Catch Diode Selection

During output short-circuits, the diode will conduct current most of the time, so it is important to choose a device with a sufficient current rating. In addition, the diode must have a reverse voltage rating greater than the maximum input voltage. Many surface mount Schottky diodes are available in very small packages. Read their data sheets carefully as they typically must be temperature derated. Basically, excessive heating prevents them from being used effectively at their rated maximum current. A few recommended diodes are listed in Table 2.

Table 2. Recommended Schottky Diodes

VENDOR	DEVICE
Diodes, Inc. www.diodes.com	PDS540 (5A, 40V) SBM1040 (10A, 40V)
Microsemi www.microsemi.com	UPS340 (3A, 40V) UPS840 (8A, 40V)
On Semiconductor www.onsemi.com	MBRD320 (3A, 20V) MBRD340 (3A, 40V)

Power MOSFET Selection

There are several important parameters to consider when choosing an N-channel power MOSFET: drain current (maximum I_D); breakdown voltage (maximum V_{DS} and V_{GS}); threshold voltage ($V_{GS(TH)}$); on-resistance ($R_{DS(ON)}$); reverse transfer capacitance (C_{RSS}); and total gate charge

APPLICATIONS INFORMATION

(Q_G). A few simple guidelines will make the selection process easier.

The maximum drain current must be higher than the maximum rated current, I_{RATED}, calculated on the previous page. Note that the I_D specification is largely temperature dependent (lower I_D at higher ambient temperatures), so most data sheets provide a graph or table of I_D versus temperature to show this.

Ensure that the V_{DS} breakdown voltage is greater than the maximum input voltage and that the V_{GS} breakdown voltage is 8V or greater. The peak-to-peak gate drive for each MOSFET is ~7V, so also ensure that the device chosen will be fully enhanced with a V_{GS} of 7V. This may preclude the use of some MOSFETs with a 20V V_{GS} rating, as some have too high of a threshold voltage. A good rule of thumb is that the maximum threshold voltage should be $V_{GS(TH)(MAX)} \leq$ 3V. 4.5V MOSFETs will work as well.

Power losses in the N-channel MOSFET come from two main sources: the on-resistance, $R_{DS(ON)}$, and the reverse transfer capacitance, C_{RSS}. The on-resistance causes ohmic losses ($I^2R_{DS(ON)}$) which typically dominate at input voltages below ~15V. The reverse transfer capacitance results in transition losses which typically dominate for input voltages above ~15V. At higher input voltages, transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} will actually provide higher efficiency. The power loss in the MOSFET can be approximated by:

$$P_{LOSS} = (\text{ohmic loss}) + (\text{transition loss})$$

$$P_{LOSS} \approx \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D} \bullet I_{OUT}{}^2 R_{DS(ON)} \bullet \rho_T \right) \left(2 \bullet V_{IN}{}^2 \bullet I_{OUT} \bullet C_{RSS} \bullet f \right)$$

where f is the switching frequency (500kHz) and ρ_T is a normalizing term to account for the on-resistance change due to temperature. For a maximum ambient temperature of 70°C, using $\rho_T \approx 1.3$ is a reasonable choice.

The trade-off in $R_{DS(ON)}$ and C_{RSS} can easily be seen in an example using real MOSFET values. To generate a 3.3V, 3A (10W) output, consider two typical N-channel power MOSFETs, both rated at V_{DS} = 30V and both available in the same SO-8 package, but having ~5x differences in on-resistance and reverse transfer capacitance:

M1: $I_D = 11.5A$, $V_{GS} = 12V$, $R_{DS(ON)} = 10m\Omega$, $C_{RSS} = 230pF$

M2: $I_D = 6.5A$, $V_{GS} = 20V$, $R_{DS(ON)} = 50m\Omega$, $C_{RSS} = 45pF$

Power loss is calculated for both devices over a wide input voltage range ($4V \leq V_{IN} \leq 30V$), and shown in Figure 6 (as a percentage of the 10W total power). Note that while the low $R_{DS(ON)}$ device power loss is 5× lower at low input

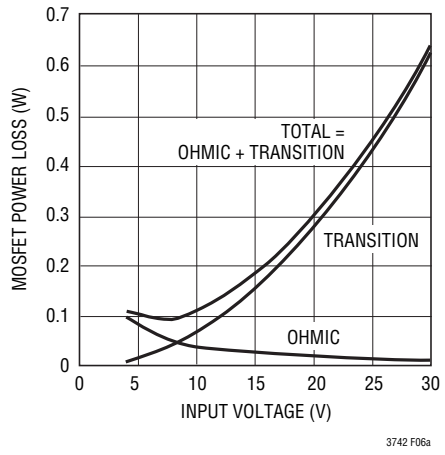


Figure 6a. Power Loss Example for M1 (10mΩ, 230pF)

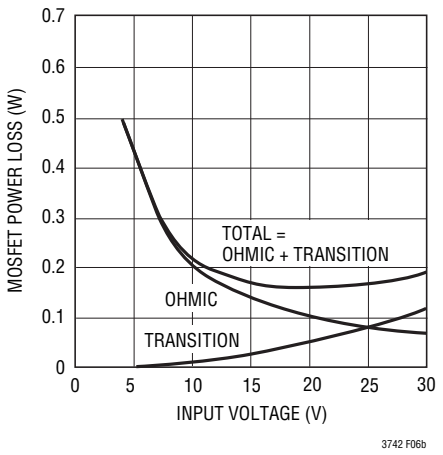


Figure 6b. Power Loss Example for M2 (50m, 45pF)

APPLICATIONS INFORMATION

voltages, it is also 3× higher at high input voltages when compared to the low C_{RSS} device.

Total gate charge, Q_G, is closely related to C_{RSS}. Low gate charge corresponds to a small value of C_{RSS}. Many manufacturers have MOSFETs advertised as "low gate charge" devices (which means they are low C_{RSS} devices) that are specifically designed for low transition loss, and are ideal for high input voltage applications.

Input Capacitor Selection

For most applications, 10µF to 22µF of input capacitance per channel will be sufficient. A small 1µF bypass capacitor between the V_{IN} and ground pins of the LT3742, placed close to the device, is also suggested for optimal noise immunity. Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3742 and to force this very high frequency switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively, and it must have an adequate ripple current rating. With two controllers operating at the same frequency but with different phases and duty cycles, calculating the input capacitor RMS current is not simple. However, a conservative value is the RMS input current for the channel that is delivering the most power ($V_{OUT} \bullet I_{OUT}$):

$$I_{RMS(CIN)} = \frac{I_{OUT}}{V_{IN}} \bullet \sqrt{V_{OUT} \bullet (V_{IN} - V_{OUT})}$$

$I_{RMS(CIN)}$ is largest ($I_{OUT}/2$) when $V_{IN} = 2V_{OUT}$ (at DC = 50%). As the second, lower power channel draws input current, the input capacitor's RMS current actually decreases as the out-of-phase current cancels the current drawn by the higher power channel, so choosing an input capacitor with an RMS ripple current rating of $I_{OUT,MAX}/2$ is sufficient.

The combination of small size and low impedance (low equivalent series resistance, or ESR) of ceramic capacitors make them the preferred choice. The low ESR results in very low input voltage ripple and the capacitors can handle plenty of RMS current. They are also comparatively robust and can be used at their rated voltage. Use only X5R or X7R types because they retain their capacitance over wider voltage and temperature ranges than other ceramics.

An alternative to a high value ceramic capacitor is a lower value (1µF) along with a larger value (10µF to 22µF) electrolytic or tantalum capacitor. Because the input capacitor is likely to see high surge currents when the input source is applied, tantalum capacitors should always be surge rated. The manufacturer may also recommend operation below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the N-channel power MOSFET.

Output Capacitor Selection

A good starting value for output capacitance is to provide 10µF of C_{OUT} for every 1A of output current. For lower output voltages (under 3.3V) and for applications needing the best possible transient performance, the ratio should be 20µF to 30µF of C_{OUT} for every 1A of output current. X5R and X7R ceramics are an excellent choice for the output capacitance. Aluminum electrolytics can be used, but typically the ESR is too large to deliver low output voltage ripple. Tantalum and newer, lower ESR organic electrolytic capacitors are also possible choices, and the manufactures will specify the ESR. Because the volume of the capacitor determines the ESR, both the size and value will be larger than a ceramic capacitor that would give you similar output ripple voltage performance.

The output capacitor filters the inductor ripple current to generate an output with low ripple. It also stores energy in order to satisfy transient loads and to stabilize the

APPLICATIONS INFORMATION

LT3742's control loop. Output ripple can be estimated with the following equation:

$$V_{RIPPLE} = \Delta I_L \left(\frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} + ESR \right)$$

where ΔI_L is the inductor ripple current and f_{SW} is the switching frequency (500kHz). The ESR is so low for ceramic capacitors that it can be left out of the above calculation. The output voltage ripple will be highest at maximum input voltage (ΔI_L increases with input voltage). Table 3 shows several low-ESR capacitor manufacturers.

Table 3. Low ESR Surface Mount Capacitors

VENDOR	TYPE	SERIES
Taiyo Yuden www.t-yuden.com	Ceramic X5R, X7R	
Murata www.murata.com	Ceramic X5R, X7R	
Kemet www.kemet.com	Tantalum Ta Organic Al Organic	T491, T494, T495 T520 A700
Sanyo www.sanyo.com	Ta or Al Organic	POSCAP
Panasonic www.panasonic.com	Al Organic	SP CAP
TDK www.tdk.com	Ceramic X5R, X7R	
Nippon Chemicon www.chemi-con.co.jp	Ceramic X5R, X7R	

Setting Output Voltage

The output of a bipolar controller requires a minimum load to prevent current sourced from the switch pin charging the output capacitor above the desired output voltage. This current, approximately 5mA, may be accounted for in the feedback string or the user may choose to force a minimum load in their application.

The output voltage for each controller is programmed with a resistor divider between the output and the FB pin. Always use 1% resistors (or better) for the best output voltage accuracy. The value of R_A should be 8k or less, and the value of R1 should be chosen according to:

$$R_B = R_A \bullet \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$

Output Short-Circuit Protection

Because the LT3742 constantly monitors the inductor current, both devices inherently providing excellent output short-circuit protection. The N-channel MOSFET is not allowed to turn on unless the inductor current is below the threshold of the current sense comparator. This guarantees that the inductor current will not "run away" and the controller will skip cycles until the inductor current has dropped below the current sense threshold.

Loop Compensation

An external resistor and capacitor connected in series from the V_C pin to ground provides loop compensation for each controller. Sometimes a second, smaller valued capacitor is placed in parallel to filter switching frequency noise from the V_C pin. Loop compensation determines the stability and transient performance of each controller.

A practical approach is to start with values of R_C = 10k and C_C = 330pF, then tune the compensation network to optimize the performance. When adjusting these values, change only one value at a time (R_C or C_C), then see how the transient response is affected. The simplest way to check loop stability is to apply a load current step while observing the transient response at the output. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature to ensure a robust design.

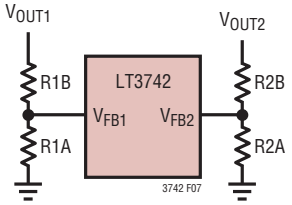


Figure 7. Setting Output Voltage with the FB Pin

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Bias Supply Considerations

The LT3742 uses an internal boost regulator to provide a bias rail for enhancement of the external MOSFETs. This bias rail is regulated to V_{IN} + 7V and must be in regulation before either controller is allowed to start switching. As this is a high speed switching regulator, standard procedures must be followed regarding placement of the external components. The SWB node should be kept small to reduce EMI effects and the bias decoupling capacitor (C_{BIAS}) should be kept close to the BIAS pin and V_{IN}. A slight surplus of power is available from this supply and it can be tapped after stringent engineering evaluation.

PC Board Layout Considerations

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement.

- Place the power components close together with short and wide interconnecting traces. The power components consist of the top MOSFETs, catch diodes and the inductors C_{IN} and C_{OUT}. One way to approach this is to simply place them on the board first.
- Similar attention should be paid to the power components that make up the boost converter. They should also be placed close together with short and wide traces.
- Always use a ground plane under the switching regulator to minimize interplane coupling.
- Minimize the parasitic inductance in the loop of C_{IN}, MOSFET and catch diode, which carry large switching currents.
- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI low.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low. Unused areas can be filled with copper and connect to any DC node (V_{IN}, V_{OUT}, GND).
- Place CB close to BIAS pin and input capacitor.
- Keep the high dv/dt nodes (SW1, SW2, G1, G2, C_{IN1}, C_{IN2}, SWB) away from sensitive small-signal nodes.

Demo board gerber files are available to assist with a reliable layout. It will be difficult to achieve data sheet performance specifications with improper layout.

APPLICATIONS INFORMATION

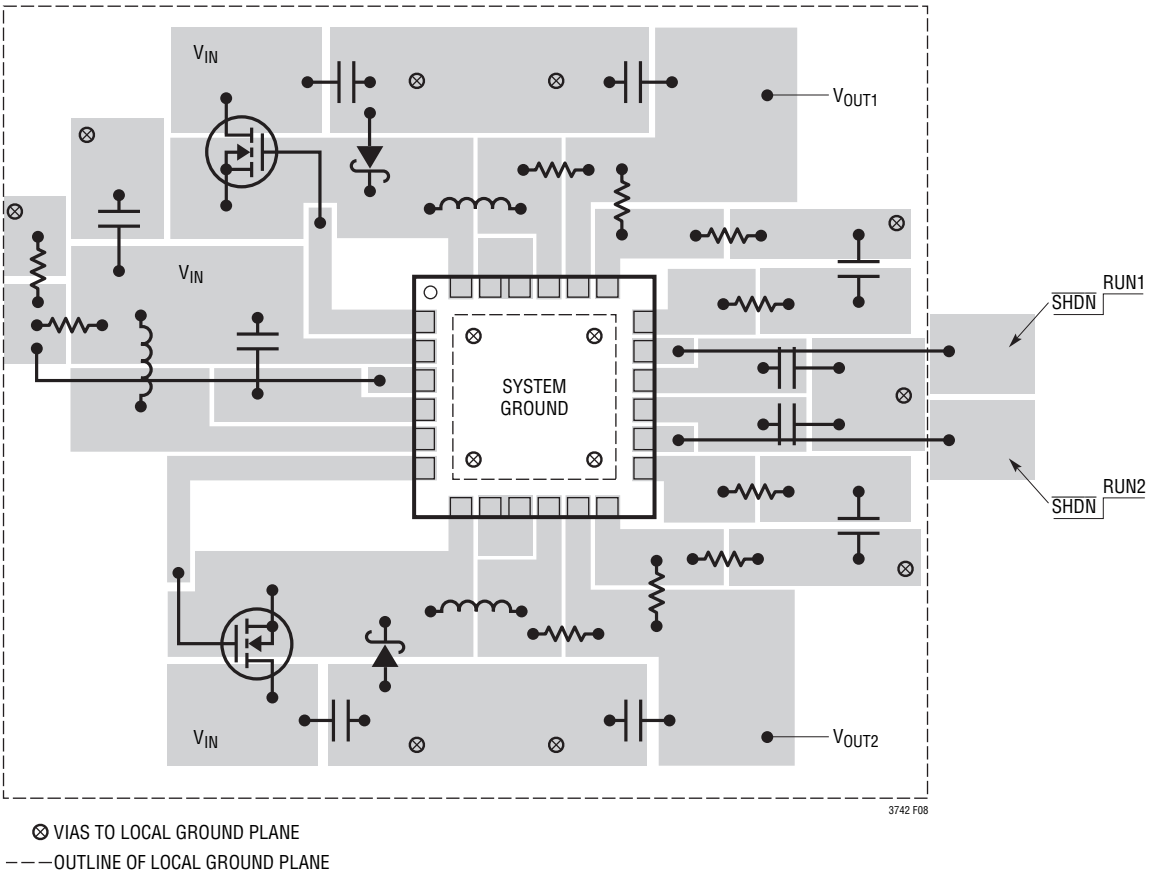
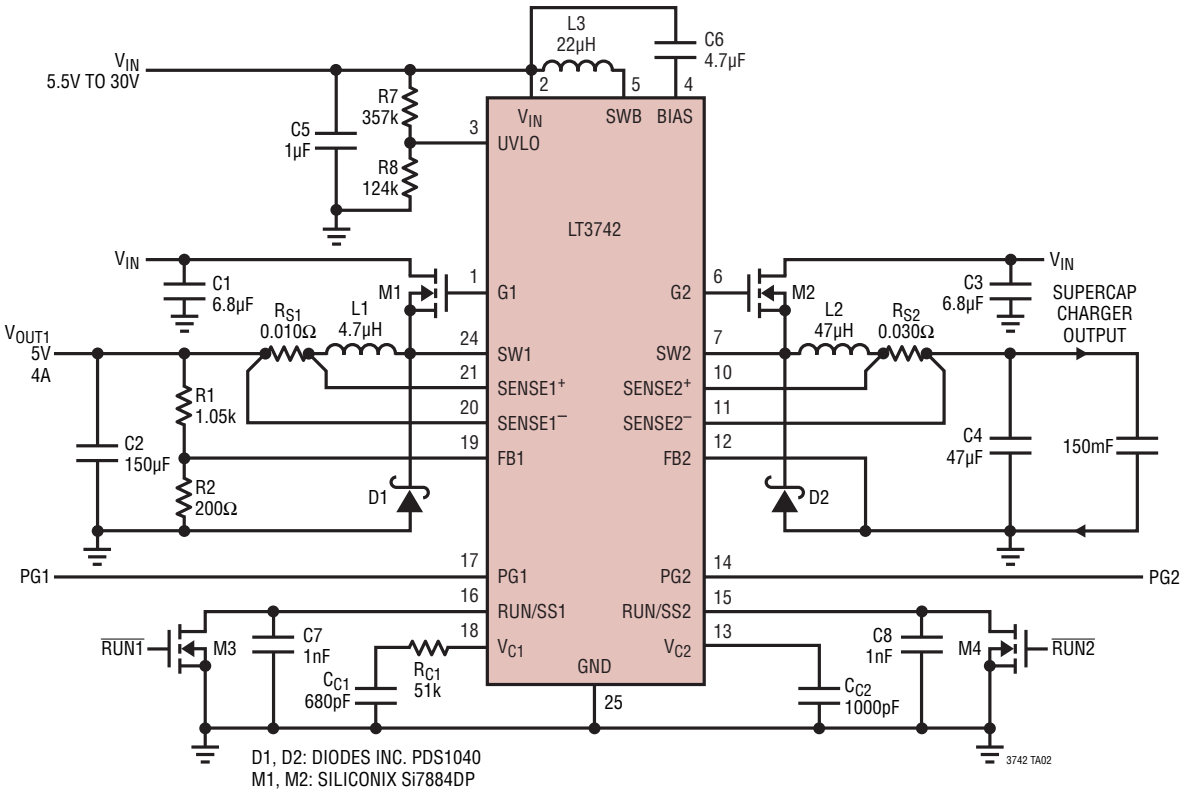


Figure 8. A Good PCB Layout Ensures Proper, Low EMI Operation

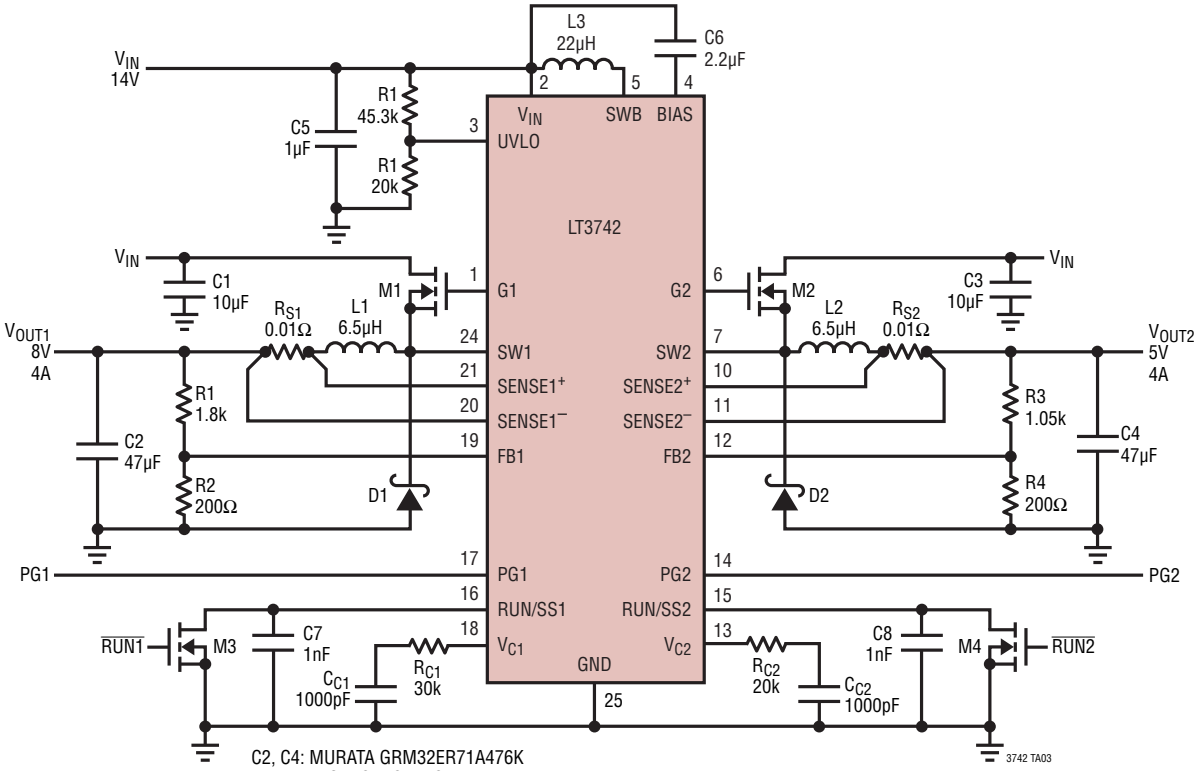
TYPICAL APPLICATIONS

Supercap Charger Plus a DC/DC Buck Converter



TYPICAL APPLICATIONS

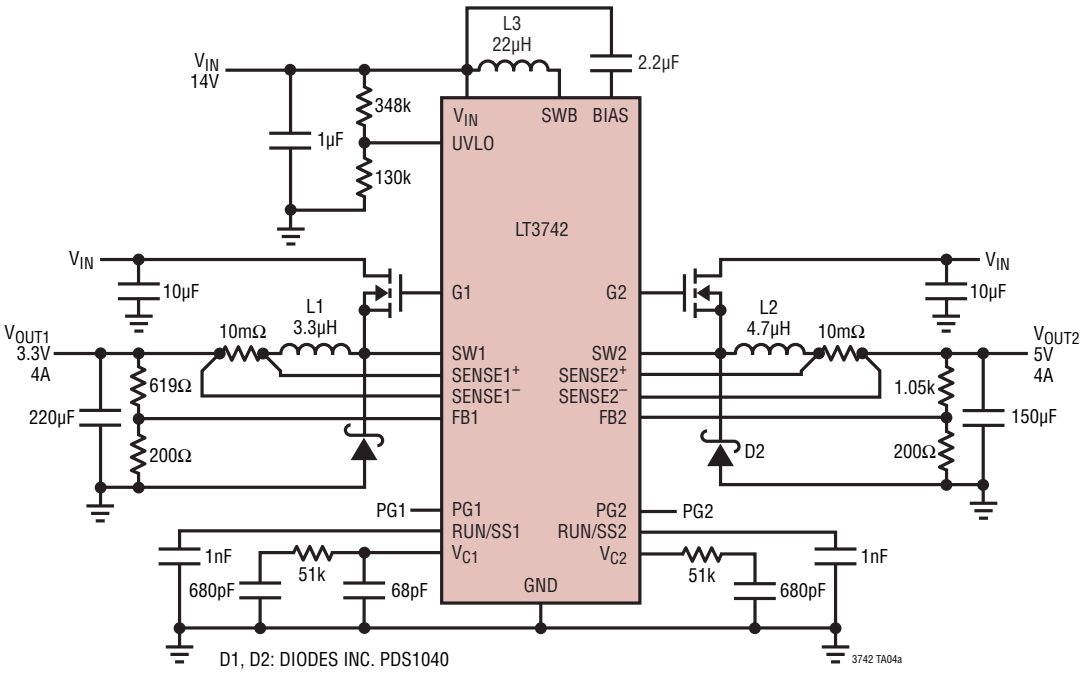
8V and 5V Dual Step-Down Converter



C2, C4: MURATA GRM32ER71A476K
D1, D2: DIODES INC. PDS1040
L1, L2: WÜRTH ELEKTRONIK 744314650
M1, M2: FAIRCHILD FDS4470

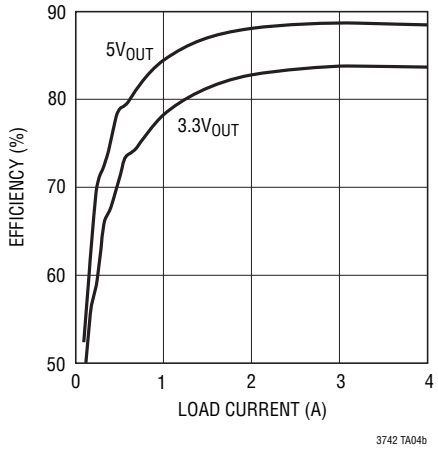
TYPICAL APPLICATIONS

5V and 3.3V Dual Step-Down Converter



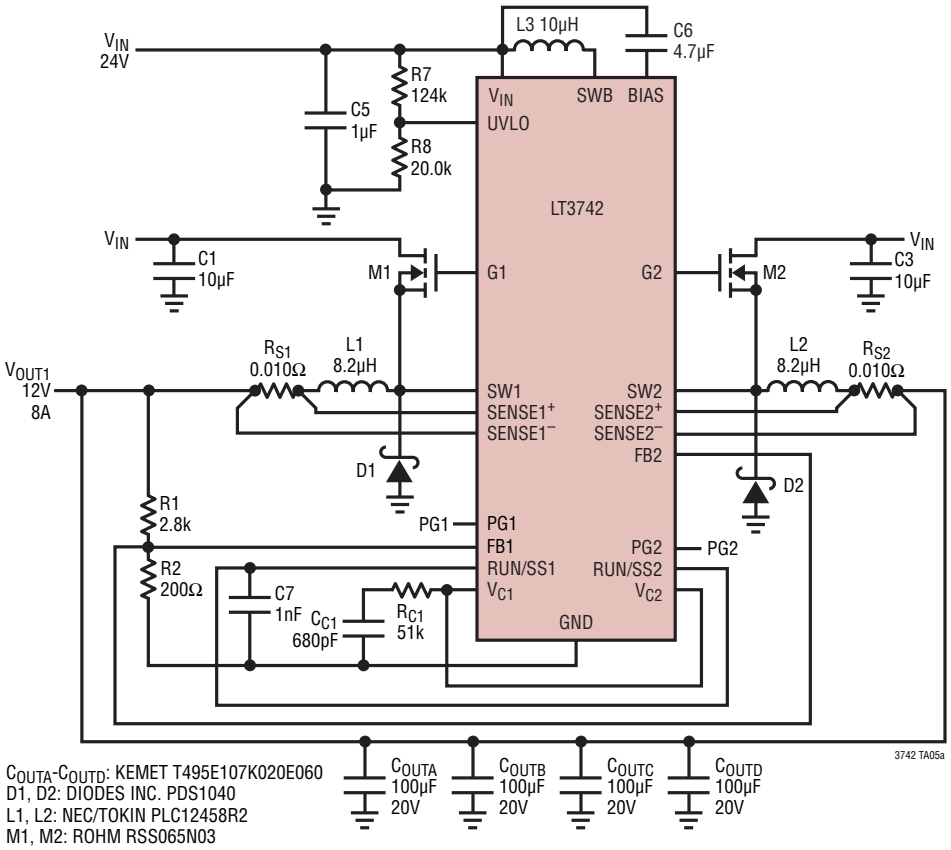
D1, D2: DIODES INC. PDS1040
L1: VISHAY IHLP2525CZER3R3
L2: VISHAY IHLP2525CZER4R7
L3: COILCRAFT: ME3220-223KL
M1, M2: VISHAY Si7848DP-T1-E3

Efficiency vs Load Current



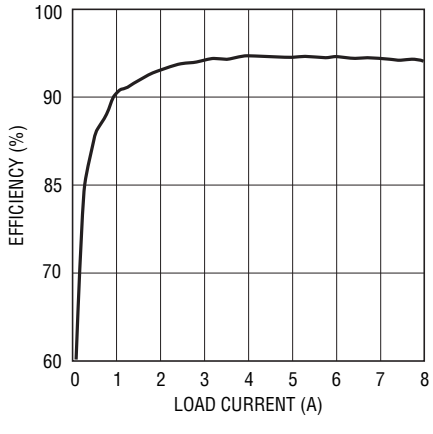
TYPICAL APPLICATIONS

High Current, Low Ripple 12V Step-Down Converter



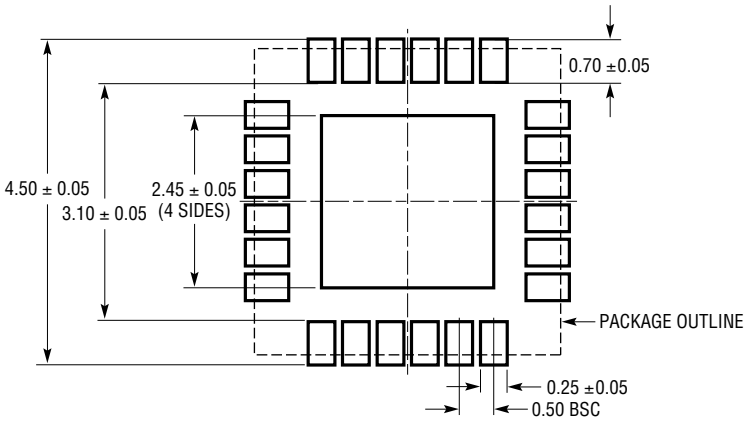
COUTA-COUTD: KEMET T495E107K020E060
D1, D2: DIODES INC. PDS1040
L1, L2: NEC/TOKIN PLC12458R2
M1, M2: ROHM RSS065N03

12V_{OUT} Efficiency vs Load Current

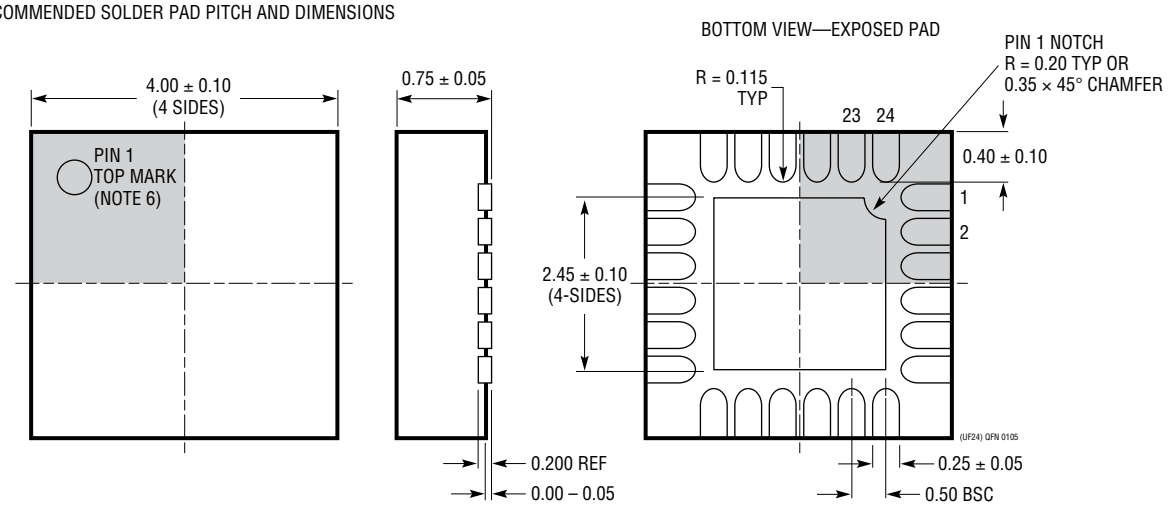


PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/11	Revised Conditions in the Electrical Characteristics section.	2, 3
		Revised the title of curve G04 in the Typical Performance Characteristics section.	4
		Updated the PG1, PG2 pin description in the Pin Functions section.	6
		Updated values in the Block Diagram, Operation, and Applications Information sections.	7-12

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1625/LTC1775	No R_{SENSE}™ Current Mode Synchronous Step-Down Controllers	97% Efficiency, No Sense Resistor, 16-Pin SSOP
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Output Fault Protection, 16-Pin SSOP
LTC1778	No R_{SENSE} Wide Input Range Synchronous Step-Down Controller	Up to 97% Efficiency, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)(V_{IN})$, I_{OUT} Up to 20A
LT3430/LT3431	Monolithic 3A, 200kHz/500kHz Step-Down Regulators	5.5V = <V_{IN} = <60V, 0.1 Saturation Switch, 16-Lead SSOP Package
LTC3703/LTC3703-5	100V Synchronous Switching Regulator Controllers	No R_{SENSE}, Voltage Mode Control, GN16 Package
LT3724	High Voltage Current Mode Switching Regulator Controllers	V_{IN} Up to 60V, $I_{OUT} \le 5A$, 16-Lead TSSOP Package, Onboard Bias Regulator, Burst Mode® Operation, $I_Q < 100\mu A$, 200kHz Operation
LT3800	High Voltage Synchronous Controller	V_{IN} Up to 60V, $I_{OUT} \le 20A$, Current Mode, Onboard Bias Regulator, Burst Mode Operation, $I_Q = 100\mu A$, 16-Lead TSSOP Package
LT3844	High Voltage Current Mode Controller with Programmable Operating Frequency	V_{IN} Up to 60V, $I_{OUT} \le 5A$, Onboard Bias Regulator, Burst Mode Operation, Sync Capability, $I_Q = 120\mu A$, 16-Lead TSSOP Package
LTC3727A-1	Dual, 2-Phase Synchronous Controller	Very Low Dropout; $V_{OUT} \le 14V$
LTC3728	2-Phase 550kHz, Dual Synchronous Step-Down Controller	QFN and SSOP Packages, High Frequency for Smaller L and C
LTC3729	20A to 200A PolyPhase® Synchronous Controllers	Expandable from 2-Phase to 12-Phase, Uses All Surface Mount Components, No Heat Sink
LTC3731	3-Phase, 600kHz Synchronous Step-Down Controller	$0.6V \le V_{OUT} \le 6V$, $4.5V \le V_{IN} \le 32V$, $I_{OUT} \le 60A$, Integrated MOSFET Drivers
LTC3773	Triple Output DC/DC Synchronous Controller	3-Phase Step-Down DC/DC Controller, $3.3V \le V_{IN} \le 36V$, Fixed Frequency 160kHz to 700kHz
LTC3826/LTC3826-1	30µA I_Q, Dual, 2-Phase Synchronous Step-Down Controllers	2-Phase Operation, 30µA One Channel No Load I_Q (50µA Total), $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$
LTC3827/LTC3827-1	Low I_Q Dual Synchronous Controllers	2-Phase Operation, 115µA Total No Load I_Q, $4V \le V_{IN} \le 36V$, 80µA No Load I_Q with One Channel On
LTC3834/LTC3834-1	Low I_Q Synchronous Step-Down Controllers	30µA No Load I_Q, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$
LTC3835/LTC3835-1	Low I_Q Synchronous Step-Down Controllers	80µA No Load I_Q, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$
LTC3850	Dual, 2-Phase Synchronous Step-Down DC/DC Controller	2-Phase Operation, $4V \le V_{IN} \le 24V$, 95% Efficiency, No R_{SENSE} Option, I_{OUT} Up to 20A, 4mm 4mm QFN
LT3845	High Voltage Synchronous Step-Down Single Output Controller	Very Low Quiescent Current (120µA), V_{IN} Up to 60V, Fixed Frequency 100kHz to 500kHz, Synchronizable Up to 600kHz

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