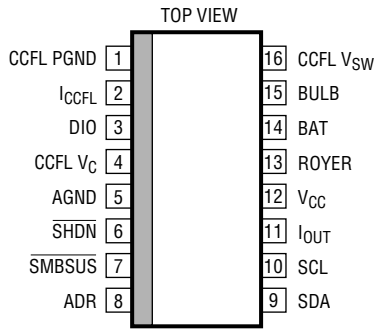
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} 7V
BAT, Royer, BULB 30V
CCFL V_{SW} 60V
Shutdown 6V
I_{CCFL} Input Current 10mA
DIO Input Current (Peak, <100ms) 100mA
Digital Inputs ..... –0.3V to (V_{CC} + 0.3V)
Digital Outputs ..... –0.3V to (V_{CC} + 0.3V)
DAC Output Voltage ..... –15V to (V_{CC} + 0.3V)
Junction Temperature (Note 2) ..... 100°C
Operating Ambient Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1786FCS

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = $\overline{SHUTDOWN}$ = $\overline{SMBSUS}$ = SCL = SDA = 3.3V, BAT = Royer = BULB = 12V, I_{CCFL} = CCFL V_{SW} = Open, DIO = I_{OUT} = GND, CCFL V_C = 0.5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	3V ≤ V_{CC} ≤ 6.5V, I_{OUT} = 0µA	●		6	9.5	mA
ISUS	$\overline{SMBSUS}$ Supply Current	$\overline{SMBSUS}$ = 0V or Command Code Bit 7 = 1, CCFL V_C = Open (Note 3)	●		40	100	µA
$I_{\overline{SHDN}}$	$\overline{SHUTDOWN}$ Supply Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = Open (Note 3)	●		150	300	µA
	$\overline{SHUTDOWN}$ Input Bias Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = Open			5	10	µA
	$\overline{SHUTDOWN}$ Threshold Voltage		●	0.45	0.85	1.2	V
f	Switching Frequency	Measured at CCFL V_{SW}, I_{SW} = 50mA, I_{CCFL} = 100µA, CCFL V_C = Open	 ●	175 160	200 200	225 240	kHz kHz
DC(MAX)	Maximum Switch Duty Cycle	Measured at CCFL V_{SW}	 ●	80 75	85 85		% %
BV	Switch Breakdown Voltage	Measured at CCFL V_{SW}		60	70		V
	Switch Leakage Current	V_{SW} = 12V, Measured at CCFL V_{SW} V_{SW} = 30V, Measured at CCFL V_{SW}				20 40	µA µA
	I_{CCFL} Summing Voltage	3V ≤ V_{CC} ≤ 6.5V	 ●	0.425 0.385	0.465 0.465	0.505 0.555	V V
	ΔI_{CCFL} Summing Voltage for ΔInput Programming Current	I_{CCFL} = 0µA to 100µA			5	15	mV
	CCFL V_C Offset Sink Current	CCFL V_C = 1.5V, Positive Current Measured into Pin		–5	5	15	µA
	ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current	I_{CCFL} = 25µA, 50µA, 75µA, 100µA, CCFL V_C = 1.5V	●	4.70	4.95	5.20	µA/µA
	CCFL V_C to DIO Current Servo Ratio	DIO = 5mA out of Pin, Measure I(V_C) at CCFL V_C = 1.5V	●	94	99	104	µA/mA
	CCFL V_C Low Clamp Voltage	V_{BAT} – V_{BULB} = BULB Protect Servo Voltage	●		0.1	0.3	V
	CCFL V_C High Clamp Voltage	I_{CCFL} = 100µA	●	1.7	2.1	2.4	V
	CCFL V_C Switching Threshold	CCFL V_{SW} DC = 0%	●	0.6	0.95	1.3	V
	CCFL High-Side Sense Servo Current	I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V	●	0.93	1.00	1.07	A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = $\overline{SHUTDOWN}$ = $\overline{SMBSUS}$ = SCL = SDA = 3.3V, BAT = Royer = BULB = 12V, I_{CCFL} = CCFL V_{SW} = Open, DIO = I_{OUT} = GND, CCFL V_C = 0.5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
	CCFL High-Side Sense Servo Current Line Regulation	BAT = 5V to 30V, I_{CCFL} = 100µA, $I(V_C)$ = 0µA at CCFL V_C = 1.5V			0.1	0.16	%/V
	CCFL High-Side Sense Supply Current	Current Measured into BAT and Royer Pins	●	50	100	150	µA
	BULB Protect Servo Voltage	I_{CCFL} = 100µA, $I(V_C)$ = 0µA at CCFL V_C = 1.5V, Servo Voltage Measured between BAT and BULB Pins	●	6.5	7.0	7.5	V
	BULB Input Bias Current	I_{CCFL} = 100µA, $I(V_C)$ = 0µA at CCFL V_C = 1.5V			5	9	µA
I_{LIM}	CCFL Switch Current Limit	Duty Cycle = 50% Duty Cycle = 75% (Note 4)	● ●	1.25 0.9	1.9 1.6	3.0 2.6	A A
V_{SAT}	CCFL Switch On Resistance	CCFL I_{SW} = 1A	●		0.6	1.0	Ω
$\frac{\Delta I_Q}{\Delta I_{SW}}$	Supply Current Increase During CCFL Switch On Time	CCFL I_{SW} = 1A			20	30	mA/A
	DAC Resolution				6		Bits
	DAC Full-Scale Current	$V(I_{OUT})$ = 0.465V	 ●	98 96	100 100	102 104	µA µA
	DAC Zero Scale Current	$V(I_{OUT})$ = 0.465V	●			±200	nA
	DAC Differential Nonlinearity		●		±0.1	±1	LSB
	DAC Supply Voltage Rejection	3V ≤ V_{CC} ≤ 6.5V, I_{OUT} = Full Scale, $V(I_{OUT})$ = 0.465V	●		0.2	2	LSB
I_{IN}	Logic Input Current	0V ≤ V_{IN} ≤ V_{CC}	●			±1	µA
V_{IH}	High Level Input Voltage	$\overline{ADR}$ $\overline{SMBSUS}$ SCL, SDA	● ● ●	V_{CC} – 0.3 2.4 1.4			V V V
V_{IL}	Low Level Input Voltage	$\overline{SMBSUS}$, $\overline{ADR}$ SCL, SDA	● ●			0.8 0.6	V V
V_{OL}	Low Level Output Voltage	I_{OUT} = 3mA, SDA Only I_{OUT} = 1.6mA, $\overline{SMBSUS}$ = 0V, Measured at $\overline{SHDN}$ Pin	● ●			0.4 0.4	V V
SMBus Timing (Notes 5, 6)							
f_{SMB}	SMB Operating Frequency		●	10		100	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		●	4.7			µs
$t_{HD:STA}$	Hold Time After (Repeated) Start Condition		●	4.0			µs
$t_{SU:STA}$	Repeated Start Condition Setup Time		●	4.7			µs
$t_{SU:STO}$	Stop Condition Setup Time		●	4.0			µs
$t_{HD:DAT}$	Data Hold Time		●	300			ns
$t_{SU:DAT}$	Data Setup Time		●	250			ns
t_{LOW}	Clock Low Period		●	4.7			µs
t_{HIGH}	Clock High Period		●	4.0		50	µs
t_f	Clock/Data Fall Time		●			300	ns
t_r	Clock/Data Rise Time		●			1000	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LT1786FCS: $T_J = T_A + (P_D)(100°C/W)$

Note 3: Does not include switch leakage.

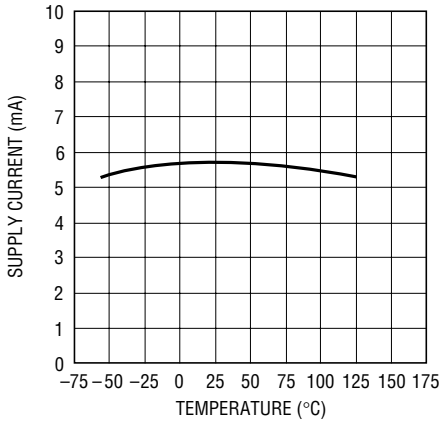
Note 4: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 1.4(1.393 – DC) for the LT1786F due to internal slope compensation circuitry.

Note 5: Timings for all signals are referenced to V_{IH} and V_{IL} signals.

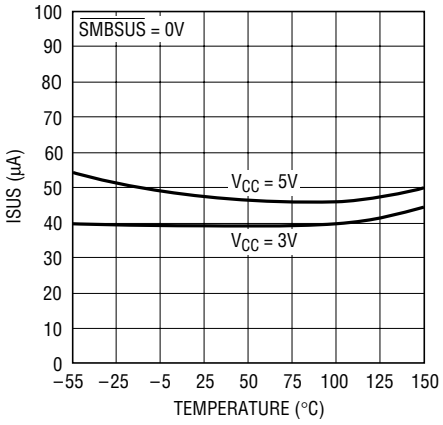
Note 6: These parameters are guaranteed by design and are not tested in production. Refer to the Timing Diagrams for additional information.

TYPICAL PERFORMANCE CHARACTERISTICS

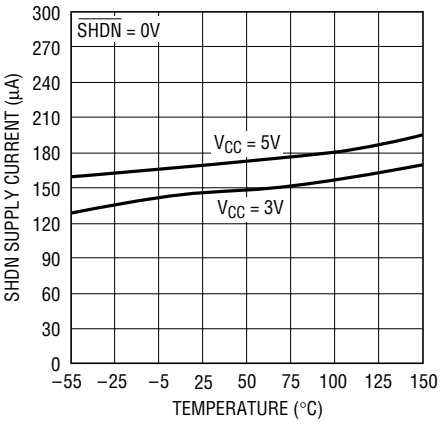
Supply Current vs Temperature



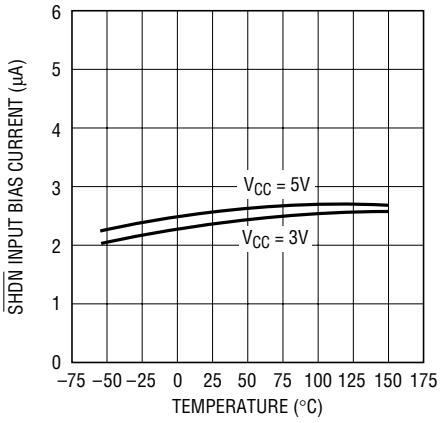
ISUS Current vs Temperature



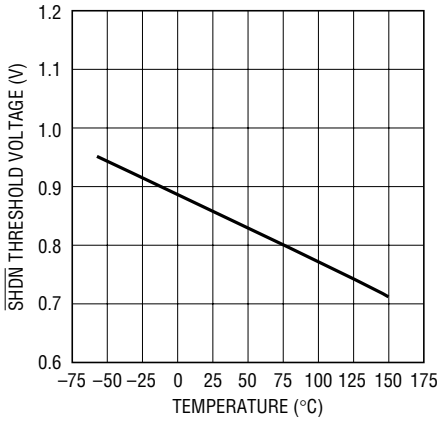
SHDN Supply Current vs Temperature



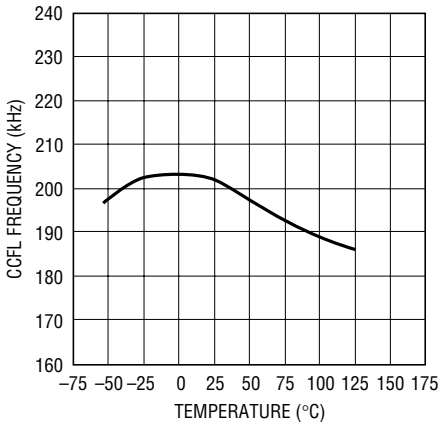
SHDN Input Bias Current vs Temperature



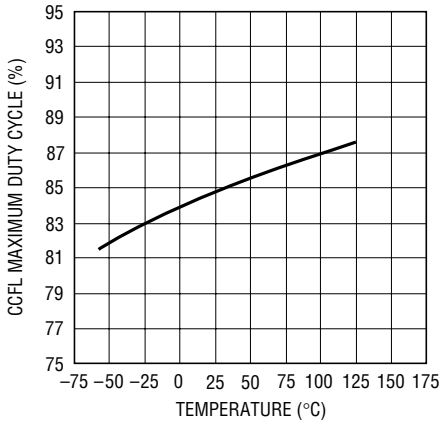
SHDN Threshold Voltage vs Temperature



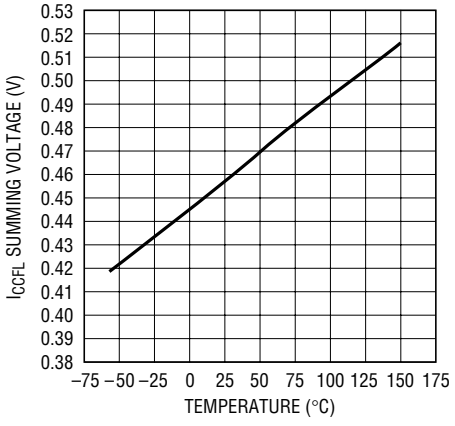
Frequency vs Temperature



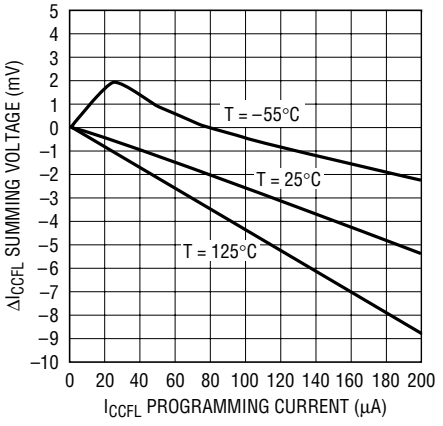
Maximum Duty Cycle vs Temperature



I_{CCFL} Summing Voltage vs Temperature

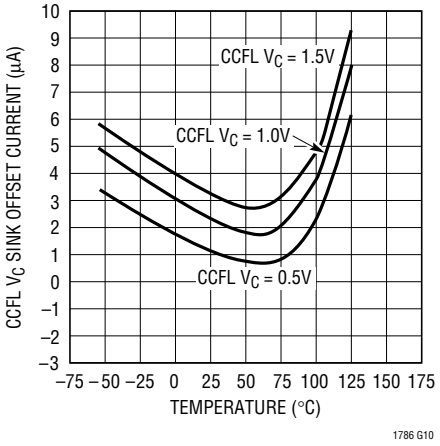


I_{CCFL} Summing Voltage Load Regulation

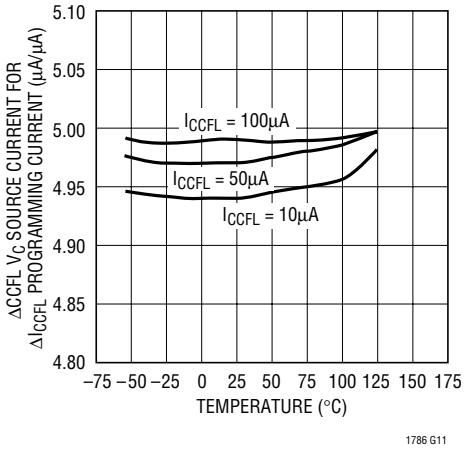


TYPICAL PERFORMANCE CHARACTERISTICS

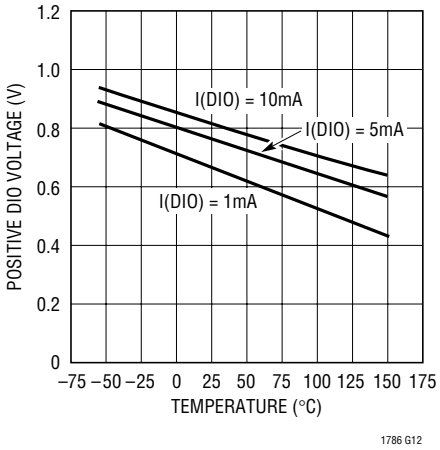
V_C Sink Offset Current vs Temperature



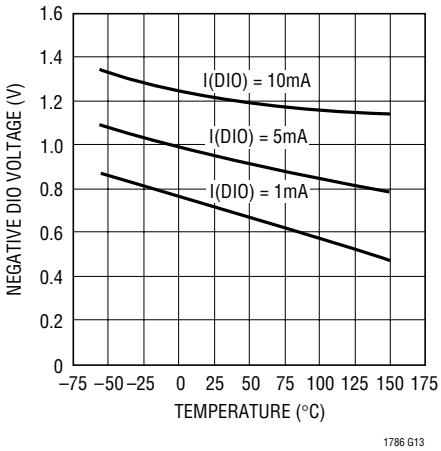
ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current vs Temperature



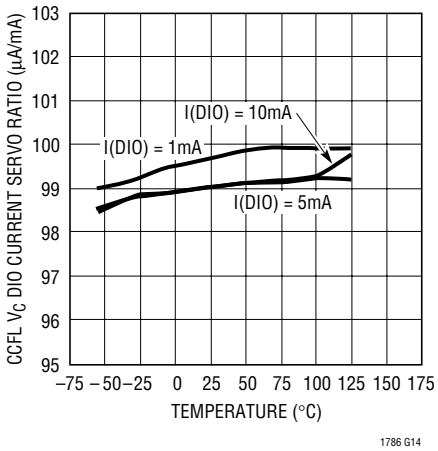
Positive DIO Voltage vs Temperature



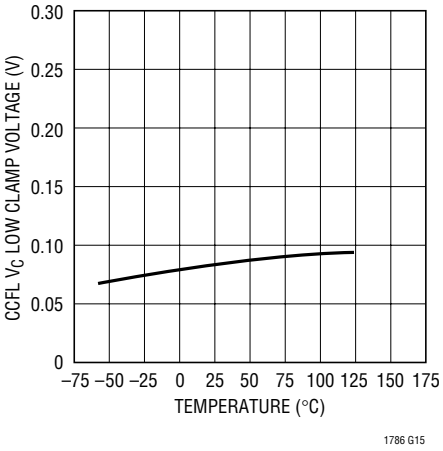
Negative DIO Voltage vs Temperature



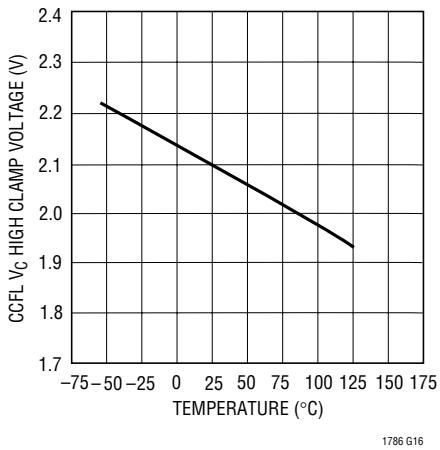
V_C to DIO Current Servo Ratio vs Temperature



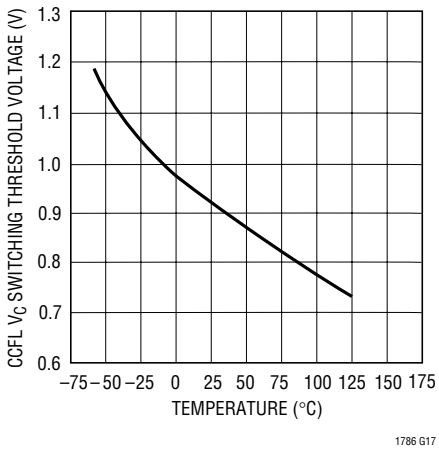
V_C Low Clamp Voltage vs Temperature



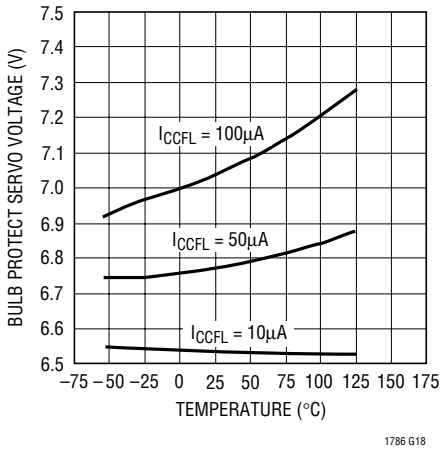
V_C High Clamp Voltage vs Temperature



V_C Switching Threshold vs Temperature

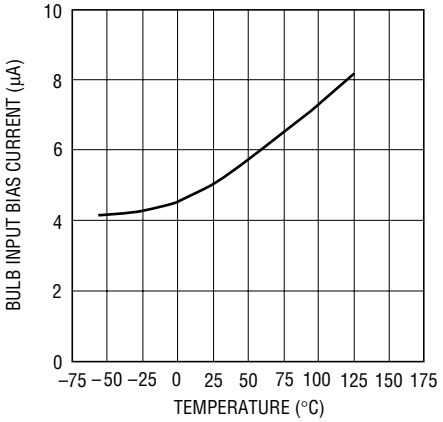


BULB Protect Servo Voltage vs Temperature



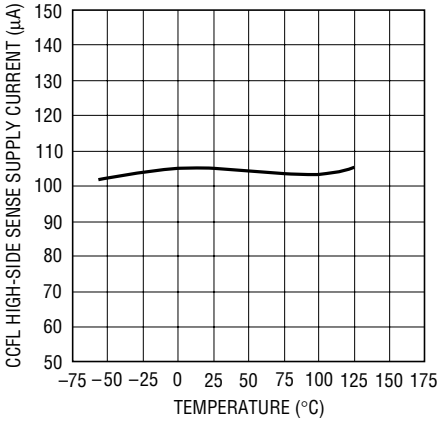
TYPICAL PERFORMANCE CHARACTERISTICS

BULB Input Bias Current vs Temperature



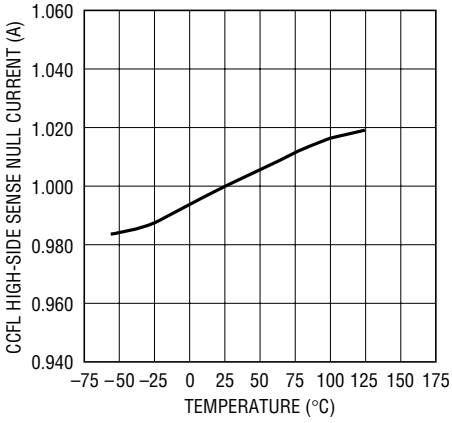
1787 G19

High-Side Sense Supply Current vs Temperature



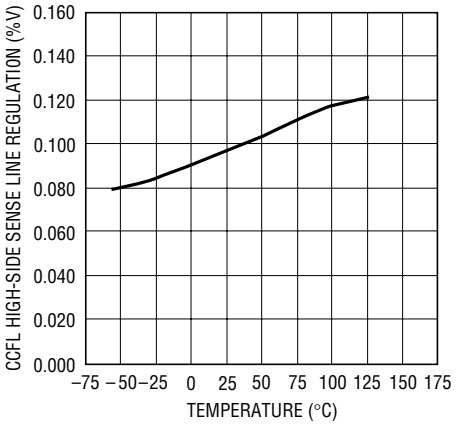
1786 G20

High-Side Sense Null Current vs Temperature



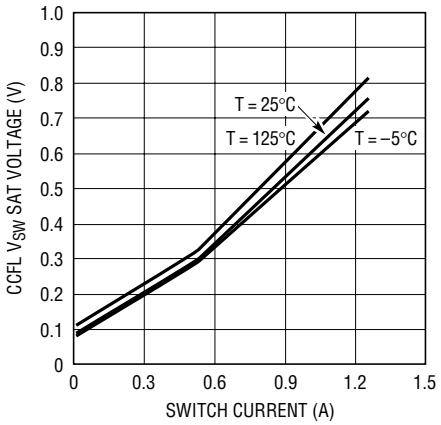
1786 G21

High-Side Sense Null Current Line Regulation vs Temperature



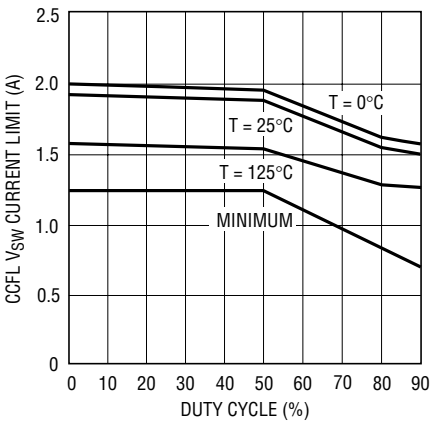
1786 G22

V_{SW} Sat Voltage vs Switch Current



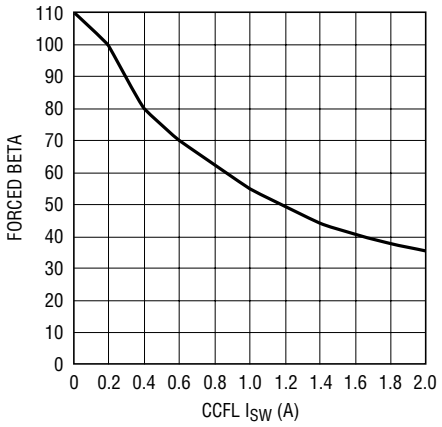
1787 G23

V_{SW} Current Limit vs Duty Cycle



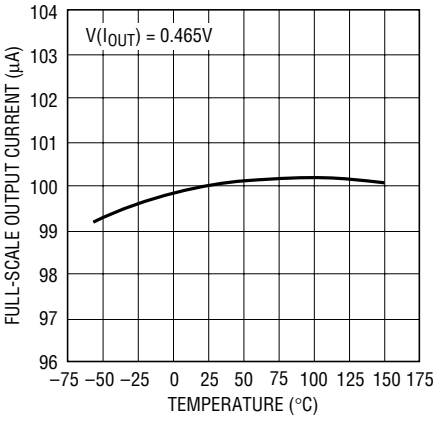
1786 G24

Forced Beta vs I_{SW} on V_{SW}



1786 G25

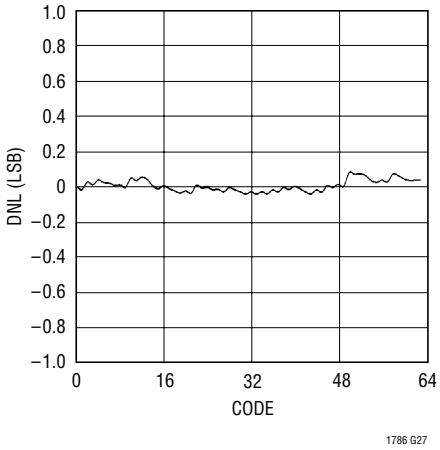
Full-Scale Output Current vs Temperature



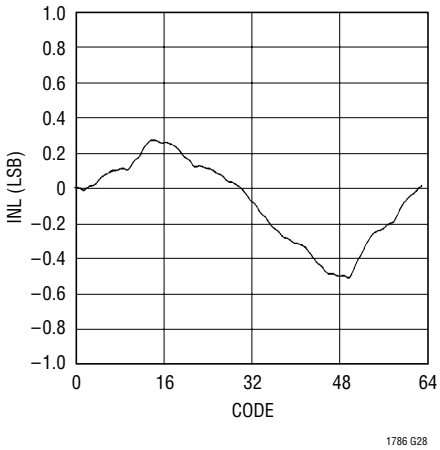
1786 G26

TYPICAL PERFORMANCE CHARACTERISTICS

DNL vs Code



INL vs Code



PIN FUNCTIONS

CCFL PGND (Pin 1): This pin is the emitter of an internal NPN power switch. CCFL switch current flows through this pin and permits internal, switch-current sensing. The regulator provides a separate analog ground and power ground to isolate high current ground paths from low current signal paths. Linear Technology recommends the use of star-ground layout techniques.

I_{CCFL} (Pin 2): This pin is the input to the CCFL lamp current programming circuit. This pin internally regulates to 465mV. The pin accepts a DC input current signal of 0µA to 100µA full scale from the DAC. This input signal is converted to a 0µA to 500µA source current at the CCFL V_C pin. As input programming current increases, the regulated lamp current increases.

DIO (Pin 3): This pin is the common connection between the cathode and anode of two internal diodes. The remaining terminals of the two diodes connect to ground. In a grounded-lamp configuration, DIO connects to the low voltage side of the lamp. Bidirectional lamp current flows in the DIO pin and thus the diodes conduct alternately on half cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL V_C pin. This current nulls against the source current provided by the lamp-current programmer circuit. A single capacitor on the CCFL V_C pin provides both stable loop compensation and an averaging function to the half-wave-rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current. This scheme reduces the number of loop compensation components and permits faster loop transient response in comparison to previously published circuits. If a floating lamp configuration is used, ground the DIO pin.

CCFL V_C (Pin 4): This pin is the output of the lamp current programmer circuit and the input of the current comparator for the CCFL regulator. Its uses include frequency compensation, lamp-current averaging for grounded-lamp circuits and current limiting. The voltage on the CCFL V_C pin determines the current trip level for switch turn-off. During normal operation this pin sits at a voltage between 0.95V (zero switch current) and 2.1V (maximum switch current) with respect to analog ground (AGND). This pin has a high impedance output and permits external voltage clamping to adjust current limit. A single capacitor to ground provides stable loop compensation. This simplified loop compensation method permits the CCFL regulator to exhibit single-pole transient response behavior and virtually eliminates transformer output overshoot.

PIN FUNCTIONS

AGND (Pin 5): This is the low current analog ground. It is the negative sense terminal for the internal 1.24V reference and the I_{CCFL} summing voltage in the LT1786F. Connect low current signal paths that terminate to ground and frequency compensation components that terminate to ground directly to this pin for best regulation and performance.

$\overline{SHDN}$ (Pin 6): Pulling this pin low causes regulator shutdown with quiescent current typically reduced to 150µA. In this condition, the DAC circuitry remains alive and the DAC I_{OUT} level is maintained. If this pin is not used, use a pull-up resistor to force a logic high level (maximum of 6V). The pin can be floated and an internal current source will pull the pin to a logic high level. However, poor PCB layout techniques can permit switching noise to inject into this pin and cause erratic operation. LTC recommends the use of a pull-up resistor. If the SMBSUS pin is pulled low or Bit 7 = 1 in the Command Byte, complete IC shutdown is enabled. An internal open drain N-channel device turns on and pulls the $\overline{SHDN}$ pin low. The N-channel can sink up to 1.6mA.

$\overline{SMBSUS}$ (Pin 7): Pulling this pin low causes complete shutdown for the IC with quiescent current typically reduced to 40µA. In this SMBus suspend condition, the DAC retains its last output current setting and returns to this level when the logic low signal at this pin is removed. If this pin is not used, use a pull-up resistor to force a logic high level or tie it directly to V_{CC}. Poor PCB layout techniques can permit switching noise to inject into this pin and cause erratic operation. A small value capacitor may be required to filter out this noise. Setting Bit 7 = 1 in the Command Byte also enables an SMBus suspend condition. Enabling an SMBus suspend condition turns on an internal open drain N-channel device which pulls the $\overline{SHDN}$ pin low. The N-channel device sinks up to 1.6mA at the $\overline{SHDN}$ pin.

ADR (Pin 8): This is the SMBus address select pin. Tie this pin to either V_{CC} or GND to select one of two SMBus addresses to which the LT1786F will respond. If the ADR pin is tied to GND, the SMBus address is set to 5A (HEX) and the DAC I_{OUT} powers up to zero scale. If the ADR pin is tied to V_{CC}, the SMBus address is set to 58 (HEX) and the DAC I_{OUT} powers up to half scale. If a different value is required for the DAC I_{OUT} on power-up, use the $\overline{SHDN}$ pin to keep the CCFL regulator off until the required value has been programmed for the DAC via the SMBus.

SDA (Pin 9): This is the SMBus bidirectional data input and digital output pin. Data is shifted into the SDA pin and acknowledged by the SDA pin. SDA is a high impedance pin while data is shifted into the pin and an open-drain N-channel output during acknowledges. SDA requires a pull-up resistor or current source to V_{CC}.

SCL (Pin 10): This is the SMBus clock input pin. Data is shifted into the SDA pin at the rising edges of the SCL clock during data transfer. SCL is a high impedance pin. SCL requires a pull-up resistor or current source to V_{CC}.

I_{OUT} (Pin 11): This pin is the current output for the DAC and provides a full-scale output current of 100µA ±4µA over temperature. Initial accuracy is 100µA ±2µA.The pin can be biased from –10V to (V_{CC} – 1.3V). This pin is typically tied directly to the I_{CCFL} pin and provides the programming current which sets the operating lamp current. The I_{OUT} pin has very little bias voltage change when tied to the I_{CCFL} pin as I_{CCFL} is regulated. The programming current is sourced from the I_{OUT} pin and sunk by the I_{CCFL} pin.

V_{CC} (Pin 12): This is the supply pin for the LT1786F. The IC accepts an input voltage range of 3V minimum to 6.5V maximum with little change in quiescent current (zero switch current). An internal, low-dropout regulator provides a 2.4V supply for most of the internal circuitry. Supply current increases as switch current increases at a rate approximately 1/50 of switch current. This corresponds to a forced Beta of 50 for the power switch. The IC incorporates undervoltage lockout by sensing regulator dropout and locking out switching for input voltages below 2.5V. Hysteresis is not used to maximize the range of input voltage. The typical input voltage is a 3.3V or 5V logic supply.

PIN FUNCTIONS

ROYER (Pin 13): This pin connects to the center-tapped primary of the Royer converter and is used with the BAT pin in a floating-lamp configuration where lamp current is controlled by sensing Royer primary-side converter current. This pin is the inverting terminal of a high-side current sense amplifier. The typical quiescent current is 50μA into the pin. If the CCFL regulator is not used in a floating-lamp configuration, tie the Royer and BAT pins together.

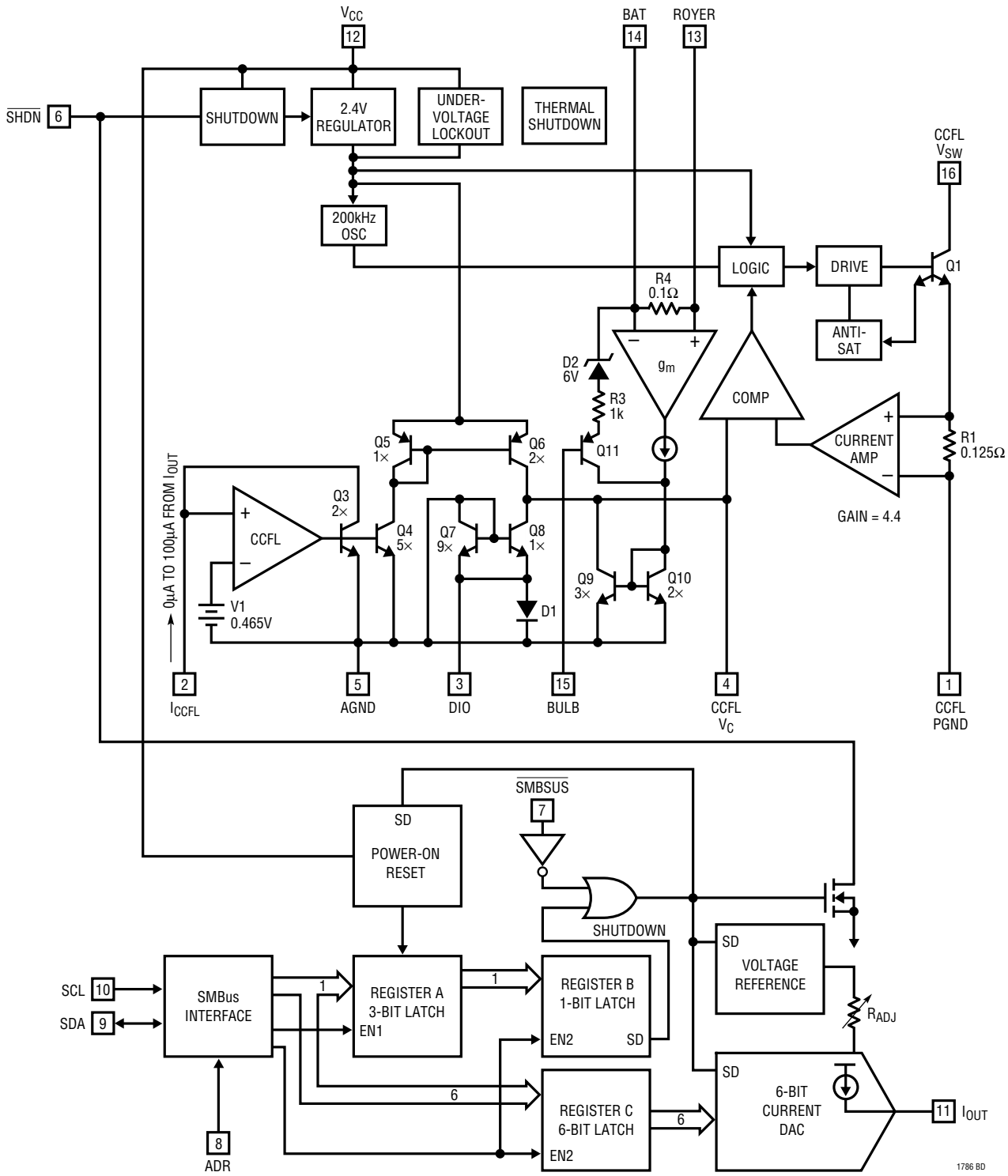
BAT (Pin 14): This pin connects to the battery or AC wall adapter voltage from which the CCFL Royer converter operates. This voltage is typically higher than the V_{CC} supply voltage but can equal V_{CC} if V_{CC} is a 5V logic supply. The BAT voltage must be at least 2.1V greater than the internal 2.4V regulator or 4.5V. This pin provides biasing for the lamp-current programming block, is used with the Royer pin for floating-lamp configurations and connects to one input for the open-lamp protection circuitry. For floating-lamp configurations, this pin is the noninverting terminal of a high-side current sense amplifier. The typical quiescent current is 50μA into the pin. The BAT and Royer pins monitor the primary-side Royer converter current through an internal 0.1Ω topside current sense resistor. A 0A to 1A primary-side, center tap converter current is translated to an input signal range of 0mV to 100mV for the current sense amplifier. This input range translates to a 0μA to 500μA sink current at the CCFL V_C pin that nulls against the source current provided by the programmer circuit. The BAT pin also connects to the topside of the internal clamp between the BAT and BULB pins that is used for open-lamp protection.

BULB (Pin 15): This pin connects to the low side of a 7V threshold comparator between the BAT and BULB pins. This circuit sets the maximum voltage level across the primary side of the Royer converter under all operating conditions and limits the maximum secondary output under start-up conditions or open-lamp conditions. This eases transformer voltage rating requirements. Set the voltage limit to ensure lamp start-up with worst-case, lamp start voltages and cold temperature, system operating conditions. The BULB pin connects to the junction of an external divider network. The divider network connects from the center tap of the Royer transformer or the actual battery supply voltage to the topside of the current source "tail inductor." A capacitor across the top of the divider network filters switching ripple and sets a time constant that determines how quickly the clamp activates. When the comparator activates, sink current is generated to pull the CCFL V_C pin down. This action transfers the entire regulator loop from current mode operation into voltage mode operation.

CCFL V_{SW} (Pin 16): This pin is the collector of the internal NPN power switch for the CCFL regulator. The power switch provides a minimum of 1.25A. Maximum switch current is a function of duty cycle as internal slope compensation ensures stability with duty cycles greater than 50%. Using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state yields fast switching times and high efficiency operation. The ratio of switch current to driver current is about 50:1.

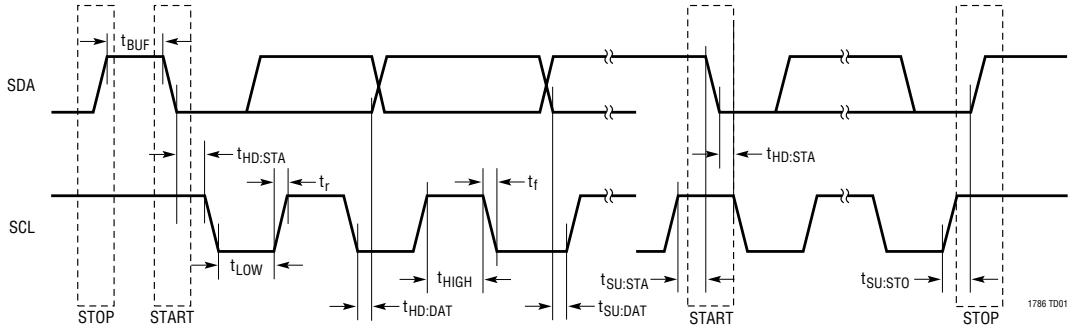
BLOCK DIAGRAM

LT1786F SMBus Programmable CCFL Switching Regulator

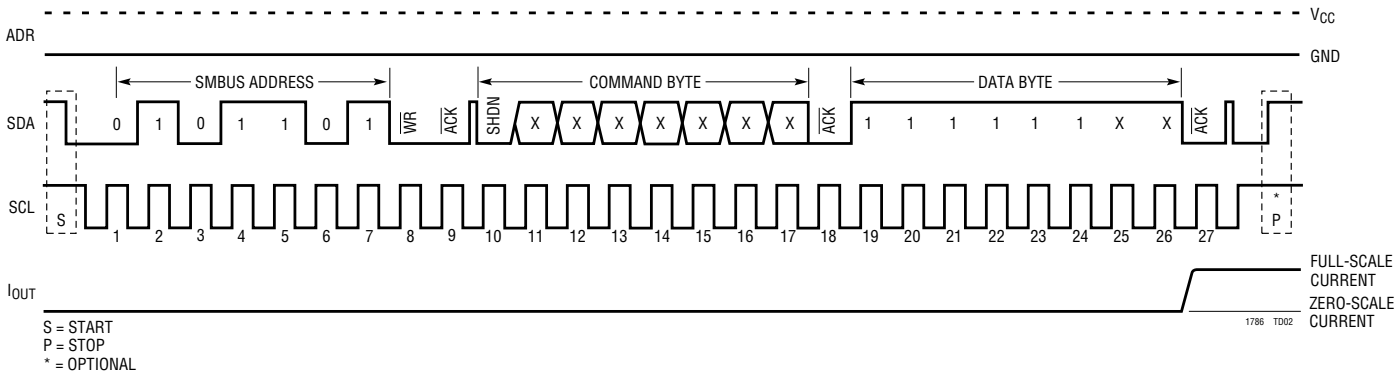


TIMING DIAGRAMS

Timing for SMBus Interface



Operating Sequence
SMBus Write Byte Protocol, with SMBus Address = 0101101B,
Command Byte = 0XXXXXXXB and Data Byte = 111111XXB



APPLICATIONS INFORMATION

Introduction

Current generation portable computers and instruments use backlit Liquid Crystal Displays (LCDs). Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency in back lighting the display. Providing the most light out for the least amount of input power is the most important goal. These lamps require high voltage AC to operate, mandating an efficient high voltage DC/AC converter. The lamps operate from DC, but migration effects damage the lamp and shorten its lifetime. Lamp drive should contain zero DC component. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This minimizes EMI and RF emissions. Such emissions can interfere with other devices and can also degrade overall operating efficiency. Sinusoidal CCFL drive maximizes current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

The small size and battery-powered operation associated with LCD equipped apparatus dictate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply can be responsible for almost 50% of the

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battery drain. Additionally, all components, including PC board and hardware, usually must fit within the LCD enclosure with a height restriction of 5mm to 10mm.

The CCFL regulator drives an inductor that acts as a switched-mode current source for a current-driven Royer-class converter with efficiencies as high as 90%. The control loop forces the CCFL PWM to modulate the average inductor current to maintain constant current in the lamp. The constant current value, and thus lamp intensity, is programmable. This drive technique provides a wide range of intensity control. A unique lamp-current programming block permits either grounded lamp or floating lamp configurations. Grounded lamp circuits directly sense one-half of average lamp current. Floating lamp circuits directly sense the Royer's primary-side converter current. Floating-lamp circuits provide symmetric differential drive to the lamp and reduce the parasitic loss from stray lamp-to-frame capacitance, extending illumination range.

Block Diagram Operation

The LT1786F is a fixed frequency, current mode switching regulator. A fixed frequency, current mode switcher controls switch duty cycle directly by switch current rather than by output voltage. Referring to the block diagram for the LT1786F, the switch turns ON at the start of each oscillator cycle. The switch turns OFF when switch current reaches a predetermined level. The control of output lamp current is obtained by using the output of a unique programming block to set current trip level. The current mode switching technique has several advantages. First, it provides excellent rejection of input voltage variations. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

The LT1786F incorporates a low dropout internal regulator that provides a 2.4V supply for most of the internal circuitry. This low dropout design allows input voltage to vary from 3V to 6.5V with little change in quiescent current. An active low shutdown pin typically reduces total supply current to 150µA by shutting off the 2.4V regulator and locks out switching action for standby operation. The IC incorporates undervoltage lockout by sensing regulator dropout and locking out switching below about 2.5V. The regulator also provides thermal shutdown protection that locks out switching in the presence of excessive junction temperatures.

A 200kHz oscillator is the basic clock for all internal timing. The oscillator turns on the output switch via its own logic and driver circuitry. Adaptive anti-sat circuitry detects the onset of saturation in the power switch and adjusts base drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides rapid turn-off of the switch. The CCFL power switch is guaranteed to provide a minimum of 1.25A in the LT1786F. The antisat circuitry provides a ratio of switch current to driver current of about 50:1.

Digital Interface

The LT1786F communicates with an SMBus host using the standard 2-wire SMBus interface. The Timing Diagram shows the signals on the SMBus. The two bus lines SDA and SCL must be high when the bus is not in use. External pull-up resistors or current sources are required at these lines.

The LT1786F is a receive-only (slave) device. The master must apply the following Write Byte protocol to communicate with the LT1786F:

1	7	1	1	8	1	8	1	1
S	Slave Address	WR	A	Command Byte	A	Data Byte	A	P

S = Start Conditon, WR = Write Bit, A = Acknowledge Bit, P = Stop Condition

The master initiates communication with the LT1786F with a START condition (see SMBus Operating Sequence) and a 7-bit address followed by the write bit = 0. The LT1786F acknowledges and the master delivers the command byte. The LT1786F acknowledges and latches the active bits of the command byte into register A (see Block Diagram) at the falling edge of the acknowledge pulse. The master sends the data byte and the LT1786F acknowledges the data byte. The data byte is latched into register C at the falling edge of the final acknowledge pulse and the DAC current output assumes the new 6-bit data

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value (see Block Diagram). A STOP condition is optional. The command code and data byte are defined with the following format:

Command Code

7	6	5	4	3	2	1	0
SHDN	X	X	X	X	X	X	X

Data Byte

7	6	5	4	3	2	1	0
D5	D4	D3	D2	D1	D0	X	X

SHDN: 0 for normal operation, 1 for shutdown
D5 to D0: DAC Data Byte Bits, D5 is the Most Significant Bit

START and STOP Conditions

At the beginning of any SMBus communication, the master must transmit a START condition by switching SDA from high to low while SCL is high. When a master has finished communicating with a slave device, a STOP condition is issued by switching SDA from low to high while SCL is high. The SMBus is then free for communication with another SMBus device.

Early STOP Conditions

The LT1786F recongnizes a STOP condition at any point in the SMBus communication sequence. If the STOP occurs prematurely before the data byte is acknowledged in the Write Byte protocol, the DAC output current value is not updated; otherwise internal register C is updated with the new data and the DAC output current changes correspondingly.

The Slave Address

The LT1786F responds to one of two 7-bit addresses. The first five bits have been factory programmed to 01011. The last two address bits are programmed by the user by tying the ADR pin to V_{CC} or GND (see functional table)

ADR	SMBus ADDRESS	DAC POWER-UP VALUE
GND	0101101	Zero Scale
V_{CC}	0101100	Midscale

6-Bit Current Output DAC

The 6-bit current output DAC is guaranteed monotonic and is digitally adjustable in 63 equal steps. On power-up, if ADR connects to V_{CC}, the 6-bit internal register C (see Block Diagram) resets to 100000B and the DAC output is set to midrange. On power-up, if ADR connects to ground, register C resets to 000000B and the DAC output is set to zero. For the LT1786F, the current source output (I_{OUT}) can be biased from –10V to (V_{CC} – 1.3V). Full-scale current is trimmed to ±2% at room temperature and ±4% over the commercial temperature range.

Shutdown

Three methods may be employed to shut down the LT1786F (see Block Diagram).

The LT1786F enters SMBus suspend mode if a logic low level is applied to the $\overline{SMBSUS}$ pin or a logic high level is applied to Bit 7 in the Command Byte of the SMBus communication sequence. In SMBus suspend mode, supply current typically drops to 40µA and the last output current setting is internally retained. The DAC resumes this level upon its return to normal operation. Enabling an SMBus suspend condition also turns on an open-drain N-channel MOSFET which pulls the $\overline{SHDN}$ pin low. The N-channel device sinks up to 1.6mA at the $\overline{SHDN}$ pin and its logic low level is guaranteed to less than 0.4V.

The LT1786F enters regulator shutdown mode if a logic low level is applied to the $\overline{SHDN}$ pin. In this mode, supply current typically drops to 150µA, the switching regulator circuitry is shut down and the DAC is kept alive. The DAC output current setting is maintained. This feature can be used to program the DAC to a desired output current level (other than the preset zero-scale or midscale level defined by the selected SMBus address) before allowing the CCFL regulator to turn on.

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LT1786F SMBus Lookup Tables

SMBus Address Byte Table

ADR	DECIMAL	BINARY	HEX	I_{OUT} POWER-UP VALUE
GND	90	0101101	5A	Zero Scale
V_{CC}	88	0101100	58	Midscale

Bit 0 (LSB) in the SMBus Address is the Write Bit = 0

SMBus Command Byte Table

DECIMAL	BINARY	HEX	MODE
0-127	0XXXXXXX	00-7F	Normal
128-255	1XXXXXXX	80-FF	Shutdown

X = Don't Care

SMBus Data Byte Table

DECIMAL	BINARY	HEX	I_{OUT} (μA)
0	000000XX	00-03	0.000
1	000001XX	04-07	1.587
2	000010XX	08-0B	3.175
3	000011XX	0C-0F	4.762
4	000100XX	10-13	6.349
5	000101XX	14-17	7.937
6	000110XX	18-1B	9.524
7	000111XX	1C-1F	11.111
8	001000XX	20-23	12.698
9	001001XX	24-27	14.286
10	001010XX	28-2B	15.873
11	001011XX	2C-2F	17.460
12	001100XX	30-33	19.048
13	001101XX	34-37	20.635
14	001110XX	38-3B	22.222
15	001111XX	3C-3F	23.810
16	010000XX	40-43	25.397
17	010001XX	44-47	26.984
18	010010XX	48-4B	28.571
19	010011XX	4C-4F	30.159
20	010100XX	50-53	31.746
21	010101XX	54-57	33.333
22	010110XX	58-5B	34.921
23	010111XX	5C-5F	36.508
24	011000XX	60-63	38.095
25	011001XX	64-67	39.683
26	011010XX	68-6B	41.270
27	011011XX	6C-6F	42.857
28	011100XX	70-73	44.444
29	011101XX	74-77	46.032
30	011110XX	78-7B	47.619
31	011111XX	7C-7F	49.206
32	100000XX	80-83	50.794
33	100001XX	84-87	52.381
34	100010XX	88-8B	53.968
35	100011XX	8C-8F	55.556
36	100100XX	90-93	57.143
37	100101XX	94-97	58.730
38	100110XX	98-9B	60.317
39	100111XX	9C-9F	61.905
40	101000XX	A0-A3	63.492
41	101001XX	A4-A7	65.079
42	101010XX	A8-AB	66.667
43	101011XX	AC-AF	68.254
44	101100XX	B0-B3	69.841
45	101101XX	B4-B7	71.429
46	101110XX	B8-BB	73.016
47	101111XX	BC-BF	74.603
48	110000XX	C0-C3	76.190
49	110001XX	C4-C7	77.778
50	110010XX	C8-CB	79.365
51	110011XX	CC-CF	80.952
52	110100XX	D0-D3	82.540
53	110101XX	D4-D7	84.127
54	110110XX	D8-DB	85.714
55	110111XX	DC-DF	87.302
56	111000XX	E0-E3	88.889
57	111001XX	E4-E7	90.476
58	111010XX	E8-EB	92.063
59	111011XX	EC-EF	93.651
60	111100XX	F0-F3	95.238
61	111101XX	F4-F7	96.825
62	111110XX	F8-FB	98.413
63	111111XX	FC-FF	100.000

X = Don't Care, I_{OUT} = Ideal Value

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Simplified Lamp Current Programming

A programming block in the LT1786F controls lamp current, permitting either grounded lamp or floating lamp configurations. Grounded configurations control lamp current by directly controlling one-half of actual lamp current and converting it to a feedback signal to close a control loop. Floating configurations control lamp current by directly controlling the Royer's primary-side converter current and generating a feedback signal to close a control loop.

Previous backlighting solutions have used a traditional error amplifier in the control loop to regulate lamp current. This approach converted an RMS current into a DC voltage for the input of the error amplifier. This approach used several time constants in order to provide stable loop frequency compensation. This compensation scheme meant that the loop had to be fairly slow and that output overshoot with start-up or overload conditions had to be carefully evaluated in terms of transformer stress and breakdown voltage requirements.

The LT1786F eliminates the error amplifier concept entirely and replaces it with a lamp current programming block. This block provides an easy-to-use interface to program lamp current. The programmer circuit also reduces the number of time constants in the control loop by combining the error signal conversion scheme and frequency compensation into a single capacitor. The control loop thus exhibits the response of a single pole system, allows for faster loop transient response and virtually eliminates overshoot under start-up or overload conditions.

Lamp current is programmed at the input of the programmer block, the I_{CCFL} pin. This pin is the input of a shunt regulator and accepts a DC input current signal of 0µA to 100µA from the DAC. This input signal is converted to a 0µA to 500µA source current at the CCFL V_C pin. The programmer circuit is simply a current-to-current converter with a gain of five.

The I_{CCFL} pin is sensitive to capacitive loading and will oscillate with capacitance greater than 10pF. For example, loading the I_{CCFL} pin with a 1× or 10× scope probe causes oscillation and erratic CCFL regulator operation because of the probe's respective input capacitance. A current meter in series with the I_{CCFL} pin will also produce oscillation due to its shunt capacitance. Use a decoupling resistor of several kilohms between the I_{CCFL} pin and the I_{OUT} pin if excessive trace stray capacitance exists. Normally, this resistor is not required.

In some applications, the maximum programming current required at the I_{CCFL} pin for a maximum lamp current will be less than the full-scale output current of the DAC, which is 100µA. The system designer can either limit the maximum programming current through software built into the system, or use a current splitter which shunts a percentage of the full-scale current from the I_{CCFL} pin. A splitter circuit is illustrated in Figure 1. A divider string is used from a reference voltage to set up a voltage level equal to the I_{CCFL} summing voltage, or 465mV. The main current flowing in the divider string should be chosen to swamp out the effects of the shunted current into the divider string.

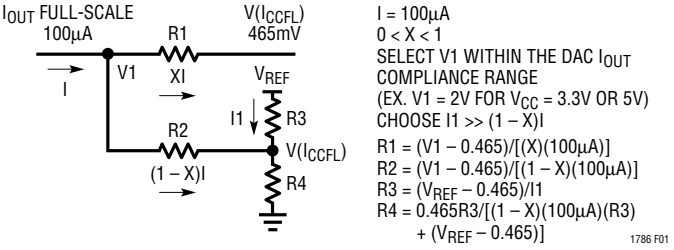

Figure 1

Grounded Lamp Configuration

In a grounded lamp configuration, the low voltage side of the lamp connects directly to the LT1786F DIO pin. This pin is the common connection between the cathode and anode of two internal diodes. In previous grounded lamp solutions, these diodes were discrete units and are now integrated onto the IC, saving cost and board space. Bidirectional lamp current flows in the DIO pin and thus, the diodes conduct alternately on half cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL V_C pin and nulls against the source current provided by the

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lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current.

The transfer function between lamp current and input programming current must be empirically determined and is dependent on the particular lamp/display housing combination used. The lamp and display housing are a distributed loss structure due to parasitic lamp-to-frame capacitance. This means that the current flowing at the high-voltage side of the lamp is higher than what is flowing at the DIO pin side of the lamp. The input programming current is set to control lamp current at the high-voltage side of the lamp, even though the feedback signal is the lamp current at the bottom of the lamp. This ensures that the lamp is not overdriven which can degrade the lamp's operating lifetime. Therefore, the full scale current of the DAC does not necessarily correspond to the current required to set maximum lamp current.

Floating Lamp Configuration

In a floating lamp configuration, the lamp is fully floating with no galvanic connection to ground. This allows the transformer to provide symmetric differential drive to the lamp. Balanced drive eliminates the field imbalance associated with parasitic lamp-to-frame capacitance and reduces "thermometering" (uneven lamp intensity along the lamp length) at low lamp currents.

Carefully evaluate display designs in relation to the physical layout of the lamp, its leads and the construction of the display housing. Parasitic capacitance from any high voltage point to DC or AC ground creates paths for unwanted current flow. This parasitic current flow degrades electrical efficiency and losses up to 25% have been observed in practice. As an example, at a Royer operating frequency of 60kHz, 1pF of stray capacitance represents an impedance of 2.65MΩ. With an operating lamp voltage of 400V and an operating lamp current of 6mA, the parasitic current is 150μA. This additional current must be supplied by the transformer secondary. Layout techniques that increase parasitic capacitance include long high voltage lamp leads, reflective metal foil around the lamp and displays supplied in metal enclosures. Losses for a good display are under 5%, whereas, losses for a bad display range from 5% to 25%. Lossy displays are the primary reason to use a floating lamp configuration. Providing symmetric, differential drive to the lamp reduces the total parasitic loss by one-half.

Maintaining closed-loop control of lamp current in a floating lamp configuration necessitates deriving a feedback signal from the primary side of the Royer transformer. Previous solutions have used an external precision shunt and high-side sense amplifier configuration. This approach has been integrated onto the LT1786F for simplicity of design and ease of use. An internal 0.1Ω resistor monitors the Royer converter current and connects between the input terminals of a high-side sense amplifier. A 0 – 1 Amp Royer primary-side, center-tap current is translated to a 0μA to 500μA sink current at the CCFL V_C pin to null against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the error sink current. Therefore, input programming current is related to average Royer converter current. Floating lamp circuits operate similarly to grounded lamp circuits except for the derivation of the feedback signal.

The transfer function between lamp current and input programming current must be empirically determined and is dependent upon a myriad of factors including lamp characteristics, display construction, transformer turns ratio and the tuning of the Royer oscillator. Once again, lamp current will be slightly higher at one end of the lamp and input programming current should be set for this higher level to ensure that the lamp is not overdriven.

The internal 0.1Ω high-side sense resistor on the LT1786F is rated for a maximum DC current of 1A. This resistor can be damaged by extremely high surge currents at start-up. The Royer converter typically uses a few microfarads of bypass capacitance at the center tap of the transformer. This capacitor charges up when the system is first powered by the battery pack or an AC wall adapter. The amount of current delivered at start-up can be very large if the total impedance in this path is small and the voltage source has high current capability. Linear Technology recommends

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the use of an aluminum electrolytic for the transformer center-tap bypass capacitor with an ESR greater than or equal to 0.5Ω. This lowers the peak surge currents to an acceptable level. In general, the wire and trace inductance in this path also help reduce the di/dt of the surge current. This issue only exists with floating lamp circuits as grounded lamp circuits do not make use of the high-side sense resistor.

Input Capacitor Type

Caution must be used in selecting the input capacitor type for switching regulators. Aluminum electrolytics are electrically rugged and the lowest cost, but are physically large to meet required ripple current ratings, and size constraints (especially height) may preclude their use. Ceramic capacitors are now available in larger values and their high ripple current and voltage rating make them ideal for input bypassing.

Solid tantalum capacitors would be a good choice except for a history of occasional failure when subjected to large current surges during start-up. The input bypass capacitor of regulators can see these high surges when a battery or high capacitance source is connected. Some manufacturers have developed tantalum capacitor lines specially tested for surge capability (AVX TPS series for instance), but even these units may fail if the input voltage surge approaches the capacitor's maximum voltage rating. AVX recommends derating the capacitor voltage by 2:1 for high surge applications.

Applications Support

Linear Technology invests an enormous amount of time, resources and technical expertise in understanding, designing and evaluating backlight/LCD contrast solutions for system designers. The design of an efficient and compact LCD backlight system is a study of compromise in a transduced electronic system. Every aspect of the design is interrelated and any design change requires complete re-evaluation for all other critical design parameters. Linear Technology has engineered one of the most complete test and evaluation setups for backlight designs and understands the issues and tradeoffs in achieving a compact, efficient and economical customer solution. Linear Technology welcomes the opportunity to discuss, design, evaluate and optimize any backlight/LCD contrast system with a customer. For further information on backlight/LCD contrast designs, consult the References.

References

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TYPICAL APPLICATION

Dual Transformer CCFL Power Supply

Space constraints may dictate utilization of two small transformers instead of a single, larger unit. Although this approach is somewhat more expensive, it can solve space problems and offers other attractive advantages. Figure 2's approach is essentially a "grounded lamp" LT1786F-based circuit. The transistors drive two transformer primaries in parallel. The transformer secondaries, stacked in series, provide the output. The relatively small transformers, each supplying half the load power, may be located directly at the lamp terminals. Aside from the obvious space advantage (particularly height), this arrangement minimizes parasitic wiring losses by eliminating high voltage lead length. Additionally, although the lamp receives differential drive, with its attendant low parasitic losses, the feedback signal is ground referred. Thus, the stacked secondaries afford floating lamp operating efficiency with grounded mode current certainty and line regulation.

L1 is directly driven, with winding 4-5 furnishing feedback in the normal fashion. L3, "slaved" to L1's and L3's interconnects must be laid out for low inductance to maintain waveform purity. The traces should be as wide as possible (e.g., 1/8") and overlaid to cancel inductive effects.

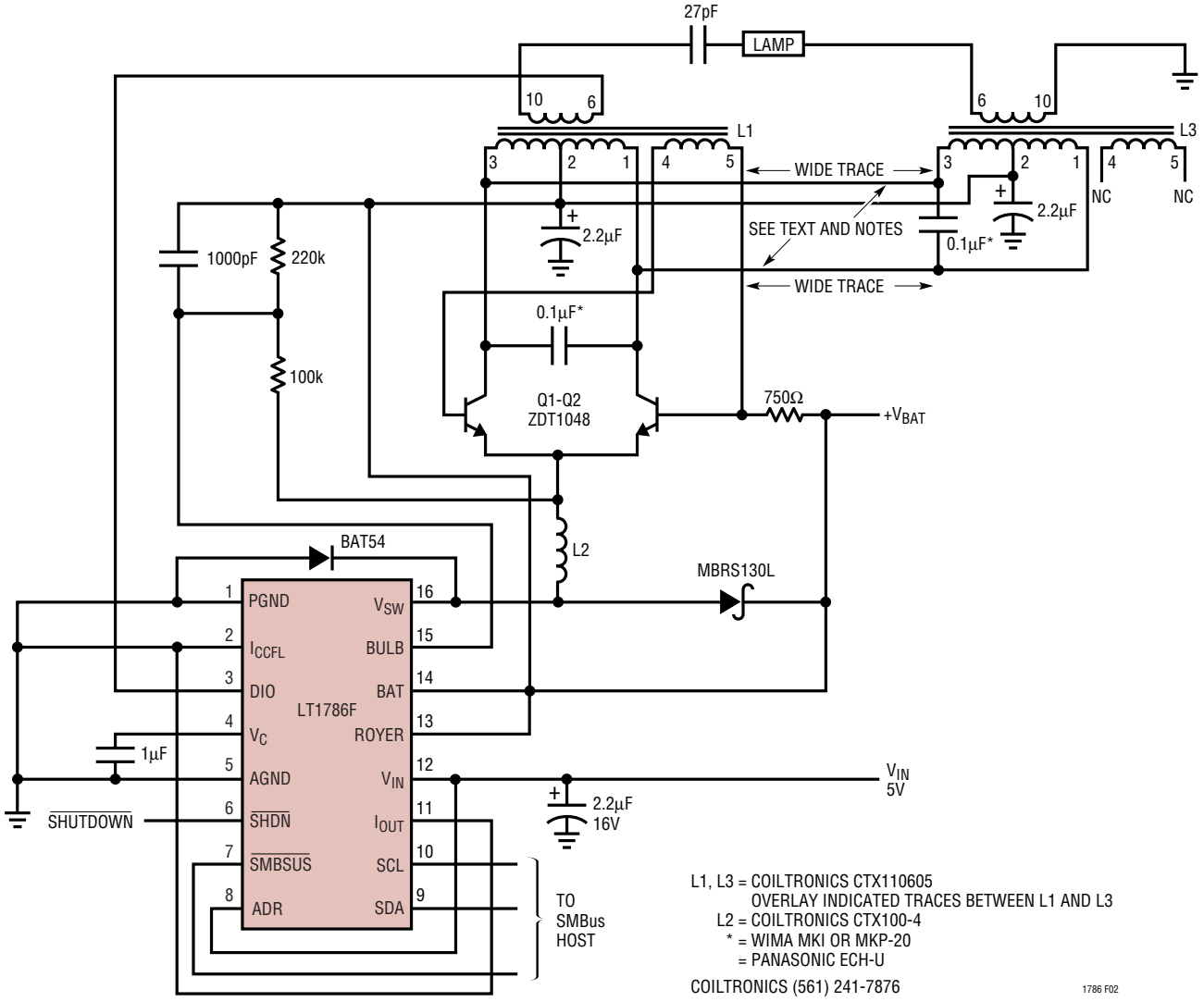
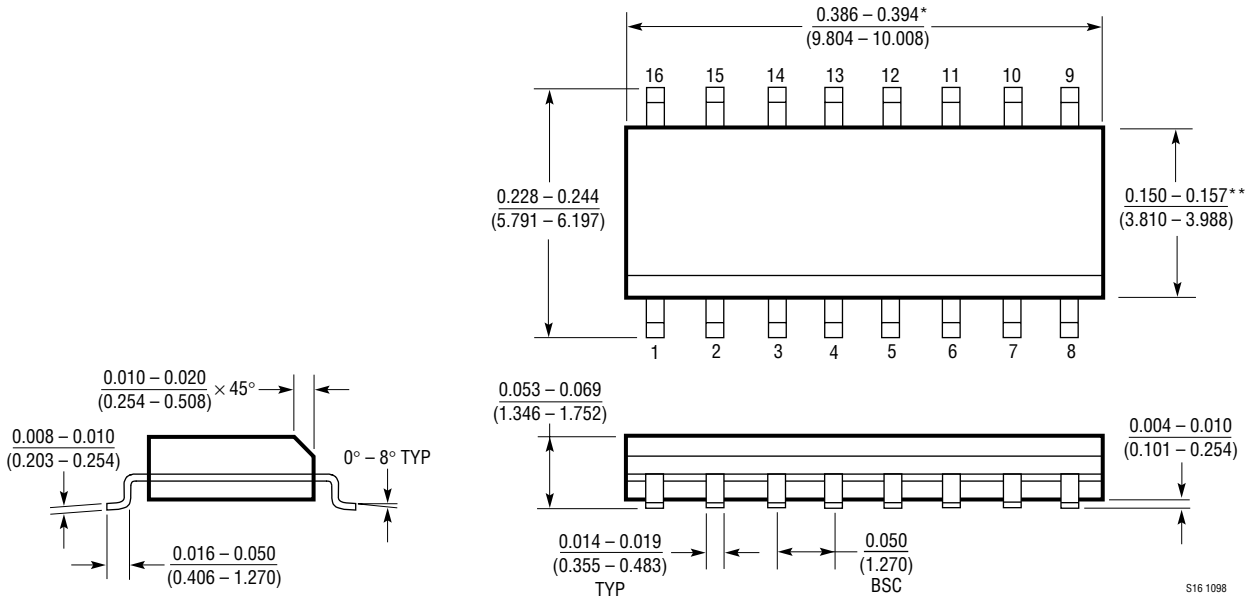


Figure 2. Dual Transformers Save Space and Minimize parasitic Losses While Maintaining Current Accuracy and Line Regulation. Trade-Off Is Increased Cost

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

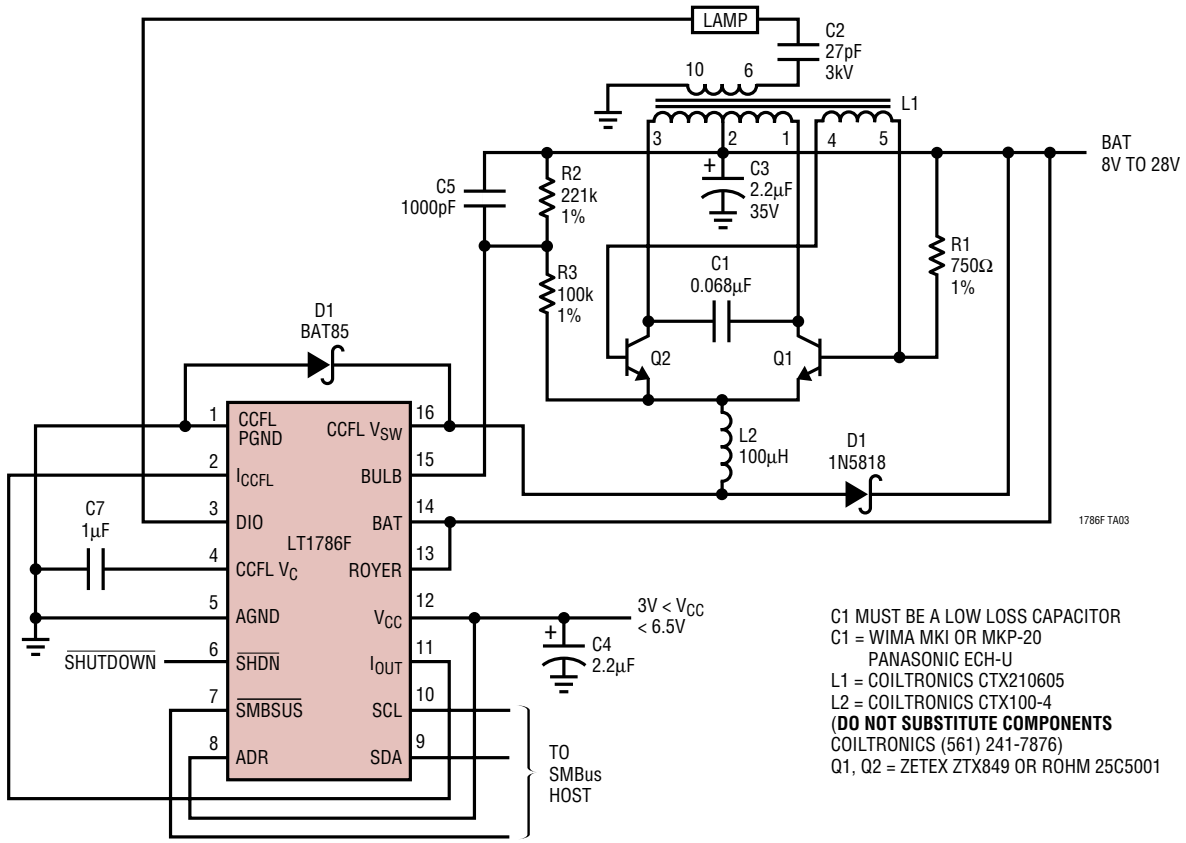


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

90% Efficient Grounded CCFL with 2-Wire SMBus Control of Lamp Current



C1 MUST BE A LOW LOSS CAPACITOR
C1 = WIMA MKI OR MKP-20
PANASONIC ECH-U
L1 = COILTRONICS CTX210605
L2 = COILTRONICS CTX100-4
(**DO NOT SUBSTITUTE COMPONENTS**
COILTRONICS (561) 241-7876)
Q1, Q2 = ZETEX ZTX849 OR ROHM 25C5001

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1172	Current Mode Switching Regulator for CCFL or LCD Contrast Control	1.25A, 100kHz
LT1173	Micropower DC/DC Converter for LCD Contrast Control	1A, 24kHz, Hysteretic
LT1182	Dual Current Mode Switching Regulator for CCFL and LCD Contrast Control	1.25A, 0.625A, 200kHz
LT1183	Dual Current Mode Switching Regulator for CCFL and LCD Contrast Control	1.25A, 0.625A, 200kHz
LT1184	Current Mode Switching Regulator for CCFL Control	1.25A, 200kHz
LT1184F	Current Mode Switching Regulator for CCFL Control	1.25A, 200kHz
LT1186F	DAC Programmable Current Mode Switching Regulator for CCFL Control	1.25A, 200kHz, SPI or Pulse Mode
LT1316	Micropower DC/DC Converter for LCD Contrast Control	Programmable Peak Current Limit
LT1372	Current Mode Switching Regulator for CCFL or LCD Contrast Contol	1.5A, 500kHz
LT1786	CCFL Controller for Wide Dimming Range and Maximum Lamp Lifetime	Multiple Lamp Capability, No Lamp Flicker, Precision Maximum and Minimum Lamp Currents Maximize Lamp Life

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