

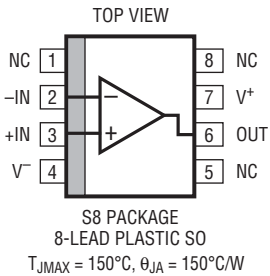
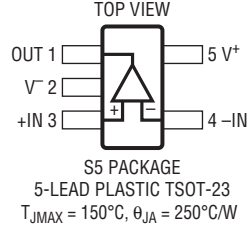
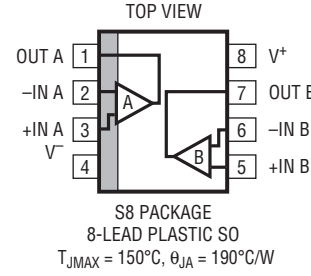
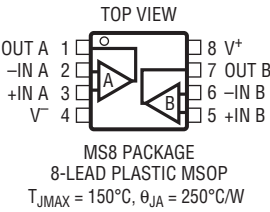
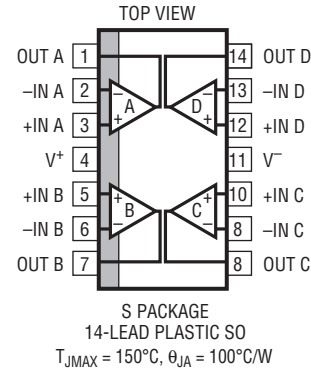
LT1722/LT1723/LT1724

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)	12.6V	Operating Temperature Range (Note 4) ...	-40°C to 85°C
Input Voltage.....	$\pm V_S$	Specified Temperature Range (Note 5)	-40°C to 85°C
Differential Input Voltage (Note 2)	$\pm 0.7V$	Maximum Junction Temperature	150°C
Input Current (Note 2).....	$\pm 10mA$	Storage Temperature Range	-65°C to 150°C
Output Short-Circuit Duration (Note 3)	Indefinite	Lead Temperature (Soldering, 10 sec).....	300°C

PIN CONFIGURATION

LT1722  S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$	LT1722  S5 PACKAGE 5-LEAD PLASTIC TSOT-23 $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 250^{\circ}C/W$	LT1723  S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 190^{\circ}C/W$
LT1723  MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 250^{\circ}C/W$	LT1724  S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 100^{\circ}C/W$	

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1722CS8#PBF	LT1722CS8#TRPBF	1722	8-Lead Plastic SO	0°C to 70°C
LT1722IS8#PBF	LT1722IS8#TRPBF	1722I	8-Lead Plastic SO	-40°C to 85°C
LT1722CS5#PBF	LT1722CS5#TRPBF	LTZB	5-Lead Plastic TSOT-23	0°C to 70°C
LT1722IS5#PBF	LT1722IS5#TRPBF	LTZB	5-Lead Plastic TSOT-23	-40°C to 85°C
LT1723CS8#PBF	LT1723CS8#TRPBF	1723	8-Lead Plastic SO	0°C to 70°C
LT1723IS8#PBF	LT1723IS8#TRPBF	1723I	8-Lead Plastic SO	-40°C to 85°C
LT1723CMS8#PBF	LT1723CMS8#TRPBF	LYC	8-Lead Plastic MSOP	0°C to 70°C
LT1723IMS8#PBF	LT1723IMS8#TRPBF	LTZA	8-Lead Plastic MSOP	-40°C to 85°C
LT1724CS#PBF	LT1724CS#TRPBF	LT1724CS	14-Lead Plastic SO	0°C to 70°C
LT1724IS#PBF	LT1724IS#TRPBF	LT1724IS	14-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

LT1722/LT1723/LT1724

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8		100 150	400 650	μV μV
I_{OS}	Input Offset Current			40	300	nA
I_B	Input Bias Current			40	300	nA
e_n	Input Noise Voltage	$f = 10\text{kHz}$		3.8		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current	$f = 10\text{kHz}$		1.2		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 3.5\text{V}$ Differential	5	35 50		$\text{M}\Omega$ $\text{k}\Omega$
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range + Input Voltage Range –		3.5	4 –4	–3.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 3.5\text{V}$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.3\text{V}$ to $\pm 5.5\text{V}$	78	90		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 3\text{V}$, $R_L = 500\Omega$ $V_{OUT} = \pm 3\text{V}$, $R_L = 150\Omega$	10 7	17 14		V/mV V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$ $R_L = 150\Omega$, $V_{IN} = \pm 10\text{mV}$	± 3.2 ± 3.1	± 3.8 ± 3.4		V V
I_{OUT}	Output Current	$V_{OUT} = \pm 3\text{V}$, 10mV Overdrive	23	50		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 1\text{V}$	35	90		mA
SR	Slew Rate	$A_V = -1$, (Note 7)	45	70		V/ μs
	Full Power Bandwidth	3V Peak, (Note 8)		3.7		MHz
GBW	Gain Bandwidth	$f = 200\text{kHz}$	115	200		MHz
t_S	Settling Time	$A_V = -1$, 2V, 0.1% $A_V = -1$, 2V, 0.01%		91 112		ns ns
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, $V_{IN} = 0.2\text{V}_{P-P}$, $R_L = 150\Omega$		6		ns
	Overshoot	$A_V = 1$, $V_{IN} = 0.2\text{V}_{P-P}$, $R_L = 150\Omega$, $R_F = 0\Omega$		15		%
	Propagation Delay	50% V_{IN} to 50% $V_{OUT} = 0.2\text{V}_{P-P}$, $R_L = 150\Omega$		3		ns
R_O	Output Resistance	$A_V = 1$, $f = 1\text{MHz}$		0.15		Ω
	Channel Separation	$V_{OUT} = \pm 3\text{V}$, $R_L = 150\Omega$	82	90		dB
I_S	Supply Current	Per Amplifier		3.7	4.5	mA

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = 2.5\text{V}$, R_L to 2.5V, unless otherwise noted.

V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8		250 350	550 800	μV μV
I_{OS}	Input Offset Current			20	300	nA
I_B	Input Bias Current			20	300	nA
e_n	Input Noise Voltage	$f = 10\text{kHz}$		4		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current	$f = 10\text{kHz}$		1.1		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = 1.5\text{V}$ to 3.5V Differential	5	32 55		$\text{M}\Omega$ $\text{k}\Omega$
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range + Input Voltage Range –		3.5	4 1	1.5	V V

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$. $V_S = 5\text{V}$, $V_{CM} = 2.5\text{V}$, R_L to 2.5V , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.5\text{V to } 3.5\text{V}$	80	100		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = 1.5\text{V to } 3.5\text{V}$, $R_L = 500\Omega$	4	10		V/mV
V_{OUT}	Output Swing+ Output Swing–	$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$ $R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	3.6	3.8 0.9	1.4	V V
I_{OUT}	Output Current	$V_{OUT} = 3.5\text{V or } 1.5\text{V}$, 10mV Overdrive	10	20		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 2.5\text{V}$, $V_{IN} = \pm 1\text{V}$	22	55		mA
SR	Slew Rate	$A_V = -1$, (Note 7)	40	70		V/ μs
	Full Power Bandwidth	1V Peak, (Note 8)		8.7		MHz
GBW	Gain Bandwidth (Note 10)	$f = 200\text{kHz}$	115	180		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, $V_{IN} = 0.2\text{V}_{P-P}$, $R_L = 500\Omega$		5		ns
	Overshoot	$A_V = 1$, $V_{IN} = 0.2\text{V}_{P-P}$, $R_L = 500\Omega$		16		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT} , 0.1V, $R_L = 500\Omega$		3		ns
R_O	Output Resistance	$A_V = 1$, $f = 1\text{MHz}$		0.19		Ω
	Channel Separation	$V_{OUT} = 1.5\text{V to } 3.5\text{V}$, $R_L = 500\Omega$	82	90		dB
I_S	Supply Current	Per Amplifier		3.8	5	mA

The ● denotes the specifications which apply over the temperature range of $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	●		700 850	μV μV
	Input V_{OS} Drift	(Note 9)	●	3	7	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●		350	nA
I_B	Input Bias Current		●		350	nA
	Input Voltage Range + Input Voltage Range –		● ●	3.5	–3.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 3.5\text{V}$	●	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.3\text{V to } \pm 5.5\text{V}$	●	76		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 3\text{V}$, $R_L = 500\Omega$ $V_{OUT} = \pm 3\text{V}$, $R_L = 150\Omega$	● ●	9 6		V/mV V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$ $R_L = 150\Omega$, $V_{IN} = \pm 10\text{mV}$	● ●	± 3.15 ± 3.05		V V
I_{OUT}	Output Current	$V_{OUT} = \pm 3\text{V}$, 10mV Overdrive	●	22		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 1\text{V}$	●	30		mA
SR	Slew Rate	$A_V = -1$, (Note 7)	●	35		V/ μs
GBW	Gain Bandwidth	$f = 200\text{kHz}$	●	100		MHz
	Channel Separation	$V_{OUT} = \pm 3\text{V}$, $R_L = 150\Omega$	●	81		dB
I_S	Supply Current	Per Amplifier	●		5.45	mA

LT1722/LT1723/LT1724

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_S = 5\text{V}$, $V_{CM} = 2.5\text{V}$, R_L to 2.5Ω , unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	●		850 950	μV μV
	Input V_{OS} Drift	(Note 9)	●	3	7	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●		350	nA
I_B	Input Bias Current		●		350	nA
	Input Voltage Range + Input Voltage Range –		● ●	3.5	1.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.5\text{V}$ to 3.5V	●	75		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = 1.5\text{V}$ to 3.5V , $R_L = 500\Omega$	●	3		V/mV
V_{OUT}	Output Swing+ Output Swing–	$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$ $R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	● ●	3.55	1.45	V V
I_{OUT}	Output Current	$V_{OUT} = 3.5\text{V}$, or 1.5V , 10mV Overdrive	●	9		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 2.5\text{V}$, $V_{IN} = \pm 1\text{V}$	●	11		mA
SR	Slew Rate	$A_V = -1$, (Note 7)	●	30		V/ μs
GBW	Gain Bandwidth (Note 10)	$f = 200\text{kHz}$	●	100		MHz
	Channel Separation	$V_{OUT} = 1.5\text{V}$ to 3.5V , $R_L = 500\Omega$	●	81		dB
I_S	Supply Current		●		5.95	mA

The ● denotes the specifications which apply over the temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	●		900 1100	μV μV
	Input V_{OS} Drift	(Note 9)	●	3	10	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●		400	nA
I_B	Input Bias Current		●		400	nA
	Input Voltage Range + Input Voltage Range –		● ●	3.5	–3.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 3.5\text{V}$	●	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.0\text{V}$ to $\pm 5.5\text{V}$	●	75		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 3\text{V}$, $R_L = 500\Omega$ $V_{OUT} = \pm 3\text{V}$, $R_L = 150\Omega$	● ●	8 5		V/mV V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$ $R_L = 150\Omega$, $V_{IN} = \pm 10\text{mV}$	● ●	± 3.1 ± 3.0		V V
I_{OUT}	Output Current	$V_{OUT} = \pm 3\text{V}$, 10mV Overdrive	●	20		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 1\text{V}$	●	25		mA
SR	Slew Rate	$A_V = -1$, (Note 7)	●	25		V/ μs
GBW	Gain Bandwidth	$f = 200\text{kHz}$	●	90		MHz
	Channel Separation	$V_{OUT} = \pm 3\text{V}$, $R_L = 150\Omega$	●	80		dB
I_S	Supply Current		●		5.95	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. $V_S = 5\text{V}$, $V_{CM} = 2.5\text{V}$, R_L to 2.5V , unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	●			1000	μV
			●			1200	μV
	Input V_{OS} Drift	(Note 9)	●		3	10	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●			400	nA
I_B	Input Bias Current		●			400	nA
	Input Voltage Range + Input Voltage Range –		●	3.5		1.5	V
			●				V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.5\text{V}$ to 3.5V	●	75			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = 1.5\text{V}$ to 3.5V , $R_L = 500\Omega$	●	2			V/mV
V_{OUT}	Output Swing+	$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	●	3.5			V
	Output Swing–	$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	●			1.5	V
I_{OUT}	Output Current	$V_{OUT} = 3.5\text{V}$ or 1.5V , 30mV Overdrive	●	8			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 2.5\text{V}$, $V_{IN} = \pm 1\text{V}$	●	10			mA
SR	Slew Rate	$A_V = -1$, (Note 7)	●	20			V/ μs
GBW	Gain Bandwidth (Note 10)	$f = 200\text{kHz}$	●	90			MHz
	Channel Separation	$V_{OUT} = 1.5\text{V}$ to 3.5V , $R_L = 500\Omega$	●	80			dB
I_S	Supply Current		●			6.45	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1722C/LT1722I, LT1723C/LT1723I, LT1724C/LT1724I are guaranteed functional over the operating temperature range of -40°C to 85°C .

Note 5: The LT1722C/LT1723C/LT1724C are guaranteed to meet specified performance from 0°C to 70°C . The LT1722C/LT1723C/LT1724C are

designed, characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1722I/LT1723I/LT1724I are guaranteed to meet specified performance from -40°C to 85°C .

Note 6: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 7: Slew rate is measured between $\pm 2\text{V}$ on the output with $\pm 3\text{V}$ input for $\pm 5\text{V}$ supplies and $\pm 1\text{V}$ on the output with $\pm 1.5\text{V}$ input for single 5V supply. (For 5V supply, the voltage levels are 2.5V referred.)

Note 8: Full power bandwidth is calculated from the slew rate:

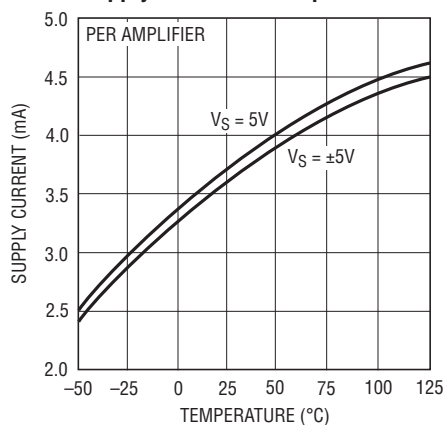
$$\text{FPBW} = \text{SR} / 2\pi V_P$$

Note 9: This parameter is not 100% tested.

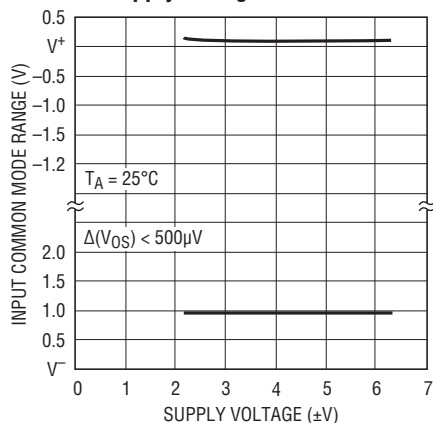
Note 10: This parameter is guaranteed through correlation with slew rate.

TYPICAL PERFORMANCE CHARACTERISTICS

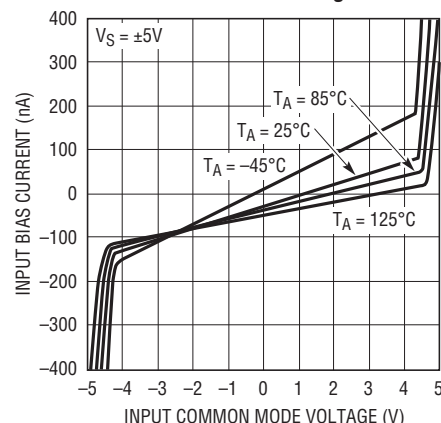
Supply Current vs Temperature



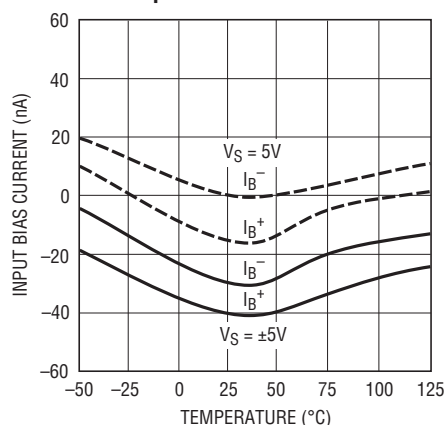
Input Common Mode Range vs Supply Voltage



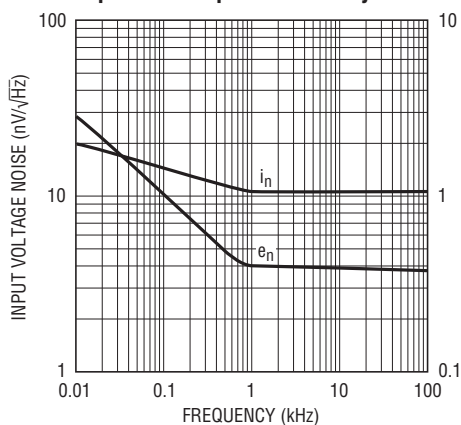
Input Bias Current vs Common Mode Voltage



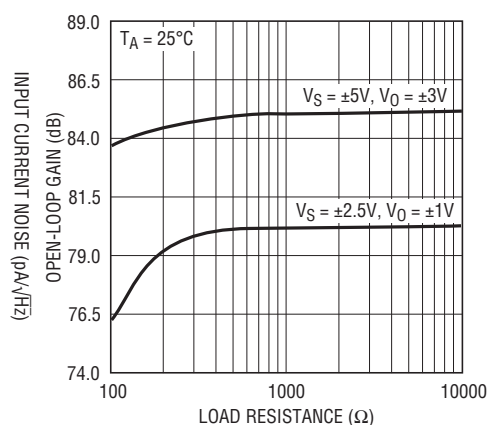
Input Bias Current vs Temperature



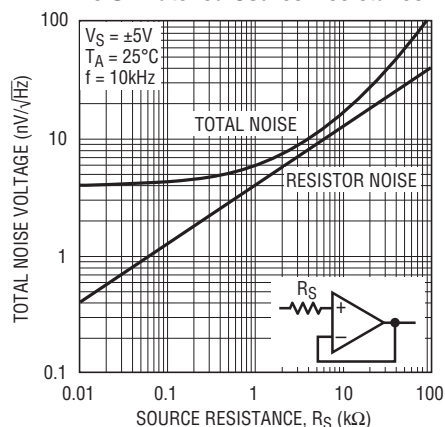
Input Noise Spectral Density



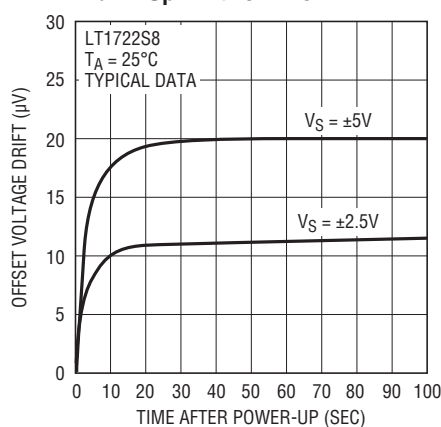
Open-Loop Gain vs Resistive Load



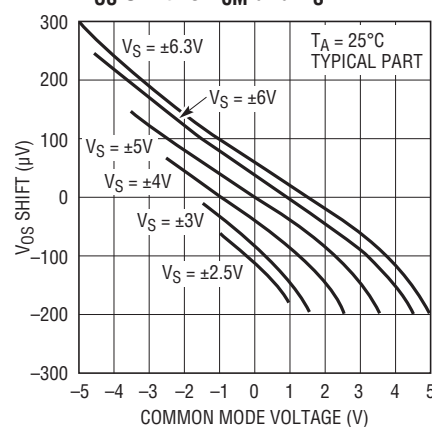
Total Noise vs Unmatched Source Resistance



Warm-Up Drift vs Time

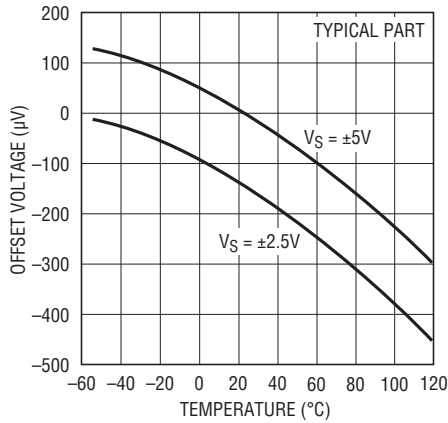


VOS Shift vs VCM and VS

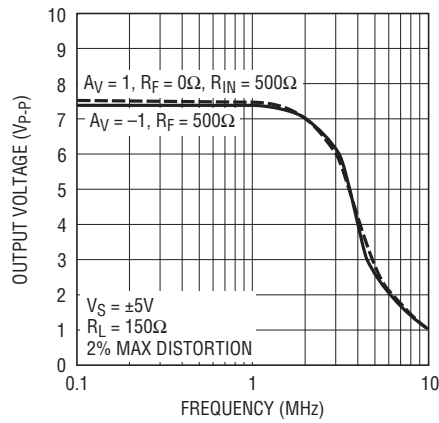


TYPICAL PERFORMANCE CHARACTERISTICS

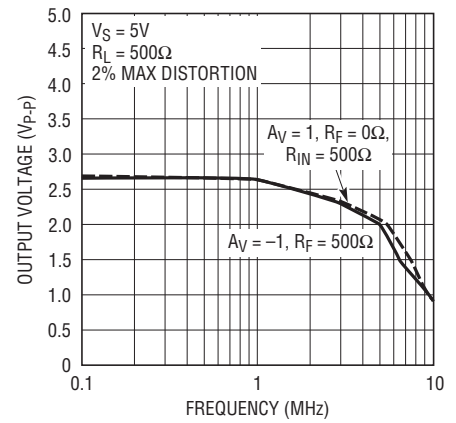
V_{OS} vs Temperature



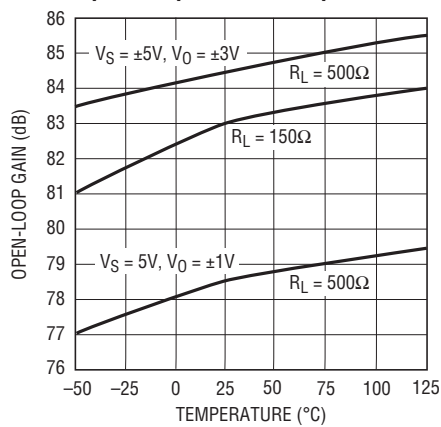
Undistorted Output Swing vs Frequency



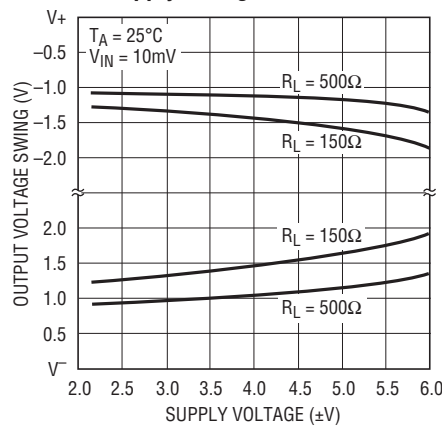
Undistorted Output Swing vs Frequency



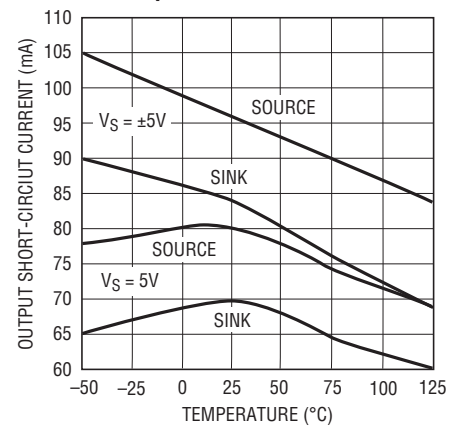
Open-Loop Gain vs Temperature



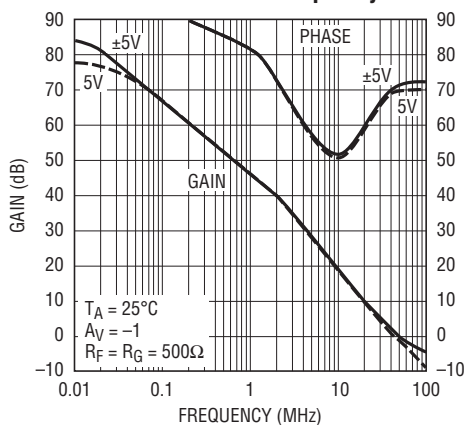
Output Voltage Swing vs Supply Voltage



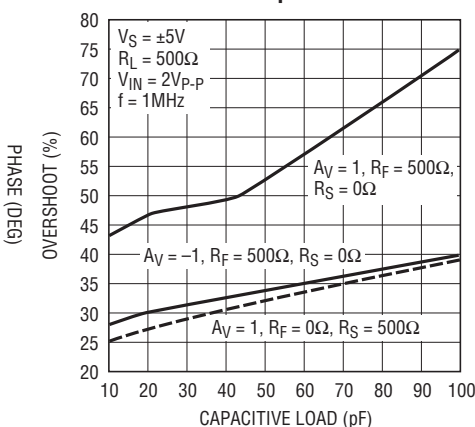
Output Short-Circuit Current vs Temperature



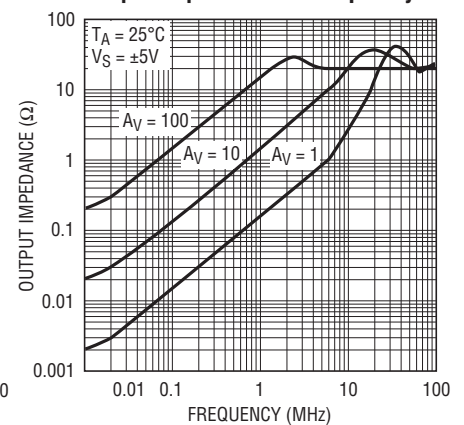
Gain and Phase vs Frequency



Overshoot vs Capacitive Load

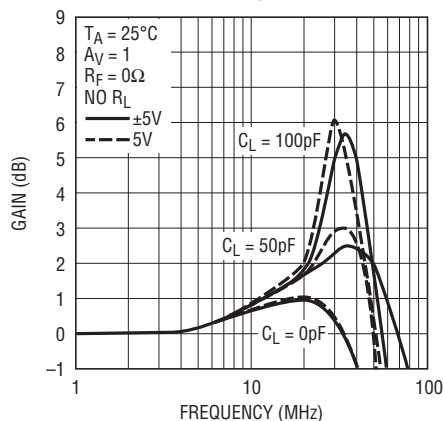


Output Impedance vs Frequency



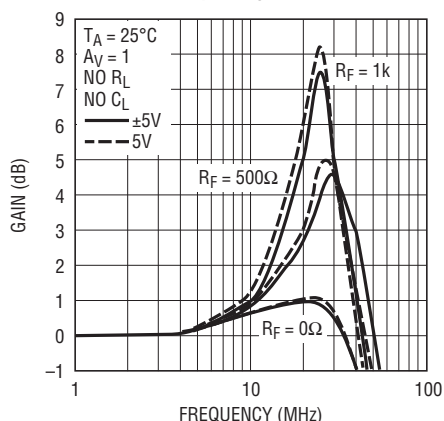
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency, $A_V = 1$



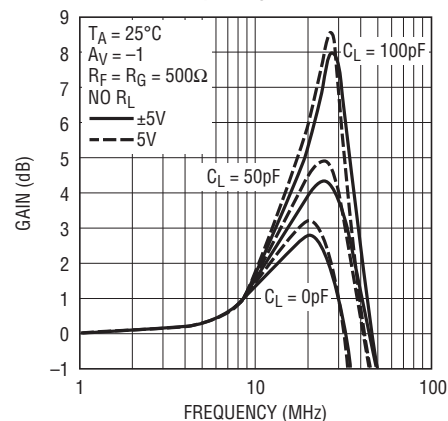
1723 G19

Gain vs Frequency, $A_V = 1$



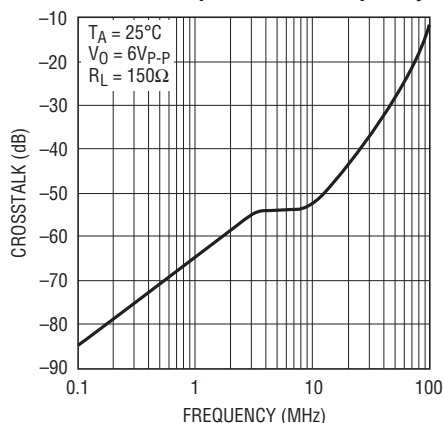
1723 G20

Gain vs Frequency, $A_V = -1$



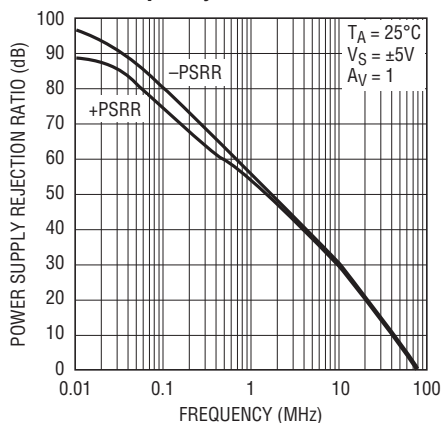
1723 G21

Channel Separation vs Frequency



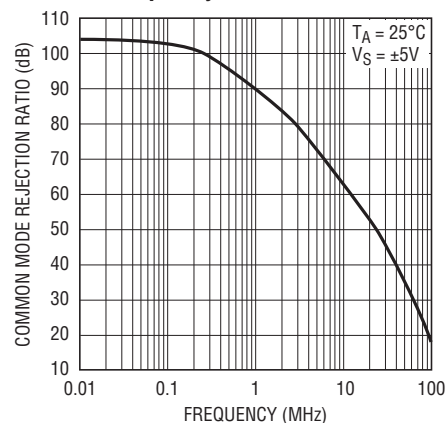
1723 G22

Power Supply Rejection Ratio vs Frequency



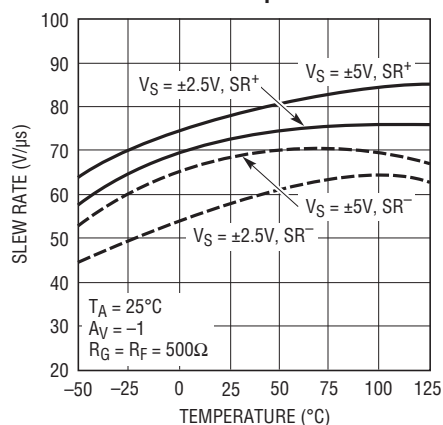
1723 G23

Common Mode Rejection Ratio vs Frequency



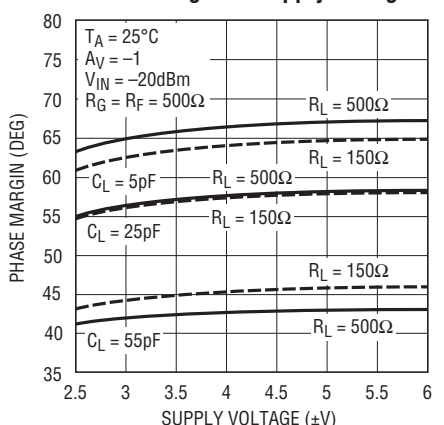
1723 G24

Slew Rate vs Temperature



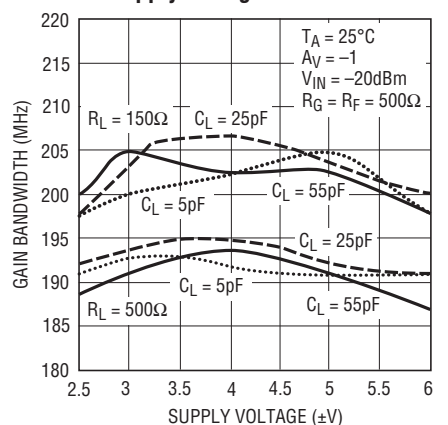
1723 G40

Phase Margin vs Supply Voltage



1723 G41

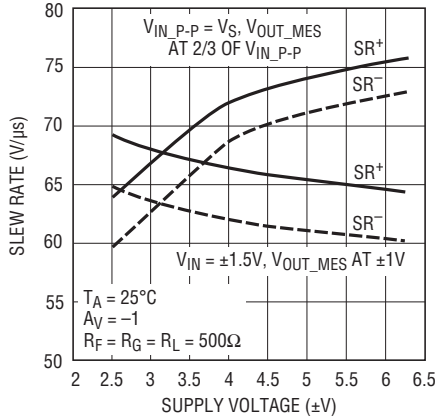
Gain Bandwidth vs Supply Voltage



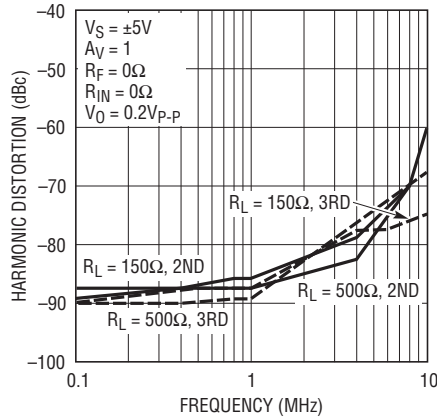
1723 G42

TYPICAL PERFORMANCE CHARACTERISTICS

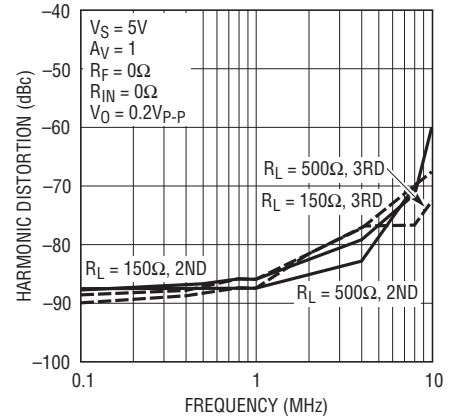
Slew Rate vs Supply Voltage



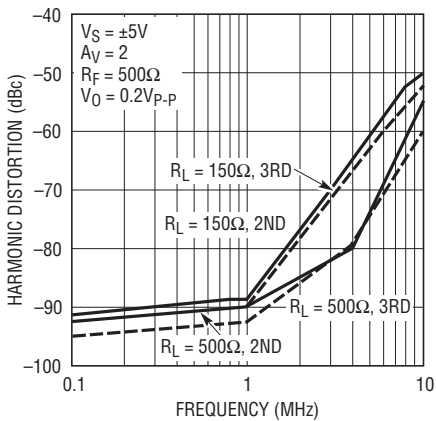
Harmonic Distortion vs Frequency
 $A_V = 1, V_0 = 0.2V_{P-P}$



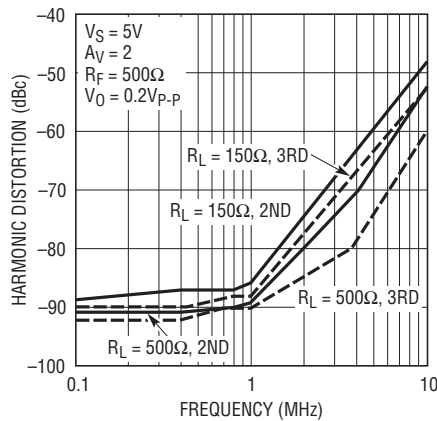
Harmonic Distortion vs Frequency
 $A_V = 1, V_0 = 0.2V_{P-P}$



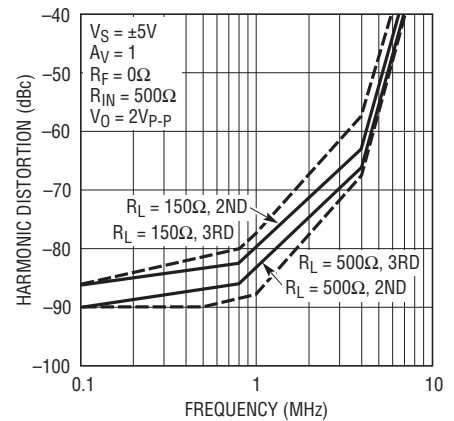
Harmonic Distortion vs Frequency
 $A_V = 2, V_0 = 0.2V_{P-P}$



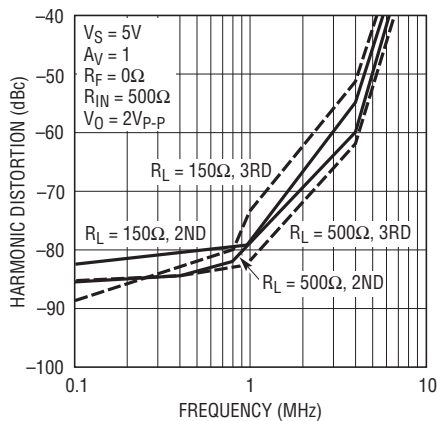
Harmonic Distortion vs Frequency
 $A_V = 2, V_0 = 0.2V_{P-P}$



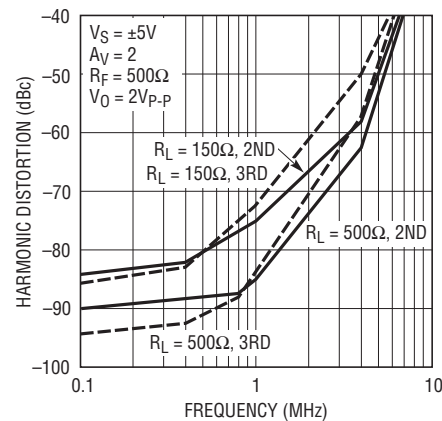
Harmonic Distortion vs Frequency
 $A_V = 1, V_0 = 2V_{P-P}$



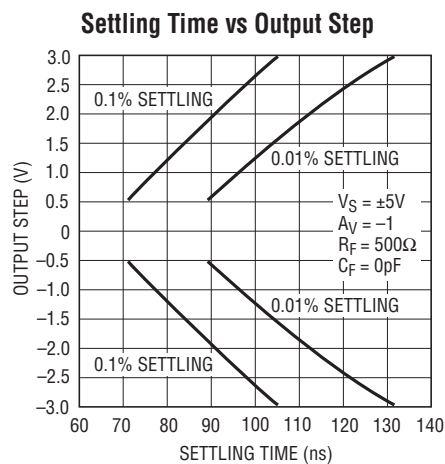
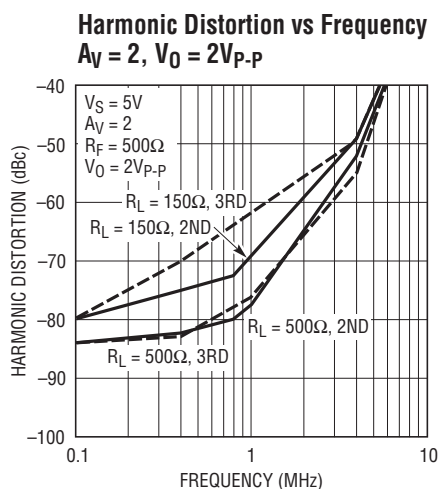
Harmonic Distortion vs Frequency
 $A_V = 1, V_0 = 2V_{P-P}$



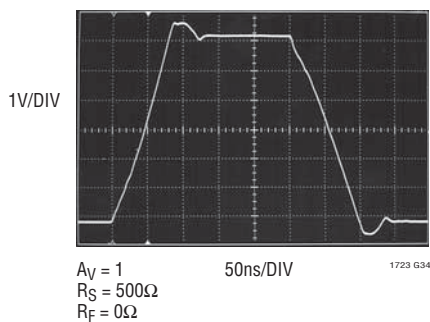
Harmonic Distortion vs Frequency
 $A_V = 2, V_0 = 2V_{P-P}$



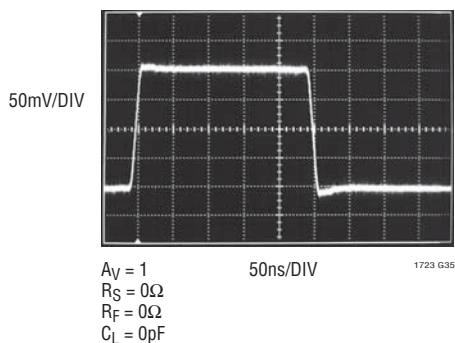
TYPICAL PERFORMANCE CHARACTERISTICS



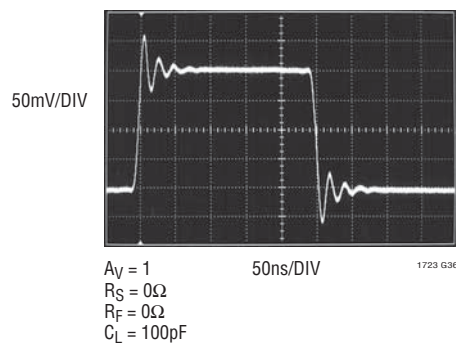
Large-Signal Transient, $A_V = 1$



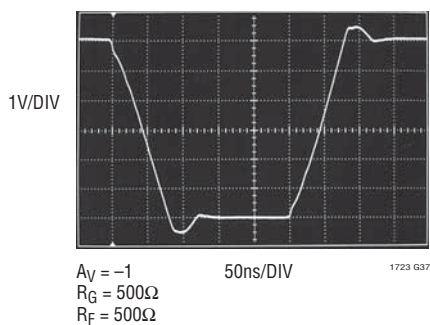
Small-Signal Transient, $A_V = 1$



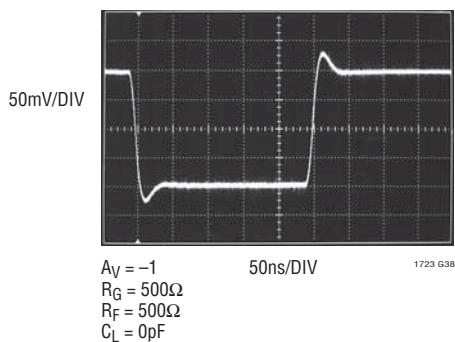
Small-Signal Transient, $A_V = 1$



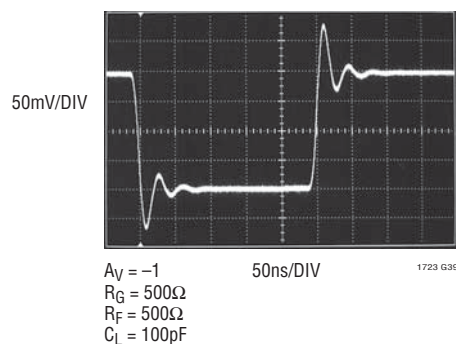
Large-Signal Transient, $A_V = -1$



Small-Signal Transient, $A_V = -1$



Small-Signal Transient, $A_V = -1$



APPLICATIONS INFORMATION

The LT1722/LT1723/LT1724 may be inserted directly into many operational amplifier applications improving both DC and AC performance, as well as noise and distortion.

Layout and Passive Components

The LT1722/LT1723/LT1724 amplifiers are more tolerant of less than ideal layouts than other high speed amplifiers. For maximum performance (for example, fast settling time) use a ground plane, short lead lengths and RF quality bypass capacitors (0.01μF to 0.1μF). For high drive current applications, use low ESR supply bypass capacitors (1μF to 10μF tantalum). The output/input parasitic coupling should be minimized when high frequency performance is required.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. In parallel with the feedback resistor, a capacitor of value:

$$C_F > R_G \cdot C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a feedback resistor is used, such as an I-to-V converter, C_F should be five times greater than C_{IN} ; an optimum value for C_F is 10pF.

Input Considerations

Each of the LT1722/LT1723/LT1724 inputs is protected with back-to-back diodes across the bases of the NPN input devices. If greater than 0.7V differential input voltages are anticipated, the input current must be limited to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven beyond the supply, limit the current with an external resistor to less than 10mA. The input stage protection circuit is shown in Figure 1.

The input currents of the LT1722/LT1723/LT1724 are typically in the tens of nA range due to the bias current cancellation technique used at the input. As the input offset current can be greater than either input current,

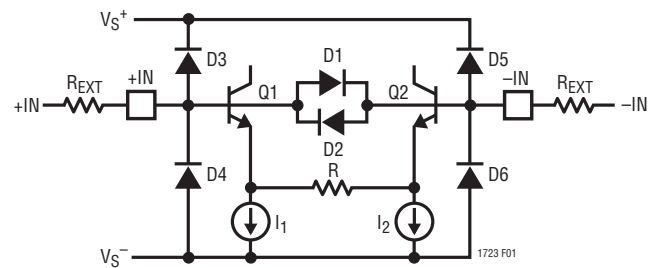


Figure 1. Input Stage Protection

adding resistance to balance source resistance is not recommended. The value of the source resistor should be below 12k as it actually degrades DC accuracy and also increases noise.

Total Input Noise

The total input noise of the LT1722/LT1723/LT1724 is optimized for a source resistance between 0.8k and 12k. Within this range, the total input noise is dominated by the noise of the source resistance itself. When the source resistance is below 0.8k, voltage noise of the amplifier dominates. When the source resistance is above 12k, the input noise current is the dominant contributor.

Capacitive Loading

The LT1722/LT1723/LT1724 drive capacitive loads up to 100pF with unity gain. As the capacitive load increases, both the bandwidth and the phase margin decrease causing peaking in the frequency response and overshoot in the transient response. When there is a need to drive a larger capacitive load, a 25Ω series resistance assures stability with any value of load capacitor. A feedback capacitor also helps to reduce any peaking.

Power Dissipation

The LT1722/LT1723/LT1724 combine high speed and large output drive in a small package. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A), power dissipation per amplifier (P_D) and number of amplifiers (n) as follows:

$$T_J = T_A + (n \cdot P_D \cdot \theta_{JA})$$

APPLICATIONS INFORMATION

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current.

Worst-case instantaneous power dissipation for a given resistive load in one amplifier occurs at the maximum supply current and when the output voltage is at half of either supply voltage (or the maximum swing if less than half supply voltage).

Therefore $P_{D(MAX)}$ in one amplifier is:

$$P_{D(MAX)} = (V^+ - V^-)(I_{S(MAX)}) + (V^+/2)^2/R_L$$

or

$$P_{D(MAX)} = (V^+ - V^-)(I_{S(MAX)}) + (V^+ - V_{O(MAX)})(V_{O(MAX)}/R_L)$$

Example. Worst-case conditions are: both op amps in the LT1723IS8 are at $T_A = 85^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 150\Omega$, $V_{OUT} = 2.5\text{V}$.

$$P_{D(MAX)} = 2 \cdot [(10\text{V})(5.95\text{mA}) + (2.5\text{V})^2/150\Omega] = 203\text{mW}$$

$$T_{J(MAX)} = 85^\circ\text{C} + (203\text{mW})(190^\circ\text{C/W}) = 124^\circ\text{C}$$

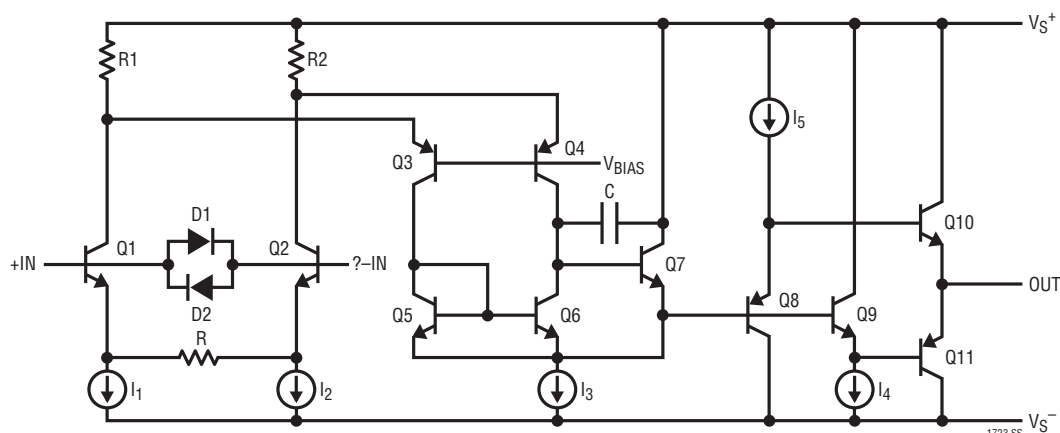
which is less than the absolute maximum rating at 150°C .

Circuit Operation

The LT1722/LT1723/LT1724 circuit topology is a voltage feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. The first stage is a folded cascode formed by the transistors Q1 through Q4. A degeneration resistor, R, is used in the input stage. The current mirror Q5, Q6 is bootstrapped by Q7. The capacitor, C, assures the bandwidth and the slew rate performance. The output stage is formed by complementary emitter followers, Q8 through Q11. The diodes D1 and D2 protect against input reversed biasing. The remaining part of the circuit assures optimum voltage and current biases for all stages.

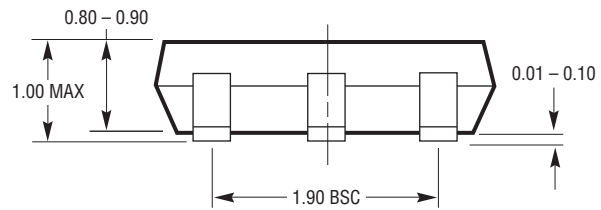
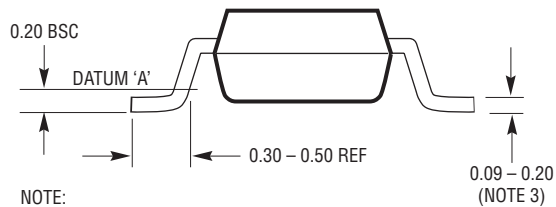
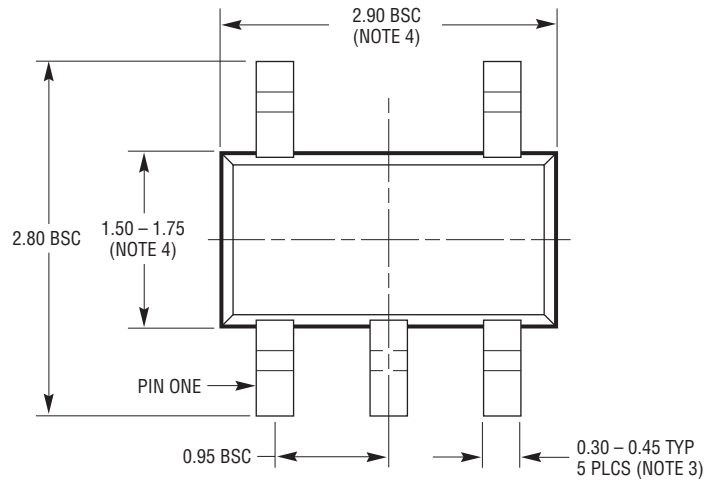
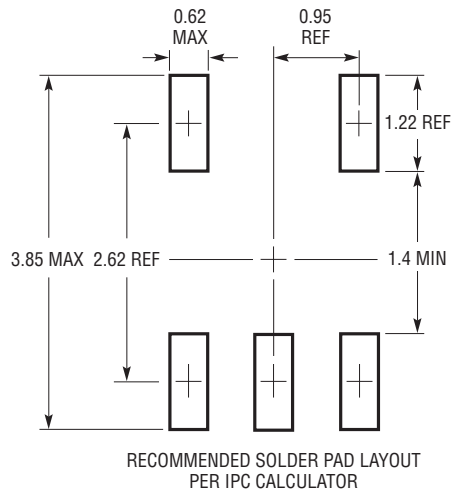
Low noise, reduced current supply, high speed and DC accurate parameters are distinctive features of the LT1722/LT1723/LT1724.

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

S5 Package
5-Lead Plastic TSOT-23
 (Reference LTC DWG # 05-08-1635)

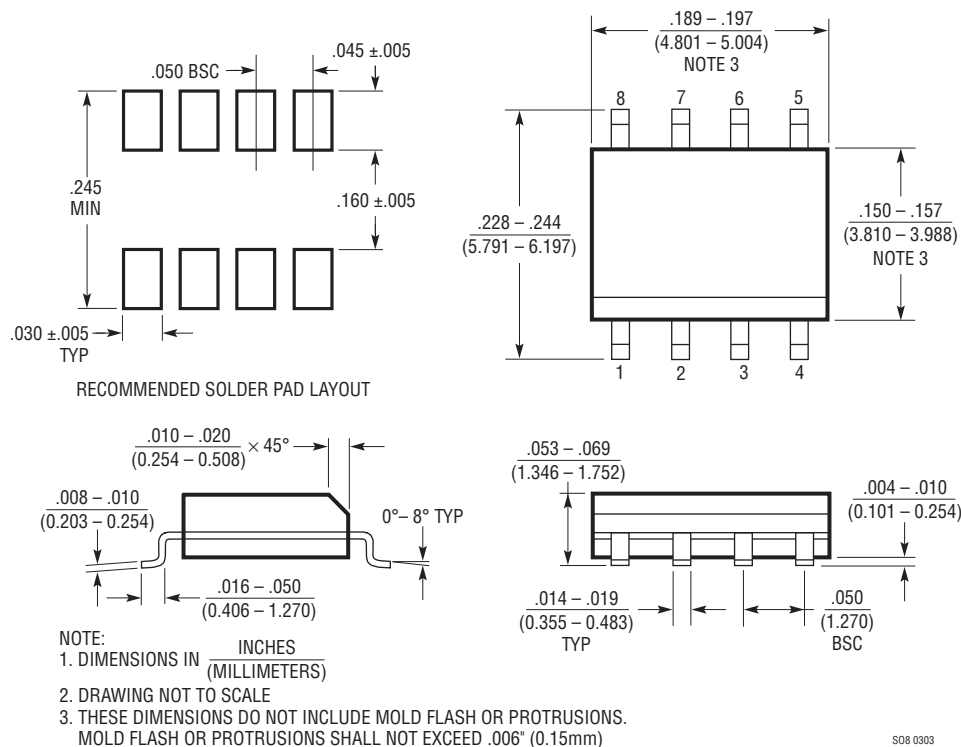


- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DRAWING NOT TO SCALE
 3. DIMENSIONS ARE INCLUSIVE OF PLATING
 4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 5. MOLD FLASH SHALL NOT EXCEED 0.254mm
 6. JEDEC PACKAGE REFERENCE IS MO-193

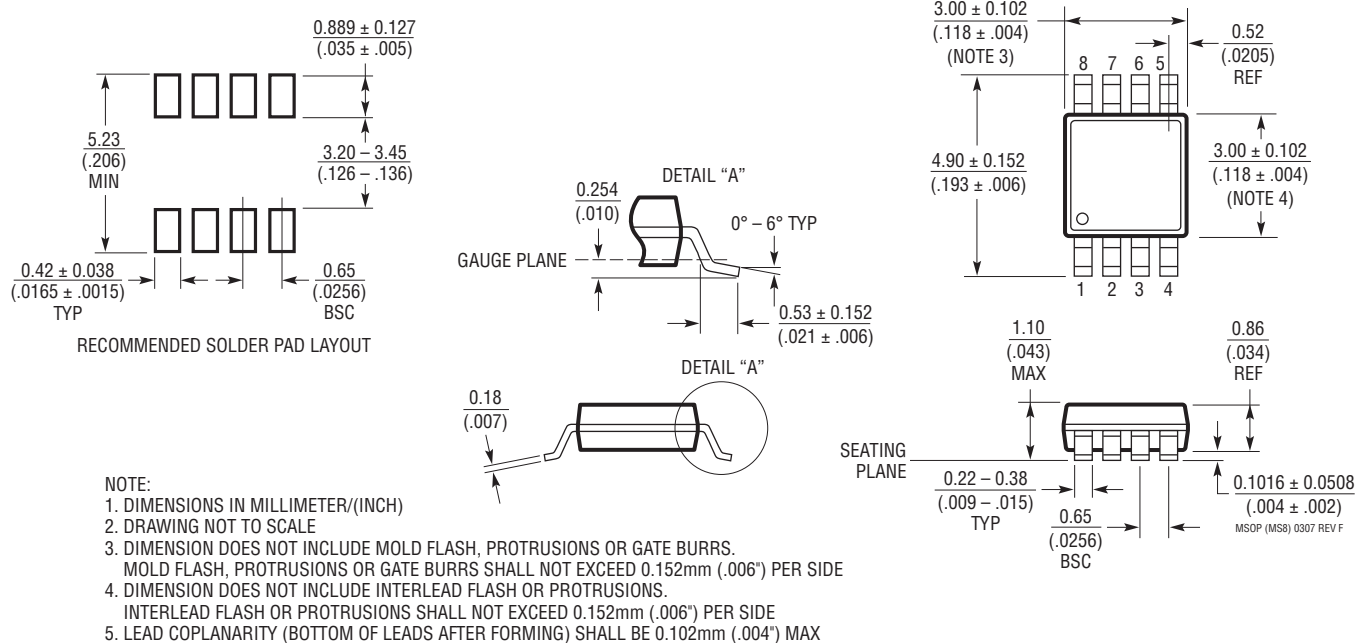
S5 TSOT-23 0302 REV B

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660 Rev F)



PACKAGE DESCRIPTION

S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

