Content

List of figures

List of tables

1   Block diagram and pin description

1.1   Block diagram

Figure 1.   Block diagram
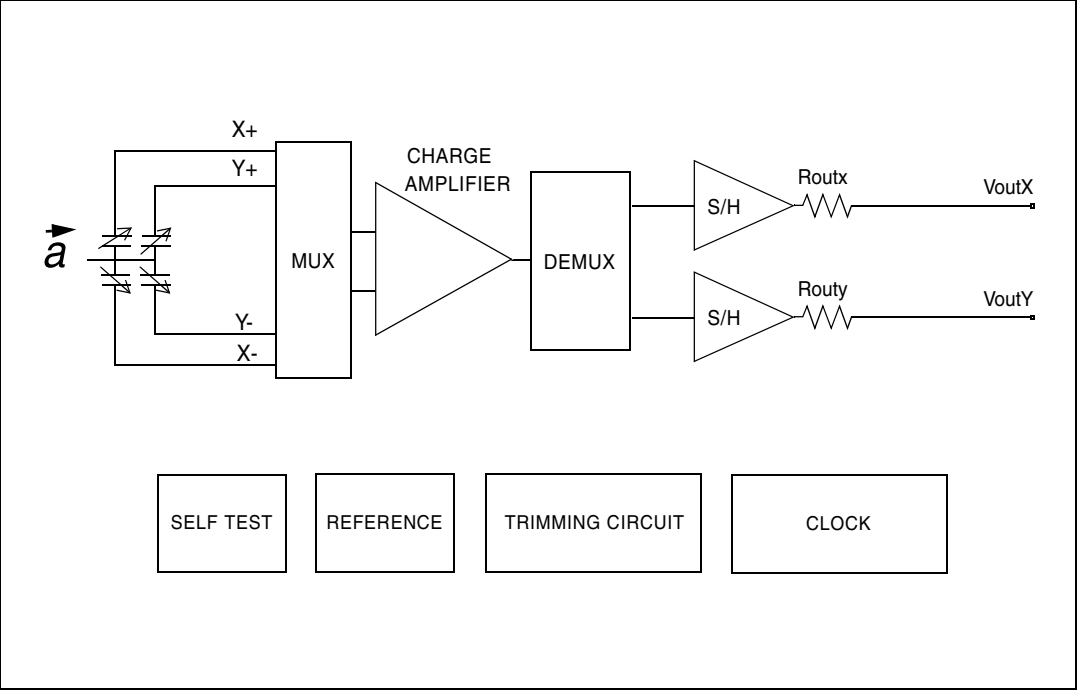
1.2   Pin description

Figure 2.   Pin connection
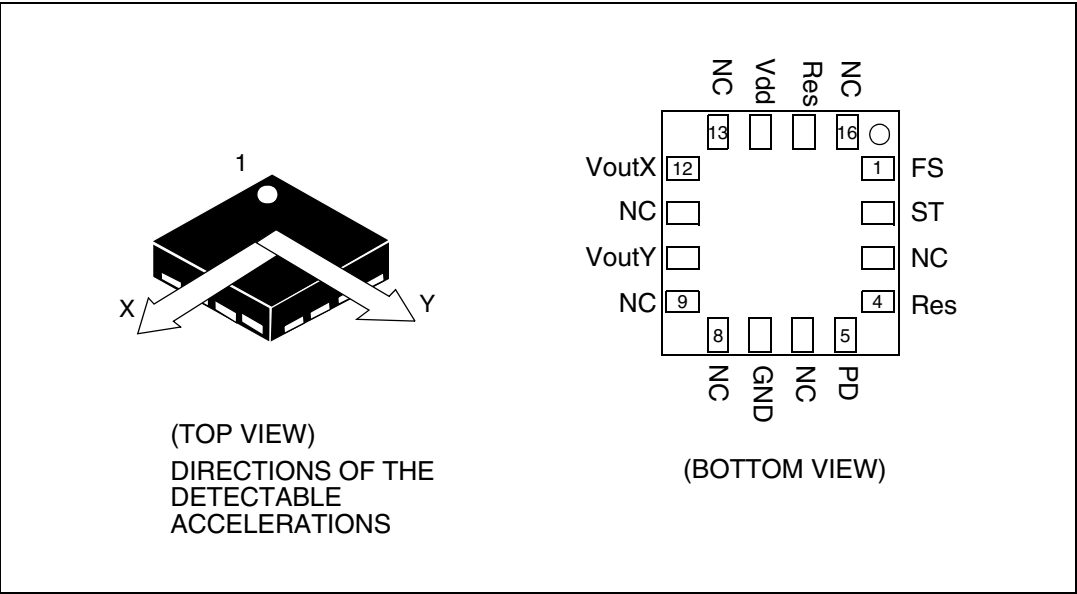
Table 2.   Pin description

Pin #	Pin name	Function
1	FS	Full scale selection (Logic 0: ±2g Full-scale; Logic 1: ±6g Full-scale)
2	ST	Self test (Logic 0: normal mode; Logic 1: Self-test mode)
3	NC	Internally not connected
4	Res	Leave Unconnected or Connect to Vdd
5	PD	Power Down (Logic 0: normal mode; Logic 1: Power-Down mode)
6	NC	Internally not connected
7	GND	0V supply
8	NC	Internally not connected
9	NC	Internally not connected
10	VoutY	Output voltage Y channel
11	NC	Internally not connected
12	VoutX	Output voltage X channel
13	NC	Internally not connected
14	Vdd	Power supply
15	Res	Connect to Vdd
16	NC	Internally not connected

2   Mechanical and electrical specifications

2.1   Mechanical characteristics

Table 3.   Mechanical characteristics @ Vdd =3.3 V, T = 25 °C unless otherwise noted[1]

Symbol	Parameter	Test condition	Min.	Typ.[2]	Max.	Unit
Ar	Acceleration range[3]	FS pin connected to GND		± 2		g
		FS pin connected to Vdd		± 6		
So	Sensitivity[4]	Full-scale = ±2 g	Vdd/5 - 5%	Vdd/5	Vdd/5 + 5%	V/g
		Full-scale = ±6 g	Vdd/15 - 10%	Vdd/15	Vdd/15 + 10%	
SoDr	Sensitivity change vs temperature	Delta from +25 °C		± 0.01		%/°C
Voff	Zero-g level[4]	Full-scale = ±2 g T = 25 °C	Vdd/2 - 4%	Vdd/2	Vdd/2 + 4%	V
OffDr	Zero-g level change vs temperature	Delta from +25 °C		±0.4		mg/°C
NL	Non linearity[5]	Best fit straight line Full-scale = ±2 g		±0.5		% FS
CrossAx	Cross-axis[6]			±2		%
An	Acceleration noise density	Vdd = 3.3 V; Full-scale = ±2 g		50		$\mu g/\sqrt{Hz}$
Vt	Self test output voltage change[7],[8],[9]	X axis T = 25 °C; Vdd=3.3 V		140		mV
		Y axis T = 25 °C; Vdd=3.3 V		-140		mV
Fres	Sensing element resonant frequency[10]	X,Y axis	2.0			KHz
Top	Operating temperature range		-40		+85	°C
Wh	Product weight			0.040		gram

1. The product is factory calibrated at 3.3 V. The operational power supply range is from 2.4 V to 3.6 V. Voff, So and Vt parameters will vary with supply voltage.
2. Typical specifications are not guaranteed.
3. Guaranteed by wafer level test and measurement of initial offset and sensitivity.
4. Zero-g level and Sensitivity are essentially ratiometric to supply voltage at the calibration level ±8%.
5. Guaranteed by design.
6. Contribution to the measuring output of an inclination/acceleration along any perpendicular axis.
7. "Self test output voltage change" is defined as $Vout_{(Vst=Logic1)}$-$Vout_{(Vst=Logic0)}$.
8. "Self test output voltage change" varies cubically with supply voltage.
9. When Full-scale is set to ±6 g, "Self test output voltage change" is one third of the specified value at ±2 g.
10. Minimum resonance frequency Fres=2.0 KHz. Sensor bandwidth=1/(2*π*110kΩ*Cload), with Cload>1 nF.

2.2 Electrical characteristics

Table 4. Electrical characteristics @ Vdd =3.3 V, T = 25 °C unless otherwise noted[1]

Symbol	Parameter	Test condition	Min.	Typ.[2]	Max.	Unit
Vdd	Supply voltage		2.4	3.3	3.6	V
Idd	Supply current	Normal mode		680		μA
		Power-down mode		1	5	
Vfs Vst Vpd	Full-scale input Self-test input Power-down input	Logic 0 level	0		0.3*Vdd	V
		Logic 1 level	0.7*Vdd		Vdd	V
Rout	Output impedance of VoutX, VoutY		90	110	130	KΩ
Cload	Capacitive load drive[3] for VoutX, VoutY		1			nF
Ton	Turn-on time at exit of Power-down mode	Cload expressed in μF		550*Cload+ 0.3		ms
Top	Operating temperature range		-40		+85	ºC

1. The product is factory calibrated at 3.3 V.

2. Typical specifications are not guaranteed.

3. Minimum resonance frequency Fres=2.0 KHz. Device bandwidth=1/(2*π*110 kΩ*Cload), with Cload>1 nF.

2.3   Absolute maximum ratings

Stresses above those listed as "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5.   Absolute maximum rating

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin (FS, ST, PD)	-0.3 to Vdd +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3.3 V)	3000 g for 0.5 ms	
		10000 g for 0.1 ms	
A_{UNP}	Acceleration (any axis, not powered)	3000 g for 0.5 ms	
		10000 g for 0.1 ms	
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4 (HBM)	KV
		1.5 (CDM)	KV
		400 (MM)	V

This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part

This is an ESD sensitive device, improper handling can cause permanent damages to the part

2.4 Terminology

Sensitivity describes the gain of the sensor and can be determined by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, note the output value, rotate the sensor by 180 degrees (point to the sky) and note the output value again thus applying ±1g acceleration to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, will give the actual sensitivity of the sensor. This value changes very little over temperature (see sensitivity change vs. temperature) and also very little over time. The Sensitivity tolerance describes the range of Sensitivities of a large population of sensors.

Zero-g level describes the actual output signal if there is no acceleration present. A sensor in a steady state on a horizontal surface will measure 0g in X axis and 0g in Y axis. The output is ideally for a 3.3V powered sensor Vdd/2 = 1650 mV. A deviation from ideal 0-g level (1650 mV in this case) is called Zero-g offset. Offset of precise MEMS sensors is to some extend a result of stress to the sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature - see "Zero-g level change vs. temperature" - the Zero-g level of an individual sensor is very stable over lifetime. The Zero-g level tolerance describes the range of Zero-g levels of a population of sensors.

Self test allows to test the mechanical and electric part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. The Self Test function is off when the ST pin is connected to GND. When the ST pin is tied at Vdd an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a voltage change in their DC levels which is related to the selected full-scale and depending on the Supply Voltage through the device sensitivity. When ST is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specification.

Output impedance describes the resistor inside the output stage of each channel. This resistor is part of a filter consisting of an external capacitor of at least 1 nF and the internal resistor. Due to the high resistor level, only small inexpensive external capacitors are needed to generate low corner frequencies. When interfacing with an ADC it is important to use high input impedance input circuitries to avoid measurement errors. Note that the minimum load capacitance forms a corner frequency close to the resonance frequency of the sensor. In general the smallest possible bandwidth for a particular application should be chosen to get the best results.

3 Functionality

The LIS244ALH is an ultra compact low-power, analog output two-axis linear accelerometer packaged in a LGA package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and provide an analog signal to the external world.

3.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is in the fF range.

3.2 IC interface

The complete signal processing uses a fully differential structure, while the final stage converts the differential signal into a single-ended one to be compatible with the external world.

The first stage is a low-noise capacitive amplifier that implements a Correlated Double Sampling (CDS) at its output to cancel the offset and the 1/f noise. The produced signal is then sent to two different S&Hs, one for each channel, and made available to the outside.

All the analog parameters (output offset voltage and sensitivity) are ratiometric to the voltage supply. Increasing or decreasing the voltage supply, the sensitivity and the offset will increase or decrease linearly. This feature provides the cancellation of the error related to the voltage supply along an analog to digital conversion chain.

3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-g level (Voff).
The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation. This allows the user to employ the device without further calibration.

4 Application hints

Figure 3. LIS244ALH electrical connection
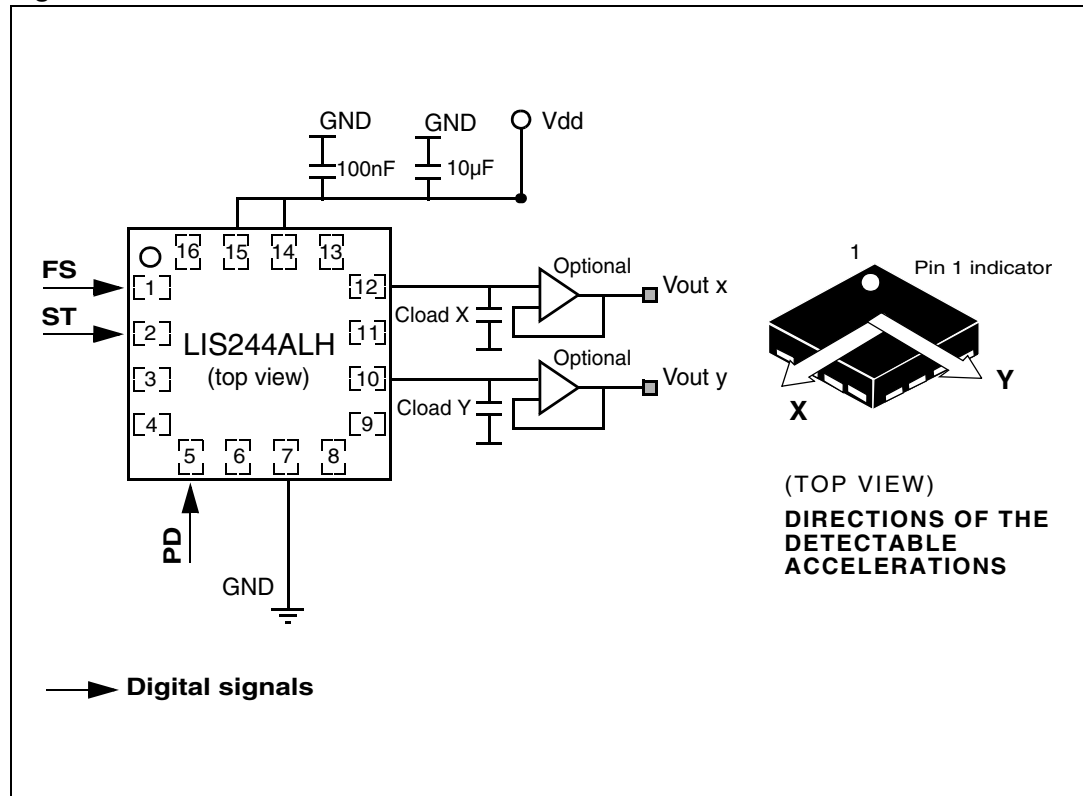
Power supply decoupling capacitors (100 nF ceramic or polyester + 10 µF Aluminum) should be placed as near as possible to the device (common design practice).

The LIS244ALH allows to band limit VoutX and VoutY through the use of external capacitors. The recommended frequency range spans from DC up to 2.0 KHz. In particular, capacitors are added at output VoutX and VoutY pins to implement low-pass filtering for antialiasing and noise reduction. The equation for the cut-off frequency (f_t) of the external filters is in this case:

$$f_t = \frac{1}{2\pi \cdot R_{out} \cdot C_{load}(x, y)}$$

Taking into account that the internal filtering resistor (R_{out}) has a nominal value equal to 110 KΩ, the equation for the external filter cut-off frequency may be simplified as follows:

$$f_t = \frac{1.45\mu F}{C_{load}(x, y)} [Hz]$$

The tolerance of the internal resistor can vary typically of ±20% within its nominal value of 110 KΩ, thus the cut-off frequency will vary accordingly. A minimum capacitance of 1 nF for $C_{load}(x, y)$ is required.

Table 6.   **Filter capacitor selection, C_{load} (x,y)**

Cut-off frequency	Capacitor value
1 Hz	1500 nF
10 Hz	150 nF
20 Hz	68 nF
50 Hz	30 nF
100 Hz	15 nF
200 Hz	6.8 nF
500 Hz	3 nF

4.1   Soldering information

The LGA package is compliant with the ECOPACK, RoHs and "Green" standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

Leave "Pin 1 Indicator" unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

4.2   Output response vs. orientation

Figure 4.   **Output response vs. orientation**

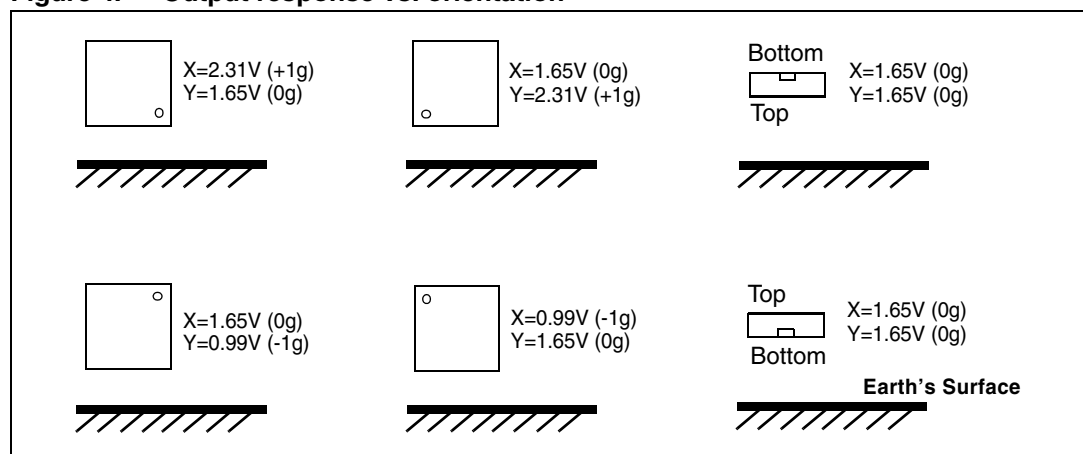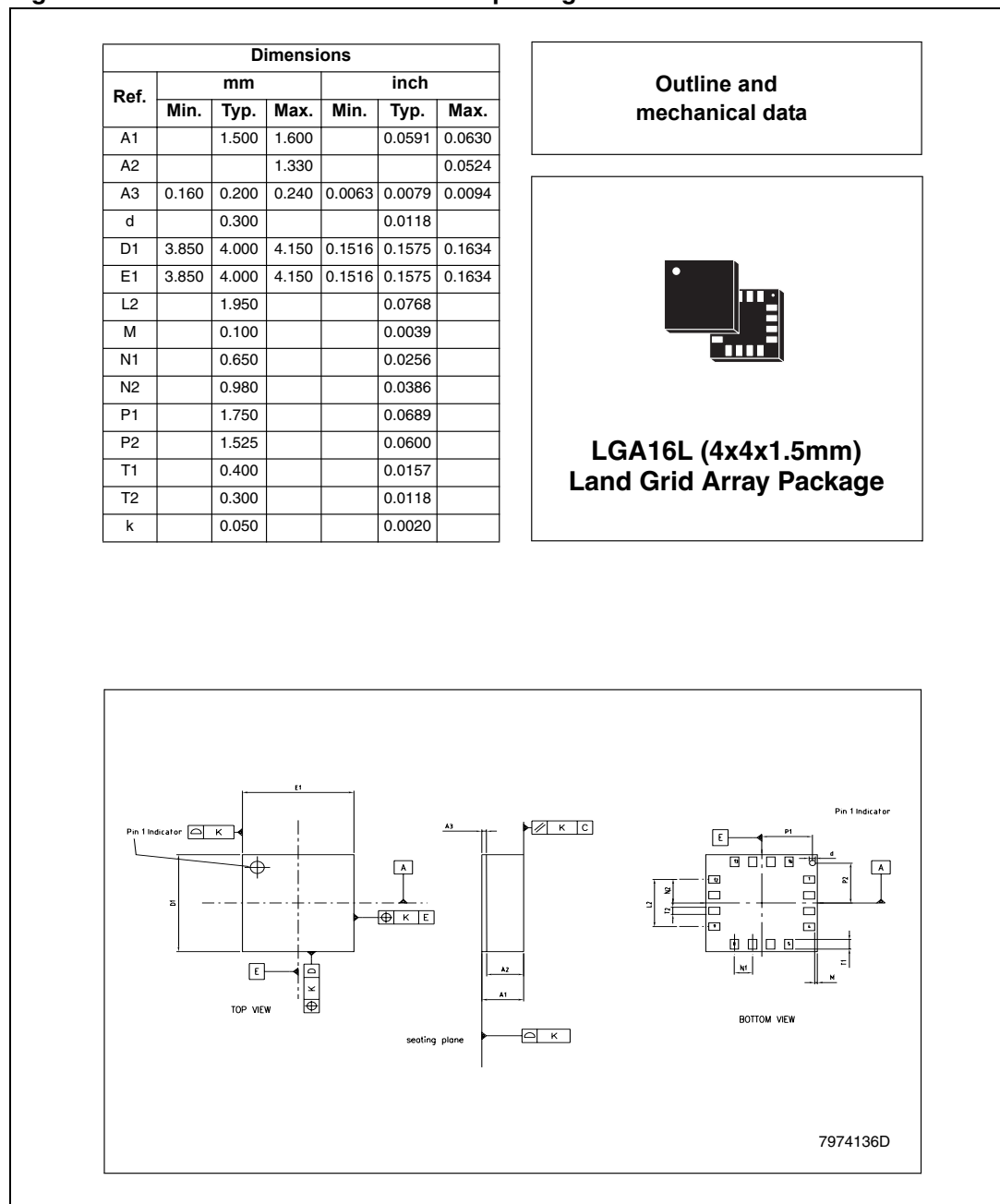*Figure 4* shows output voltage values of LIS244ALH, powered at 3.3 V, with full-scale ±2 g.

5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK® is an ST trademark.

ECOPACK® specifications are available at: www.st.com.

Figure 5.   LGA16: mechanical data and package dimensions

Dimensions						
Ref.	**mm**			**inch**		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A1		1.500	1.600		0.0591	0.0630
A2			1.330			0.0524
A3	0.160	0.200	0.240	0.0063	0.0079	0.0094
d		0.300			0.0118	
D1	3.850	4.000	4.150	0.1516	0.1575	0.1634
E1	3.850	4.000	4.150	0.1516	0.1575	0.1634
L2		1.950			0.0768	
M		0.100			0.0039	
N1		0.650			0.0256	
N2		0.980			0.0386	
P1		1.750			0.0689	
P2		1.525			0.0600	
T1		0.400			0.0157	
T2		0.300			0.0118	
k		0.050			0.0020	

Outline and mechanical data

LGA16L (4x4x1.5mm) Land Grid Array Package

7974136D

6   Revision history

Table 7.   Document revision history

Date	Revision	Changes
15-Jan-2008	1	Initial release.
19-Feb-2008	2	Updated *Figure 2: Pin connection on page 5*

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