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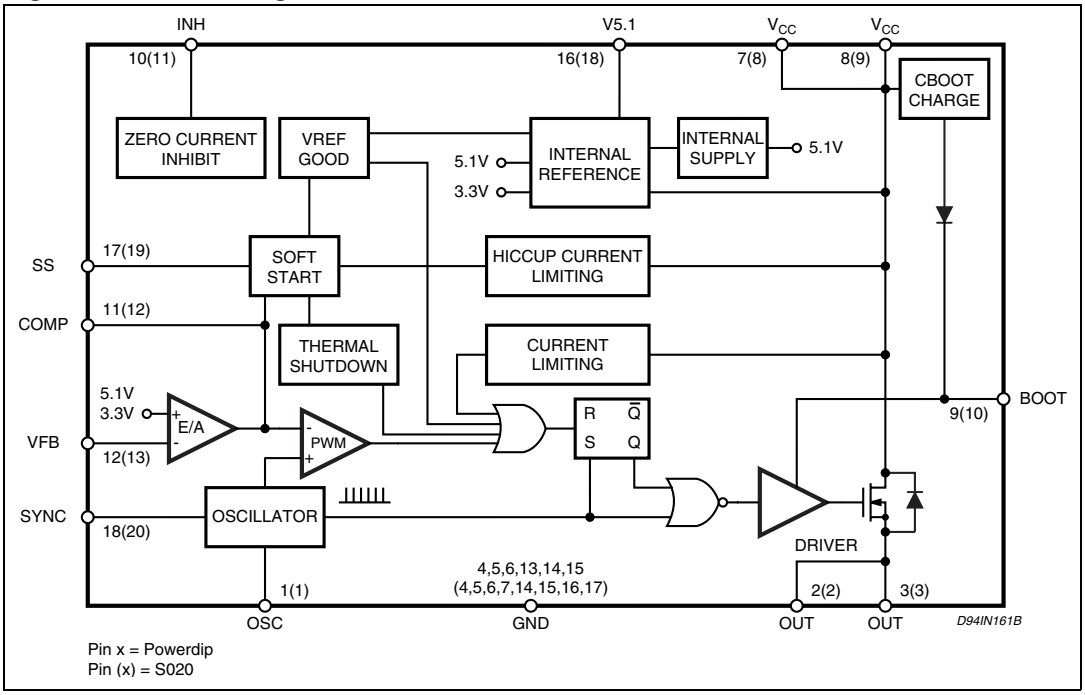
1 Block diagram

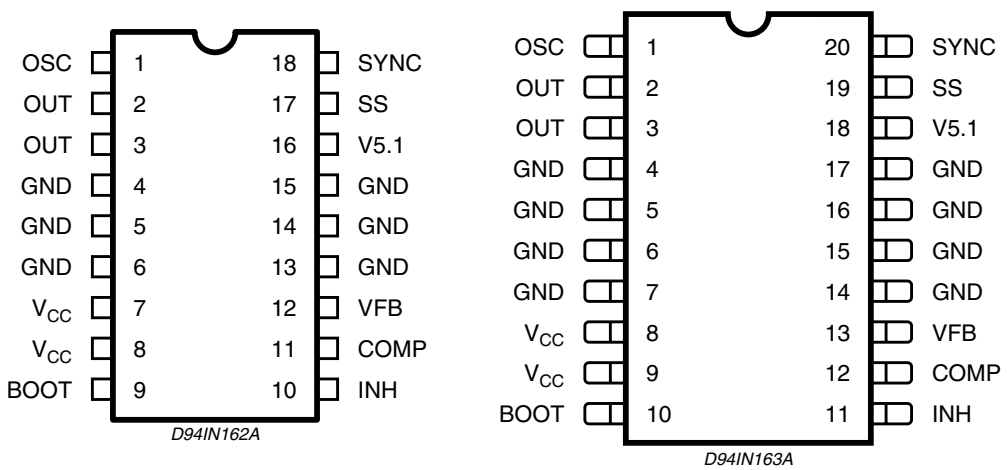
Figure 2. Block diagram



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top view)



DIP -18 (12+3+3) **SO20 (12+4+4)**

2.2 Pin description

Table 1. Pin description

N° Pin		Name	Description
DIP-18	SO-20		
11	12	COMP	E/A output to be used for frequency compensation
10	11	INH	A logic signal (active high) disables the device (sleep mode operation). If not used it must be connected to GND; if floating the device is disabled.
9	10	BOOT	A capacitor connected between this pin and the output allows to drive the internal D-MOS.
18	20	SYNC	Input/Output synchronization.
7,8	8,9	V_{CC}	Unregulated DC input voltage
2,3	2,3	OUT	Stepdown regulator output.
12	13	VFB	Stepdown feedback input. Connecting the output directly to this pin results in an output voltage of 3.3 V for the L4973V3.3 and 5.1 V for L4973V5.1. An external resistive divider is required for higher output voltages. For output voltage resistive divider is required for higher output voltages. For output voltage less than 3.3 V, see *Note: 1* and *Figure 33.*
16	18	V5.1	Reference voltage externally available.
4,5,6 13,14,15	4,5,6,7 14,15,16,17	GND	Signal ground
1	1	OSC	An external resistor connected between the unregulated input voltage and Pin 1 and a capacitor connected from Pin 1 to ground fixes the switching frequency. (Line feed forward is automatically obtained)

Note: 1 The maximum power dissipation of the package must be observed.

3 Electrical data

3.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol		Parameter	Value	Unit
DIP-18	S0-20			
V_7,V_8	V_9,V_8	Input voltage	58	V
V_2,V_3	V_2,V_3	Output DC voltage Output peak voltage at t = 0.1 µs f = 200 kHz	-1 - 5	V V
I_2,I_3	I_2,I_3	Maximum output current	int. limit.	
V_9-V_8	V_{10}-V_8		14	V
V_9	V_{10}	Bootstrap voltage	70	V
V_{11}	V_{12}	Analogs input voltage (V_{CC} = 24 V)	12	V
V_{17}	V_{19}	Analogs input voltage (V_{CC} = 24 V)	13	V
V_{12}	V_{13}	(V_{CC} = 20 V)	6 -0.3	V V
V_{18}	V_{20}	(V_{CC} = 20 V)	5.5 0.3	V V
V_{10}	V_{11}	Inhibit	V_{CC} -0.3	V V
P_{tot}		DIP 12+3+3 Power dissipation a Tpins ≤ 90 °C (T_A = 70 °C no copper area) (T_A = 70 °C 4 cm copper area on PCB)	 5 1.3 2	 W W W
		SO-20 Power dissipation a T_{pins} = 90 °C	 4	 W
T_J,T_{STG}		Junction and storage temperature	-40 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	DIP-18	SO-20	Unit
R_{thJP}	Maximum thermal resistance junction-pin	12	15	°C/W
R_{thJA}	Maximum thermal resistance junction-ambient	60 (1)	80 (1)	°C/W

1. Package mounted on board

4 Electrical characteristics

Table 4. Electrical characteristics
(Refer to the test circuit, V_{CC} = 24 V; T_J = 25 °C, C_{OSC} = 2.7 nF; R_{OSC} = 20 kΩ; unless otherwise specified)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Dynamic characteristics							
	Input voltage range (1)	V_O = V_{REF} to 40 V; I_O = 3.5A	(2)	8		55	V
	Output voltage L4973V5.1	I_O = 1 A		5.05	5.1	5.15	V
		I_O = 0.5 A to 3.5 A V_{CC} = 8 V to 55 V		5.00	5.1	5.20	V
			(2)	4.95	5.1	5.25	V
	Output voltage L4973V3.3	I_O = 1 A		3.326	3.36	3.393	V
		I_O = 0.5 A to 3.5 A V_{CC} = 8 V to 40 V		3.292	3.36	3.427	V
			(2)	3.26	3.36	3.46	V
	$R_{DS(on)}$	V_{CC} = 10.5 V I_O = 3.5 A			0.15	0.22	Ω
			(2)			0.35	Ω
	Maximum limiting current	V_{CC} = 8 V to 55 V	(2)	3.8	4.5	5.5	A
				4	4.5	5.5	A
η	Efficiency	V_O = 5.1 V; I_O = 3.5 A			90		%
		V_O = 3.3 V; I_O = 3.5 A			85		%
	Switching frequency		(2)	90	100	110	kHz
	Supply voltage ripple rejection	V_i = V_{CC}+2 V_{RMS} V_O = V_{ref}; I_O = 1 A; f_{ripple} = 100 Hz		60			dB
Δf_{sw}	Switching frequency stability vs., supply voltage	V_{CC} = 8 V to 55 V			2	5	%
Reference section							
	Reference voltage	I_{ref} = 0 to 20 mA; V_{CC} = 8 to 55 V		5.025	5.1	5.175	V
			(2)	4.950	5.1	5.250	V
	Line regulation	I_{ref} = 0 mA; V_{CC} = 8 to 55 V			5	10	mV
	Load regulation	V_{ref} = 0 to 5 mA; V_{CC} = 0 to 20 mA			2 6	10 25	mV mV
	Short circuit current			30	65	100	mA

Table 4. Electrical characteristics (continued)
(Refer to the test circuit, V_{CC} = 24 V; T_J = 25 °C, C_{OSC} = 2.7 nF; R_{OSC} = 20 kΩ; unless otherwise specified)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Soft-start							
	Soft-start charge current			30	45	60	µA
	Soft-start discharge current			15	22	30	µA
Inhibit							
	High level voltage		(2)	3.0			V
	Low level voltage		(2)			0.8	V
	I_{source} high level	V_{INH} = 3 V	(2)	10	16	50	µA
	I_{source} low level	V_{INH} = 0.8 V	(2)	10	15	50	µA
DC characteristics							
	Total operating quiescent current	Duty cycle = 50 %			4	6	mA
	Quiescent current	Duty cycle = 0			2.7	4	mA
	Total stand-by quiescent current	V_{CC} = 24 V; V_{INH} = 5 V			100	200	µA
		V_{CC} = 55 V; V_{INH} = 5 V			150	300	µA
Error amplifier							
	High level output voltage			11.0			V
	Low level output voltage					0.65	V
	Source bias current			1	2	3	µA
	Source output current			200	300	600	µA
	Sink output current			200	300		µA
	Supply voltage ripple rejection	V_{COMP} = VFB C_{REF} = 4.7 µF 1-5 mA load current		60	80		dB
	DC open loop gain	R_L = ∞		50	60		dB
	Transconductance	I_{comp} = -0.1 to 0.1 mA; V_{comp} = 6 V			2.5		mS
Oscillator section							
	Ramp valley			0.78	0.85	0.92	V
	Ramp peak	V_{CC} = 8 V V_{CC} = 55 V		1.9 9	2.1 9.6	2.3 10.2	V V
	Maximum duty cycle			95	97		%

Table 4. Electrical characteristics (continued)
(Refer to the test circuit, V_{CC} = 24 V; T_J = 25 °C, C_{OSC} = 2.7 nF; R_{OSC} = 20 kΩ; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
	Maximum frequency	Duty cycle = 0%; R_{OSC} =13 kΩ; C_{OSC} = 820 pF;			300	kHz
Sync function						
	High input voltage	V_{CC} = 8 V to 55 V	3.5			V
	Low input voltage	V_{CC} = 8 V to 55 V			0.9	V
	Slave sink current		0.15	0.25	0.45	mA
	Master output amplitude	I_{source} = 3 mA	4	4.5		V
	Output pulse width	No load, V_{sync} = 4.5 V	0.20	0.35		µs

1. Pulse testing with a low duty cycle
2. Specifications referred to T_J from -40 °C to 125 °C.

5 Evaluation board

Figure 4. Evaluation board circuit

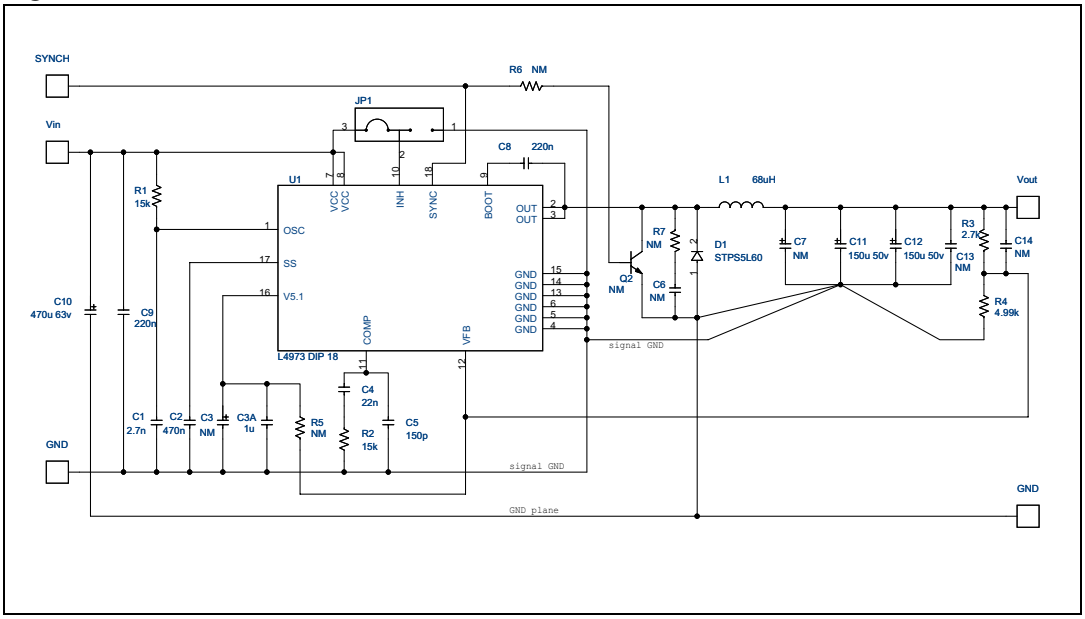


Table 5. Component list (fsw = 150 kHz, V_{OUT} = 5 V)

Reference	Description	Part number	Manufacturer
R1	Resistor 15 kΩ 1%		
R2	Resistor 15 kΩ 1%		
R3	Resistor 2.7 kΩ 1%		
R4	Resistor 4.99 kΩ 1%		
R5	Not mounted		
R6	Not mounted		
R7	Not mounted		
C1	Capacitor 2.7 nF 5%		
C2	Capacitor 470 nF 5%		
C3	Capacitor 1 µF 5%		
C4	Capacitor 22 nF 5%		
C5	Capacitor 150 pF 5%		
C6	Not mounted		
C7	Not mounted		
C8	Capacitor 220 nF 5%		
C9	Capacitor 220 nF 5%		
C10	Capacitor 470 µF 63V	EKY-630ELL471ML20S	Nippon Chemi-con

Table 5. Component list (fsw = 150 kHz, V_{OUT} = 5 V) (continued)

Reference	Description	Part number	Manufacturer
C11	Capacitor 150 µF 35 V	EKY-350ELL151MHB5D	Nippon Chemi-con
C11	Capacitor 150 µF 35 V	EKY-350ELL151MHB5D	Nippon Chemi-con
C13	Capacitor 100 nF 5 %		
C14	Not mounted		
L1	68 µH I_{RMS} = 3.4 A I_{SAT} = 6.7 A	DO5040H-683MLD	Coilcraft
U1		L4973V3.3	STMicroelectronics

Table 6. Resistor divider for V_{OUT} = 12 V

Reference	Description	Part number	Manufacturer
R3	Resistor 2.7 kΩ 1%		
R4	Resistor 1 kΩ 1%		

Table 7. Resistor divider for V_{OUT} = 3.3 V

Reference	Description	Part number	Manufacturer
R3	Resistor 2.7 kΩ 1%		
R4	Not mounted		

Figure 5. Evaluation board (components side)

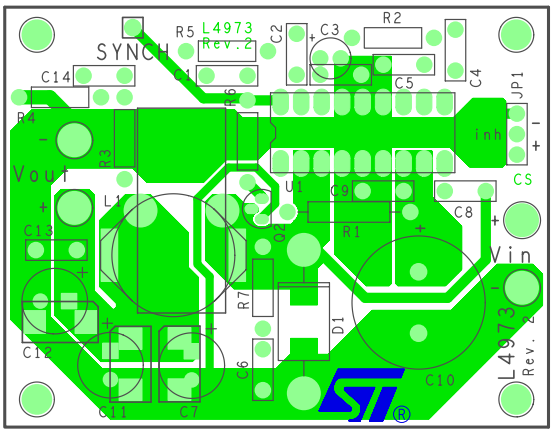
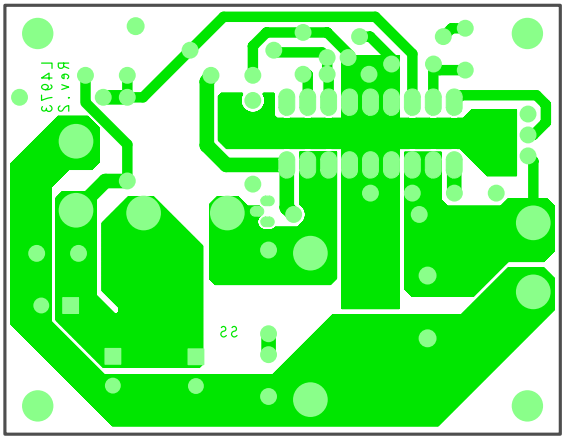


Figure 6. Evaluation board (solder side)



6 Application circuit

Figure 7. Application circuit (see *Figure 4* part list)

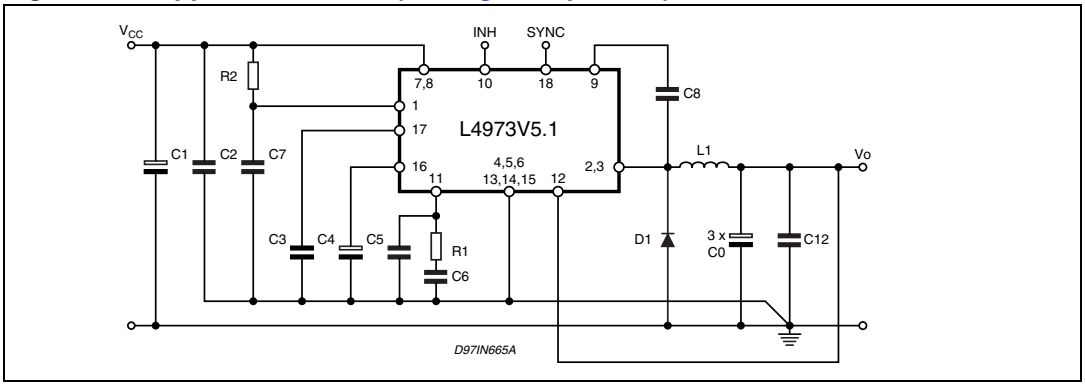
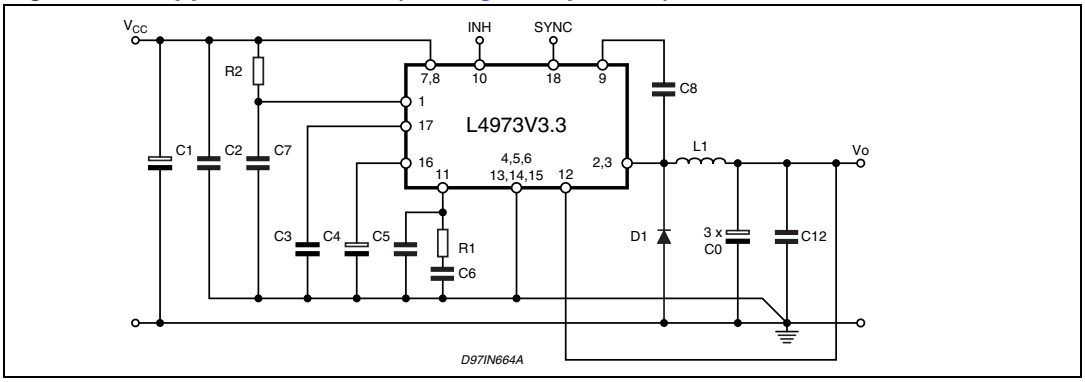


Figure 8. Application circuit (see *Figure 4* part list)



7 Typical characteristics

Figure 9. Quiescent drain current vs. input voltage (0% duty cycle)

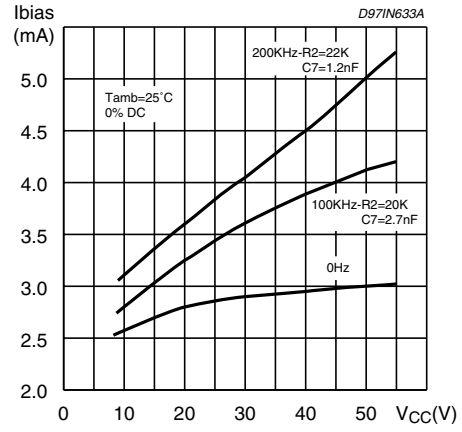


Figure 10. Quiescent drain current vs. junction temperature

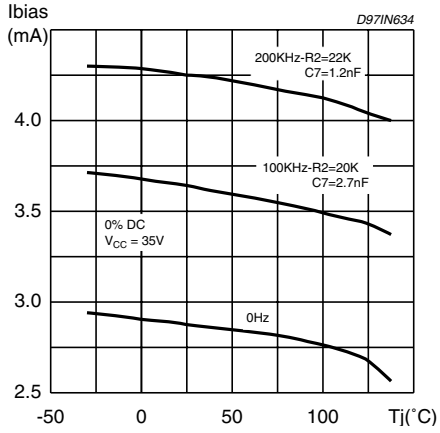


Figure 11. Stand by drain current vs. input voltage

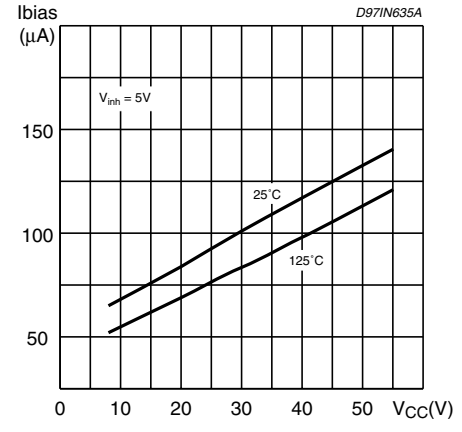


Figure 12. Reference voltage vs. junction temperature (pin 16)

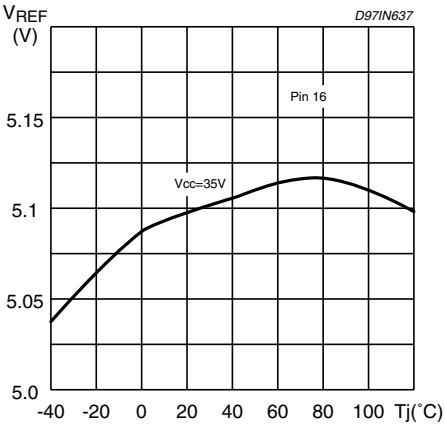


Figure 13. Reference voltage vs. input voltage (pin 16)

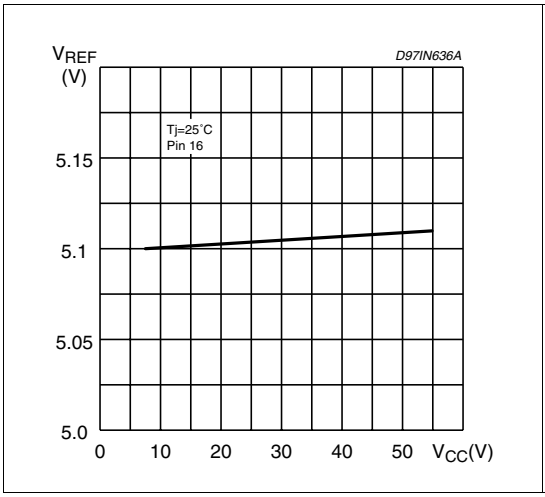


Figure 14. Reference voltage vs. reference input current

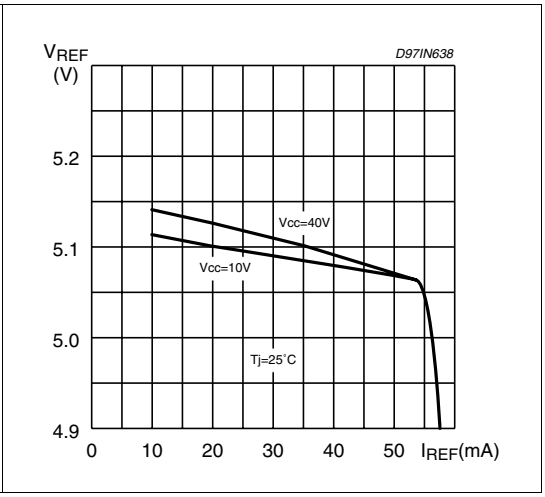


Figure 15. Inhibit current vs. inhibit voltage (pin 10)

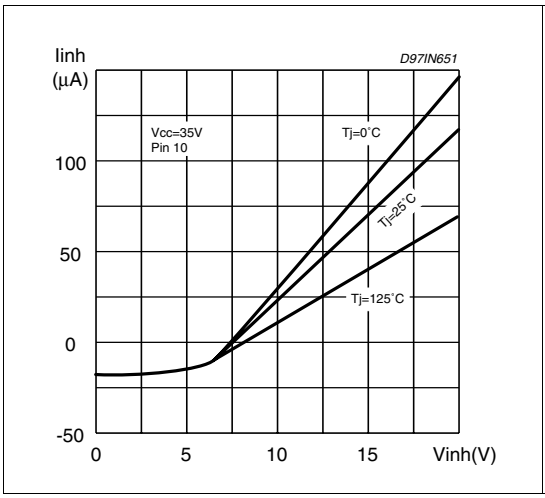


Figure 16. Line regulation (see *Figure 7*)

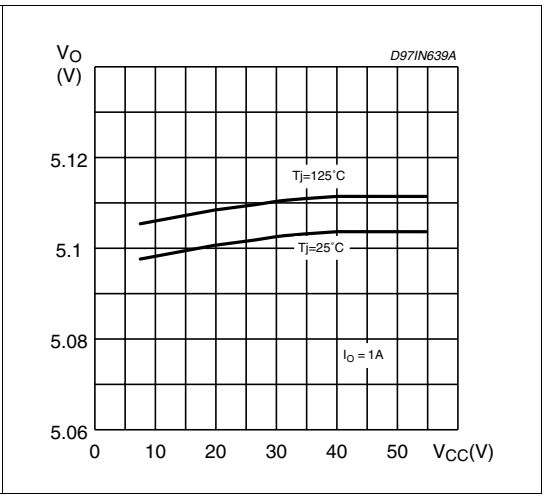


Figure 17. Load regulation (see *Figure 7*)

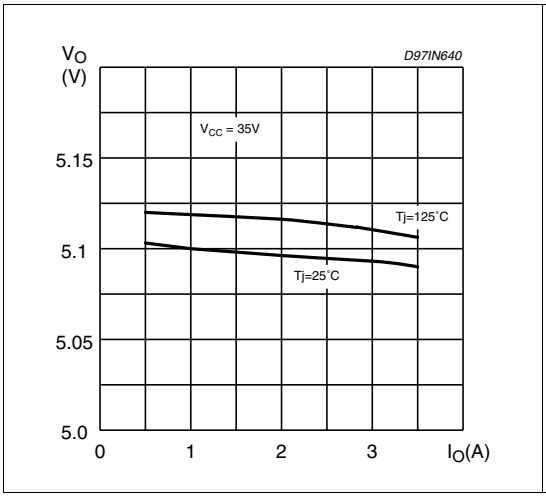


Figure 18. Line regulation (see *Figure 8*)

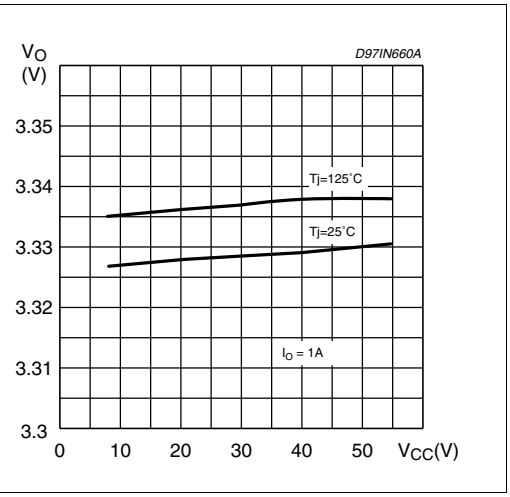


Figure 19. Load regulation (see *Figure 4*)

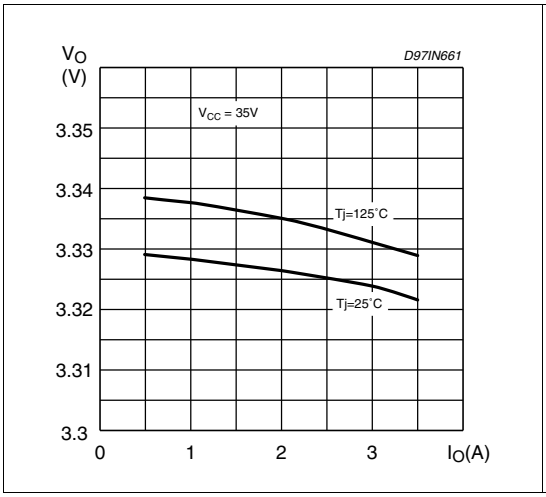


Figure 20. Switching frequency vs. R2 and C7 (*Figure 4*)

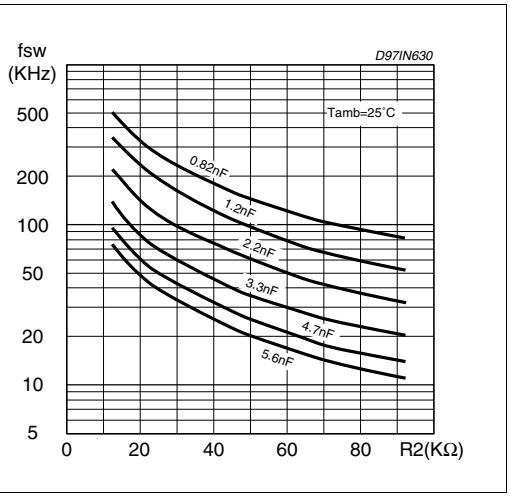


Figure 21. Switching frequency vs. input voltage

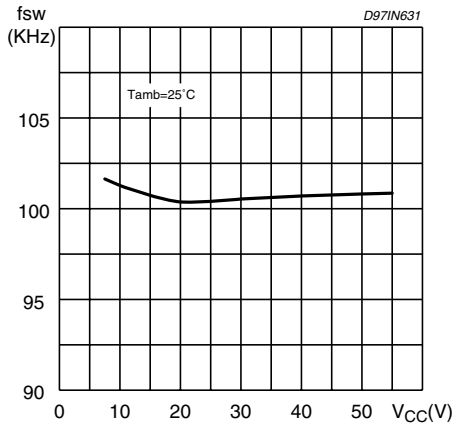


Figure 22. Switching frequency vs. junction temperature (see *Figure 4*)

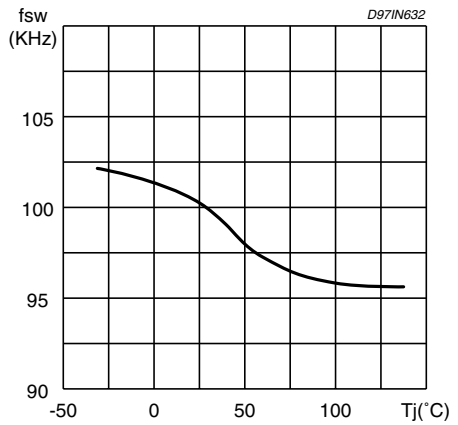


Figure 23. Dropout voltage between pin 7,8 and 2,3

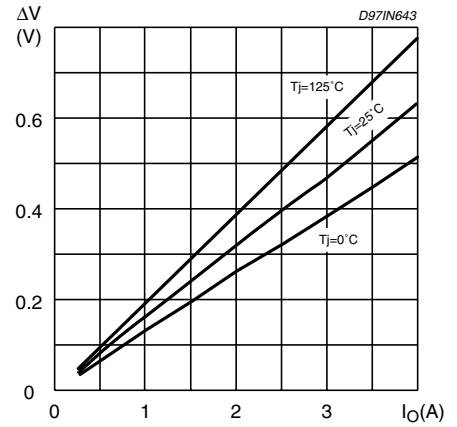


Figure 24. Efficiency vs. output voltage (see *Figure 6*)

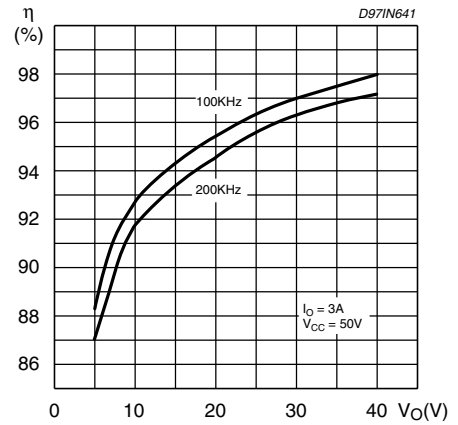


Figure 25. Dropout voltage between pin 7,8 and 2,3

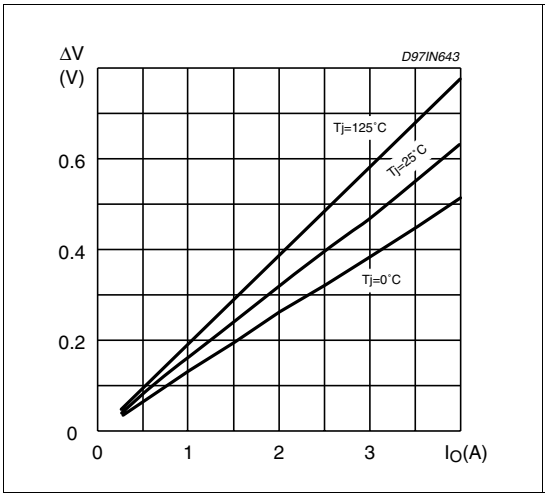


Figure 26. Efficiency vs. output voltage (see *Figure 4*)

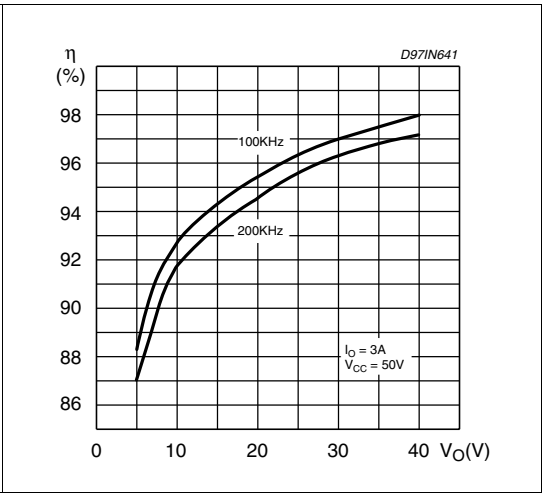


Figure 27. Efficiency vs. output voltage (Diode STPS745D)

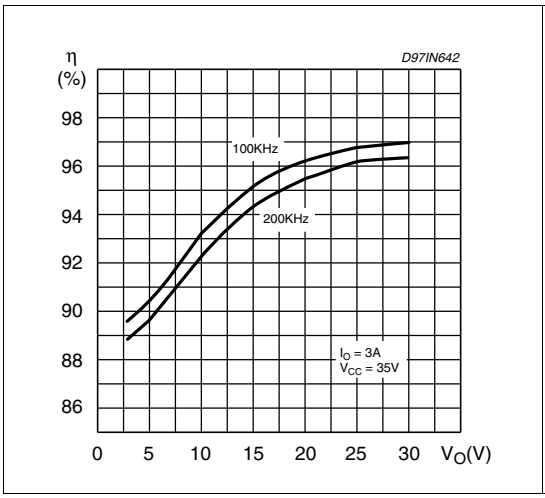


Figure 28. Efficiency vs. output current (see *Figure 7*)

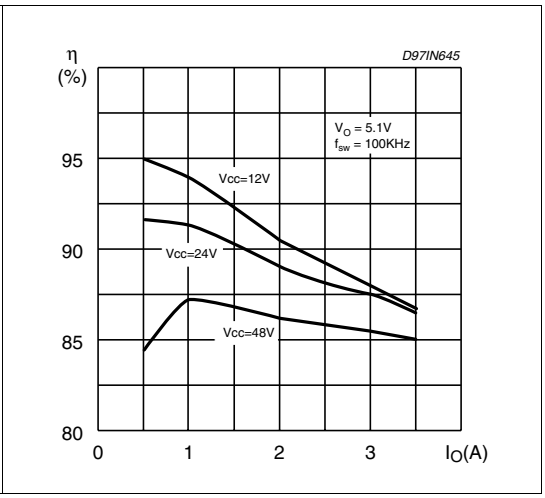


Figure 29. Efficiency vs. output current (see *Figure 7*)

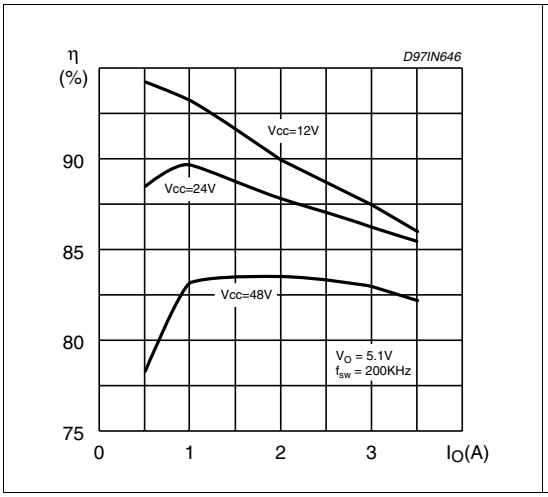


Figure 30. Efficiency vs. output current (see *Figure 8*)

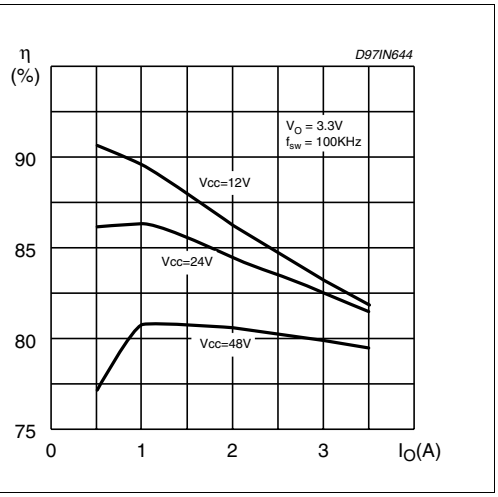


Figure 31. Efficiency vs. output current (see *Figure 8*)

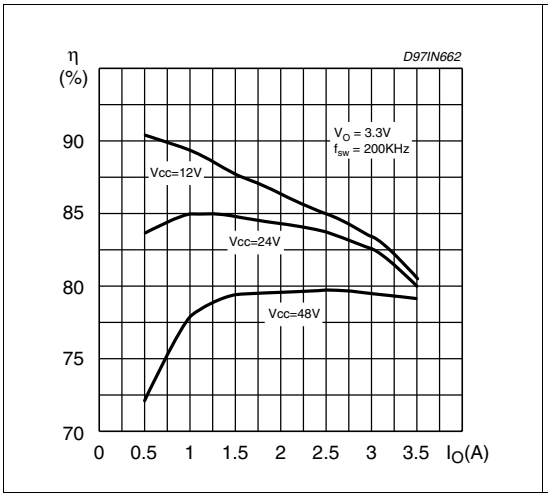


Figure 32. Power dissipation vs. input voltage (device only) (see *Figure 7*)

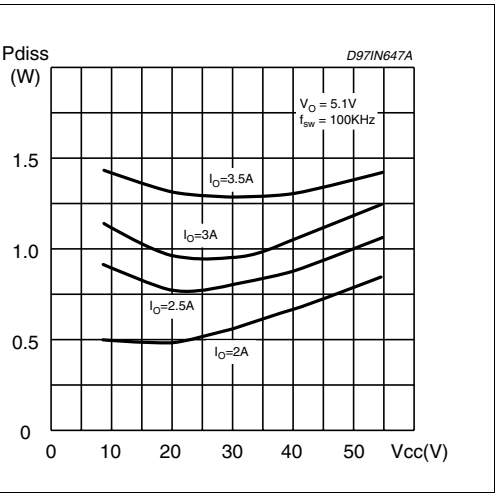


Figure 33. Power dissipation vs. output voltage (device only)

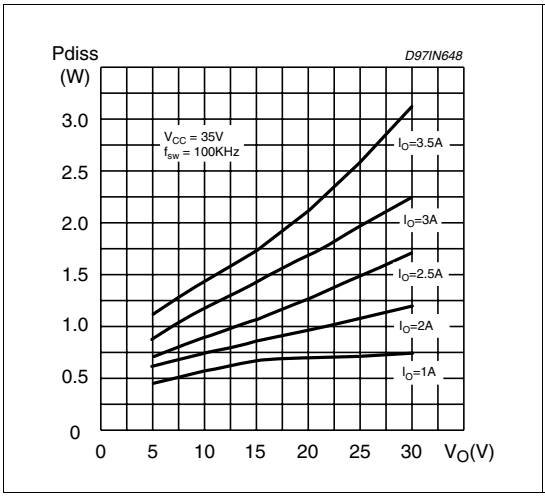


Figure 34. Pulse by pulse limiting current vs. junction temperature

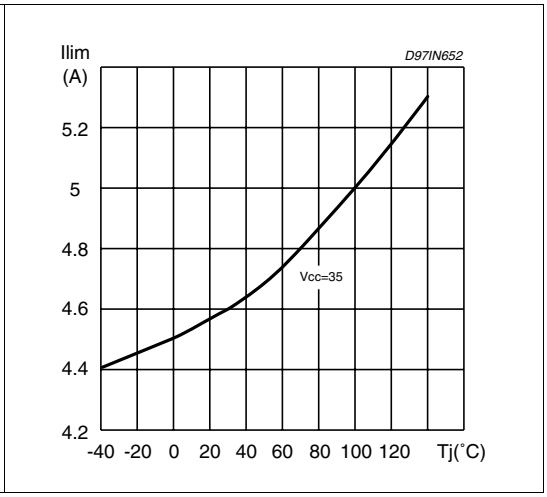


Figure 35. Load transient

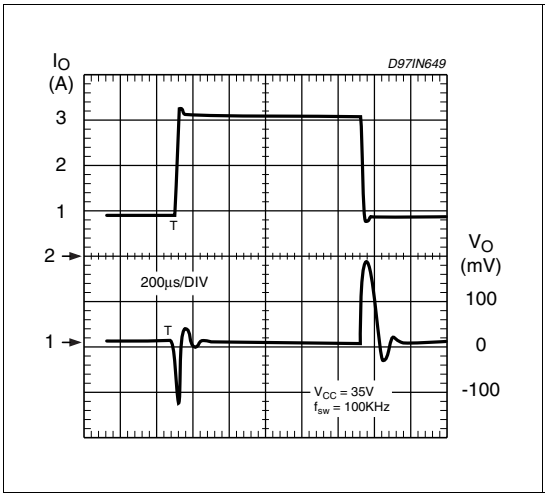


Figure 36. Line transient

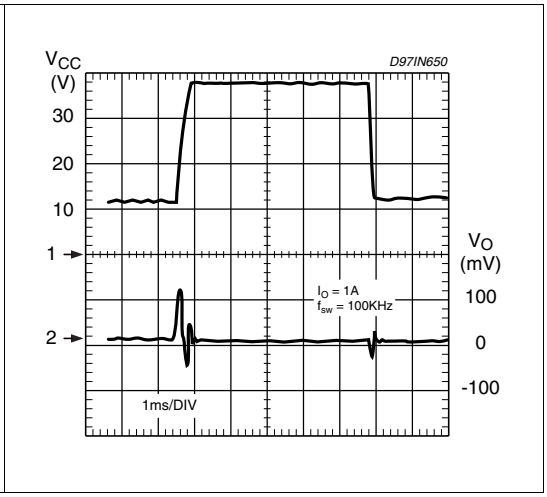


Figure 37. Source current rise and fall time, pin 2, 3 (see *Figure 4*)

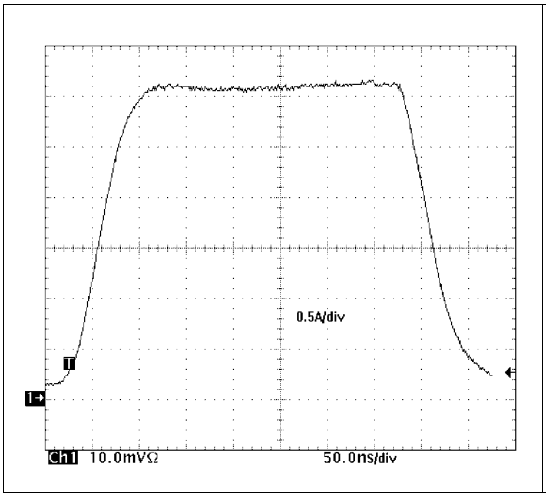


Figure 38. Soft-start capacitor selection vs. inductor and V_{CC} max (ref. AN938)

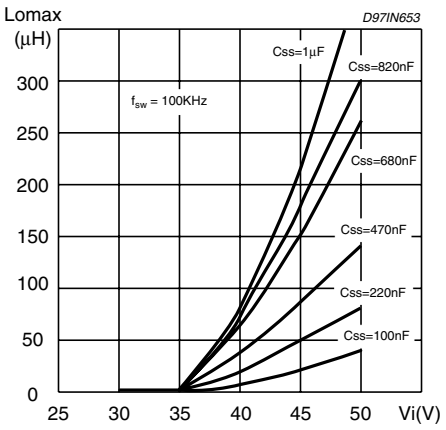


Figure 39. Soft-start capacitor selection vs. inductor and V_{CC} max (ref. AN938)

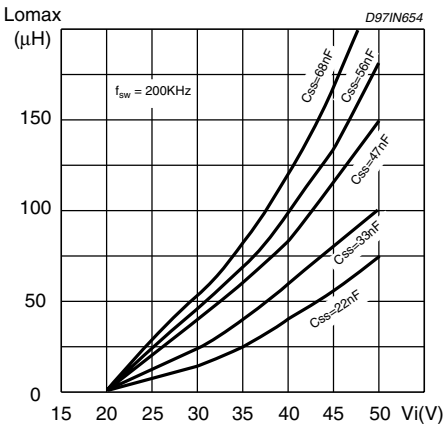
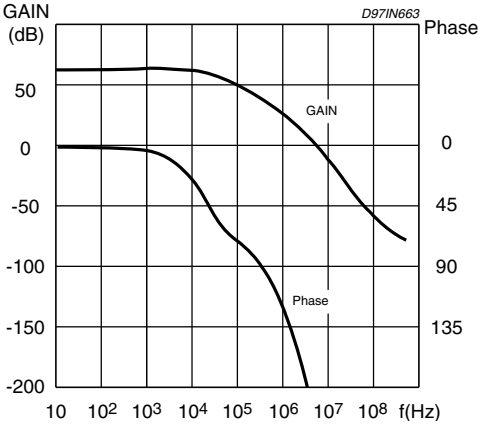


Figure 40. Open loop frequency and phase of error amplifier



8 Application ideas

Figure 41. 3.5 A at V_O < 3.3 V (see part list *Figure 4*)

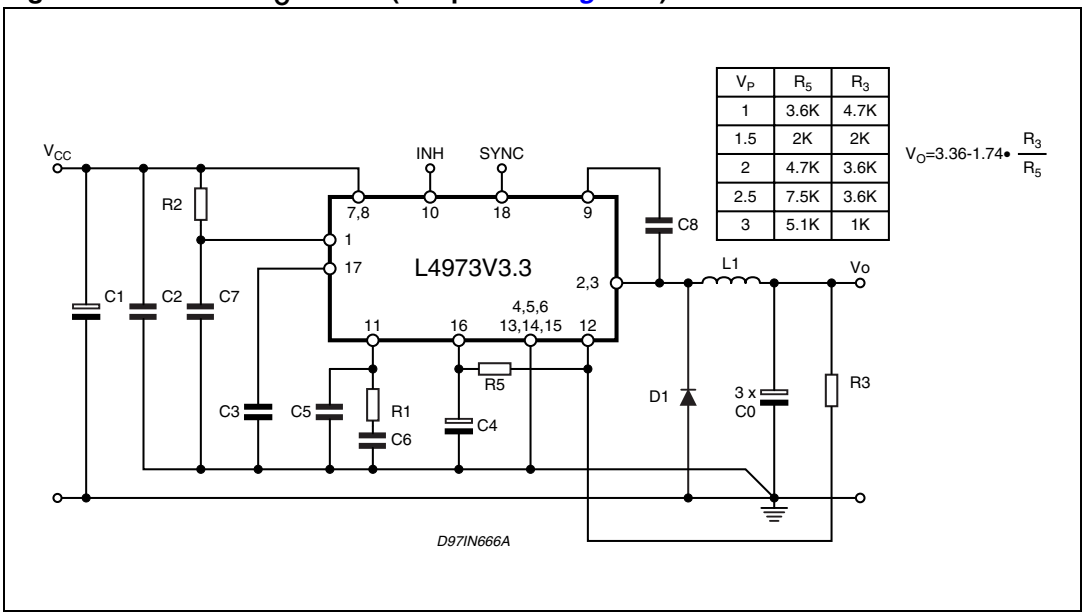


Figure 42. 12 V to 3.3 V high performance buck converter (fsw = 200 kHz)

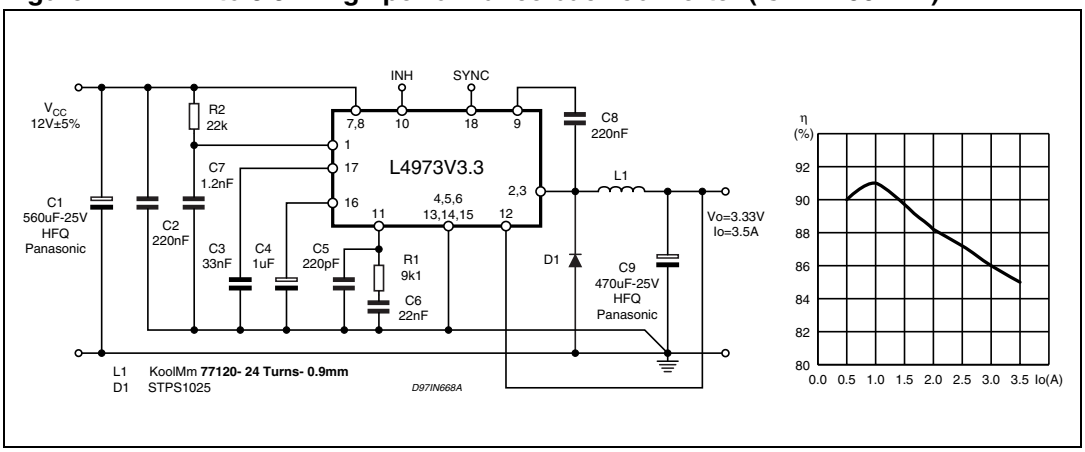


Figure 43. Synchronization example

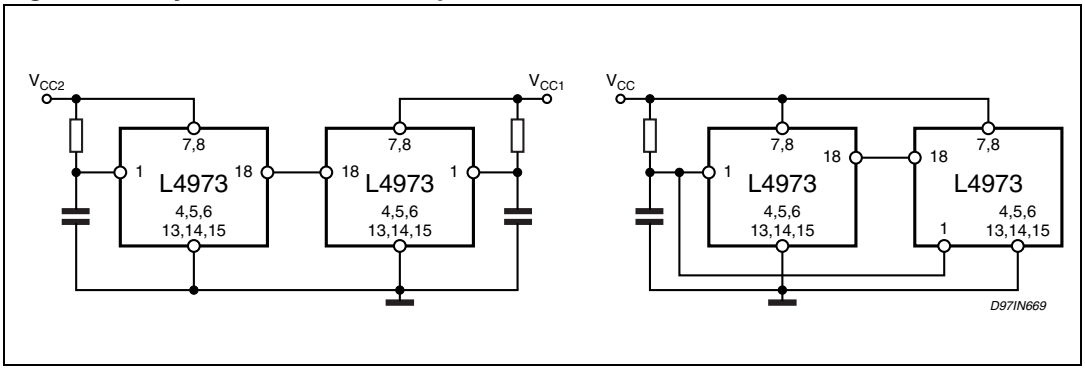
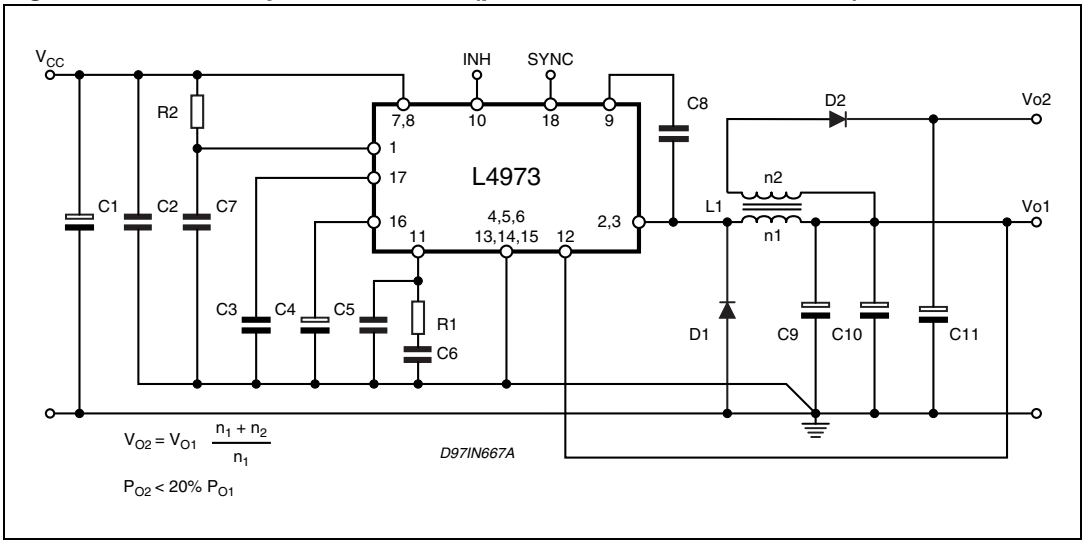


Figure 44. Multi output not isolated (pin out referred to DIP12+3+3)



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. DIP-18 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100

Figure 45. Package dimensions

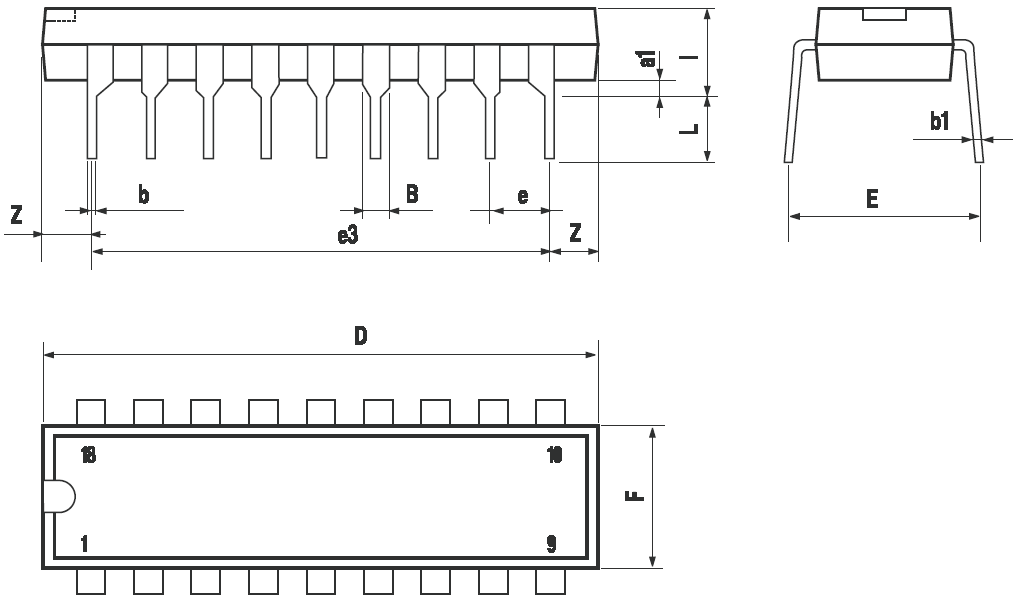
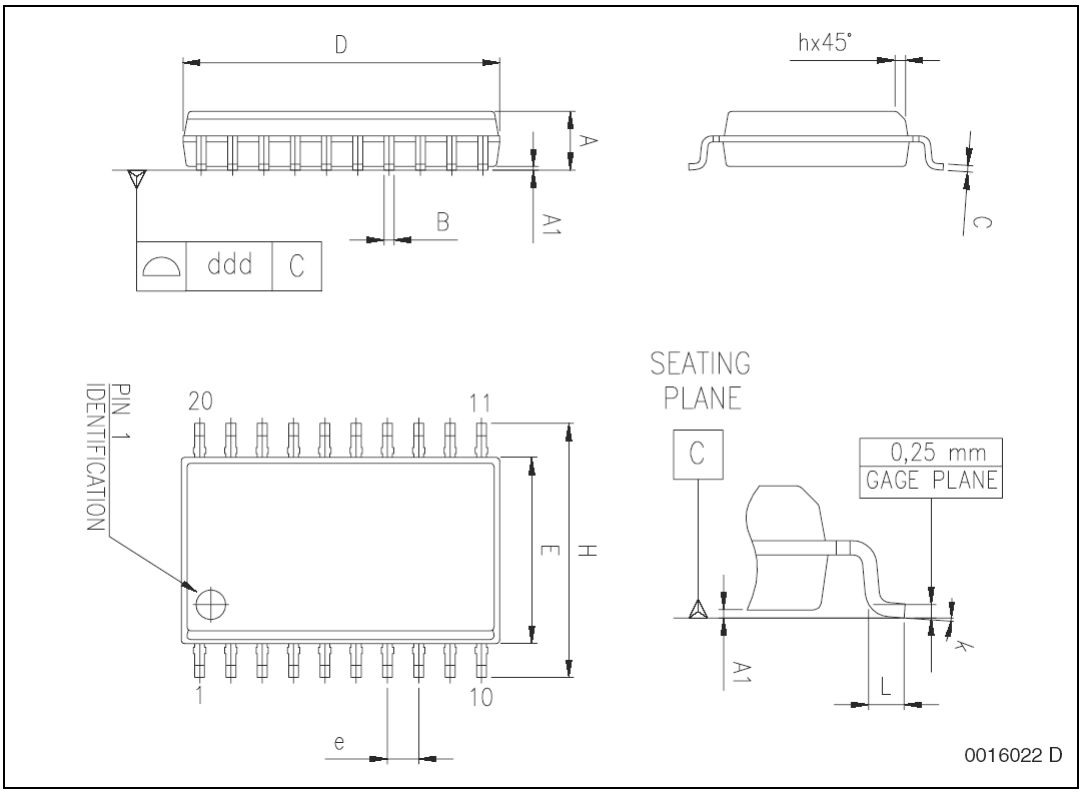


Table 9. SO-20 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Figure 46. Package dimensions



10 Order code

Table 10. Order code

Part number	Package	Packaging
L4973D3.3, E-L4973D3.3	SO-20	Tube
L4973D3.3-013TR, E-L4973D3.3-TR	SO-20	Tape and reel
L4973D5.1	SO-20	Tube
L4973D5.1-013TR	SO-20	Tape and reel
L4973V3.3, E-L4973V3.3	DIP-18	Tube
L4973V5.1, E-L4973V5.1	DIP-18	Tube

11 Revision history

Table 11. Document revision history

Date	Revision	Changes
12-Sep-2001	13	First Issue
07-May-2005	14	Updated the Layout look & feel. Changed name of the D1 on the fig. 5.
14-Dec-2005	15	Added the ECOPACK part numbers in the Table 1. Order Codes.
06-Dec-2006	16	The document has been reformatted, and order codes updated
07-May-2007	17	New data on *Table 4*
26-Feb-2009	18	Updated *Section 5: Evaluation board on page 9*

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