Features

Switch Management

- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K entry MAC Address look-up engine and a store-and-forward architecture
- Fully compliant with IEEE802.3u standards
- Full-duplex IEEE 802.3x flow control (Pause) with force mode option
- Half-duplex back pressure flow control

Advanced Switch Management

- IEEE 802.1Q VLAN support for up to 16 groups (full-range of VLAN IDs)
- VLAN ID tag/untag options, per port basis
- IEEE 802.1p/Q tag insertion or removal on a per-port basis (egress)
- Programmable rate limiting at the ingress and egress port
- Broadcast storm protection
- IEEE 802.1d spanning tree protocol support
- MAC filtering function to filter unicast packets
- Unknown MAC address forwarding function
- Direct forwarding mode enabling the processor to identify the ingress port and to specify the egress port
- IGMP v1/v2 snooping support for multicast packet filtering
- IPV6 Multicast Listener Discovery (MLD) snooping support

Monitoring

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- Management information base (MIB) counters for fully compliant statistics gathering: 32 MIB counters per port
- Loop back modes for remote failure diagnostics

Comprehensive Register Access

- There are three kinds of register groups:
- The PCI configuration registers are used to initialize and configure the PCI interface
- The PCI control/status registers are used to communicate between the host and KSZ8842-PMQL/PMBL
- Switch registers are used to support transceiver control and status. They are configurable on-the-fly (port-priority, 802.1p/d/Q, etc.)

QoS/CoS Packets Prioritization Support

- Per port, 802.1p and DiffServ based
- Re-mapping of 802.1p priority field on a per port basis

Power Modes, Packaging, and Power Supplies

- Full-chip hardware power-down (register configuration not saved) provides for low power dissipation
- Per port-based software power-save on PHY (idle link detection, register configuration preserved)
- Single power supply: 3.3V
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-pin PQFP and 100-ball LFBGA

Additional Features

In addition to offering all of the features of an integrated Layer-2 managed switch, the KSZ8842-PMQL/PMBL offers:

- Repeater mode capabilities to allow for cut through in latency critical Industrial Ethernet or Embedded Ethernet applications
- Dynamic buffer memory scheme essential for applications such as Video over IP where image jitter is unacceptable
- 2-Port switch with a 32-bit/33MHz PCI processor interface.
- Micrel LinkMD® cable diagnostics to determine cable length, diagnose faulty cables, and determine distance-to-fault
- Hewlett Packard (HP) Auto MDI-X crossover with disable and enable options
- Four priority queues to handle voice, video, data, and control packets
- Ability to transmit and receive jumbo frame sizes up to 1916 bytes

Applications

- Video Distribution Systems
- High-end Cable, Satellite, and IP set-top boxes
- Video over IP
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

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Ordering Information

Part Number	Operation Temp. Range	Package
KSZ8842-PMQL	0°C to 70°C	128-Pin PQFP
KSZ8842-PMQLI **(Industrial grade)**	-40°C to +85°C	128-Pin PQFP
KSZ8842-PMBL	0°C to 70°C	100-Ball LFBGA
KSZ8842-PMBL AM **(Industrial/Automotive grade)**	-40°C to +85°C	100-Ball LFBGA

Revision History

Revision	Date	Summary of Changes
1.0	09/29/05	Data sheet created.
1.1	01/13/06	Package information updated.
1.2	01/16/07	Update support transformer, table and other.
1.3	04/17/07	Add the base address and range for host MIB, change description for soft reset and other.
1.4	06/01/07	Add the package thermal information in the operating ratings.
1.5	10/02/07	Add the KSZ8842-PMBL BGA device information.

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Pin Configuration

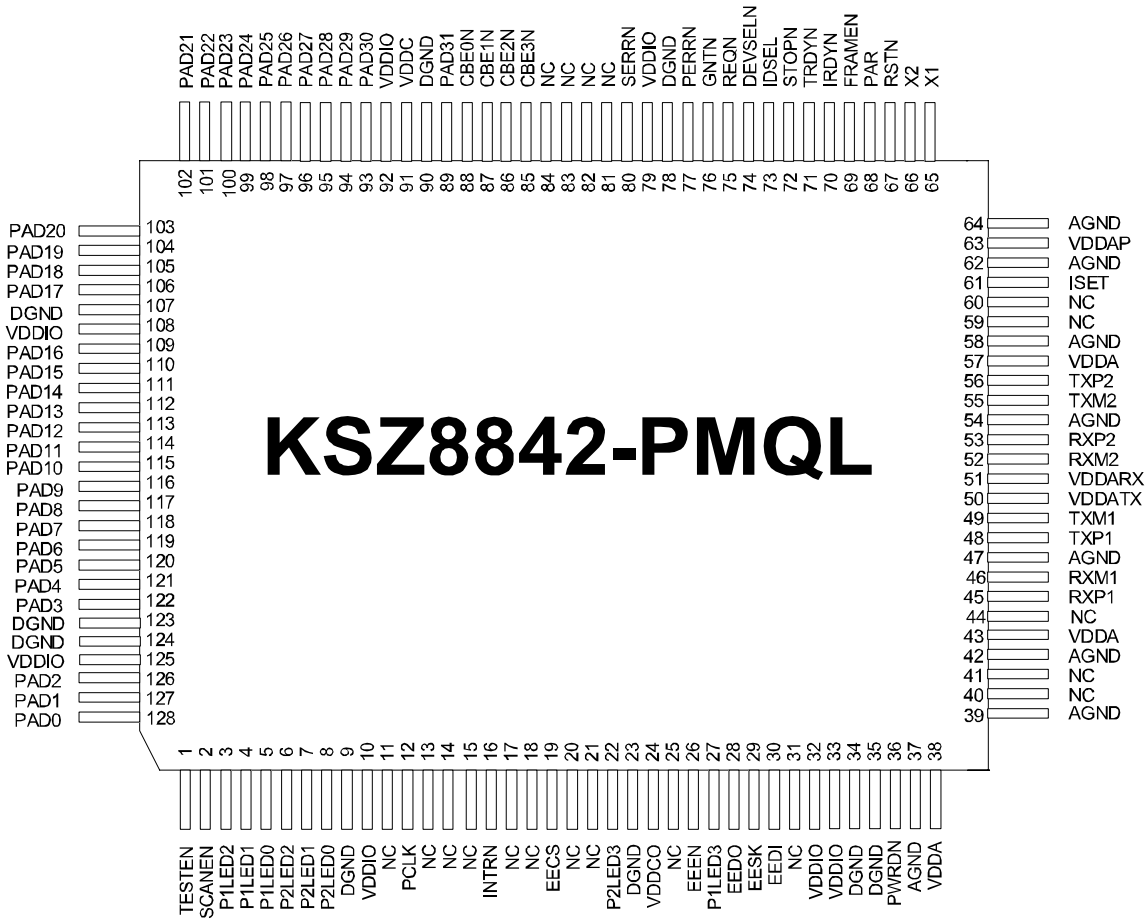

Figure 2. KSZ8842-PMQL 128-Pin PQFP (Top View)

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Balls Configuration

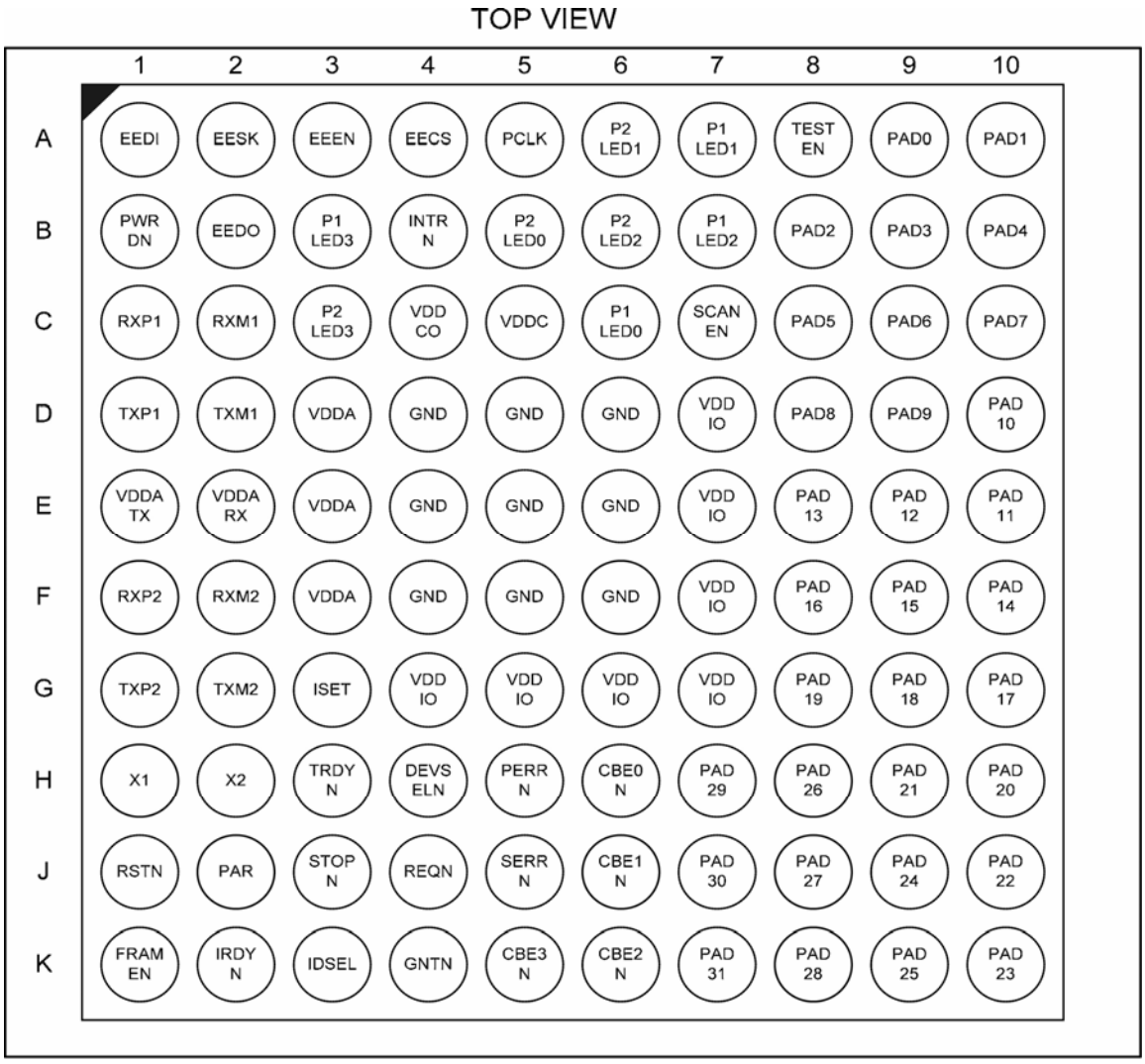

Figure 3. KSZ8842-PMBL 100-Ball LFBGA (Top View)

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Pins Description of KSZ8842-PMQL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Pin Function</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>3
4
5
6
7
8</td><td>P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td>Opu
Opu
Opu
Opu
Opu
Opu</td><td>Port 1 and Port 2 LED indicators[1] defined as follows:
LEDs turn on when low.
<table>
<tr><td></td><td colspan="2">Chip Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1]</td></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">Reg. SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[1,0]</td><td>[1,1]</td></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is pin 27. P2LED3 is pin 22

Port 1 and Port 2 LED indicators[1] for Repeater mode defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1] [1,0],[1,1]</td></tr>
<tr><td>P1LED3/P2LED3</td><td>RPT_COL, RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>RPT_Link3/RX, RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>RPT_Link2/RX, RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>RPT_Link1/RX, RPT_ERR1</td><td>—</td></tr>
</table>
Note:
1. RPT_COL = Blink; RPT_Link3/RX (Host port) = On/Blink;
RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink;
RPT_ACT = On if any activity; RPT_ERR3 (Host port) = On if any CRC error;
RPT_ERR2 (port 2) = On if any CRC error; RPT_ERR1 (port 1) = On if any CRC error;</td></tr>
<tr><td>9</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital I/O V_{DD}</td></tr>
</table>

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Pin Number	Pin Name	Type	Pin Function
11	NC	—	No connect
12	PCLK	Ipd	***PCI Bus Clock*** This Clock provides the timing for all PCI bus phases. The rising edge defines the start of each phase. The clock maximum frequency is 33MHz.
13	NC	—	No connect
14	NC	—	No connect
15	NC	—	No connect
16	INTRN	Opd	***Interrupt Request*** Active Low signal to host CPU to request an interrupt when any one of the interrupt conditions occurs in the registers. This pin should be pull-up externally.
17	NC	—	No connect
18	NC	—	No connect
19	EECS	Opu	***EEPROM Chip Select*** This signal is used to select an external EEPROM device
20	NC	—	No connect
21	NC	—	No connect
22	P2LED3	Opd	***Port 2 LED Indicator*** See the description in pins 6, 7, and 8.
23	DGND	Gnd	Digital IO Ground
24	VDDCO	P	***1.2V Core Voltage Output. (Internal 1.2V LDO power supply output)*** This pin is used to provide 1.2V power supply to all 1.2V power VDDC, VDDA and VDDAP. It is recommended the pin should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
25	NC	—	No connect
26	EEEN	Ipd	***EEPROM Enable*** EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
27	P1LED3	Opd	***Port 1 LED Indicator*** See the description in pins 3, 4, and 5.
28	EEDO	Opd	***EEPROM Data Out*** This pin is connected to DI input of the serial EEPROM.
29	EESK	Opd	***EEPROM Serial Clock*** 4µs serial clock to load configuration data from the serial EEPROM.
30	EEDI	Ipd	***EEPROM Data In*** This pin is connected to DO output of the serial EEPROM.
31	NC	—	No connect
32	VDDIO	P	3.3V digital I/O V_{DD}.
33	VDDIO	P	3.3V digital I/O V_{DD}.
34	DGND	Gnd	Digital ground
35	DGND	Gnd	Digital ground
36	PWRDN	Ipu	Full-chip power-down input. Active Low.
37	AGND	Gnd	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	Gnd	Analog ground
40	NC	—	No connect

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Pin Number	Pin Name	Type	Pin Function
41	NC	—	No connect
42	AGND	Gnd	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	NC	—	No connect
45	RXP1	I/O	Physical receive (MDI) or transmit (MDIX)signal (+ differential)
46	RXM1	I/O	Physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	Gnd	Analog ground
48	TXP1	I/O	Physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}
51	VDDARX	P	3.3V analog V_{DD}
52	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX)signal (- differential)
53	RXP2	I/O	Port 2 physical receive(MDI) or transmit (MDIX) signal (+ differential)
54	AGND	Gnd	Analog ground
55	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential)
56	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
57	VDDA	P	1.2 analog V_{DD}
58	AGND	Gnd	Analog ground
59	NC	—	No connect
60	NC	—	No connect
61	ISET	O	***Set physical transmit output current*** Pull-down this pin with a 3.01K 1% resistor to ground.
62	AGND	Gnd	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL
64	AGND	Gnd	Analog ground
65	X1	I	***25MHz crystal/oscillator clock connections*** Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is not connected. Note: Clock is ±50ppm for both crystal and oscillator.
66	X2	O	
67	RSTN	Ipu	***Hardware Reset, Active Low*** RSTN will cause the KSZ8842-PMQL to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 ms.
68	PAR	I/O	***PCI Parity*** Even parity computed for PAD [31:0] and CBE [3:0]N, master drives PAR for address and write data phase, target drives PAR for read data phase.
69	FRAMEN	I/O	***PCI Cycle Frame*** This signal is asserted low to indicate the beginning of the address phase of the bus transaction and de-asserted before the final transfer of the data phase of the transaction in a bus master mode. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
70	IRDYN	I/O	***PCI Initiator Ready*** As a bus master, this signal is asserted low to indicate valid data phases on PAD [31:0] during write data phases, indicates it is ready to accept data during read data phases. As a target, it'll monitor this IRDYN signal that indicates the master has put the data on the bus.

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Pin Number	Pin Name	Type	Pin Function
71	TRDYN	I/O	***PCI Target Ready*** As a bus target, this signal is asserted low to indicate valid data phases on PAD [31:0] during read data phases, indicating it is ready to accept data during write data phases. As a master, it will monitor this TRDYN signal that indicates the target is ready for data during read/write operation.
72	STOPN	I/O	***PCI Stop*** This signal is asserted low by the target device to stop the current transaction.
73	IDSEL	I/O	***PCI Initialization Device Select*** This signal is used to select the KSZ8842-PMQL during configuration read and write transactions.
74	DEVSELN	I/O	***PCI Device Select*** This signal is asserted low when it is selected as a target during a bus transaction. As a bus master, the KSZ8842-PMQL samples this signal to insure that the destination address for the data transfer is recognized by a PCI target.
75	REQN	O	***PCI Bus Request*** The KSZ8842-PMQL will assert this signal low to request PCI bus master operation.
76	GNTN	I	***PCI Bus Grant*** This signal is asserted low to indicate to the KSZ8842-PMQL that it has been granted the PCI bus master operation.
77	PERRN	I/O	***PCI Parity Error*** The KSZ8842-PMQL as a master or target will assert this signal low to indicate a parity error on any incoming data. As a bus master, it will monitor this signal on all write operations.
78	DGND	Gnd	Digital I/O ground
79	VDDIO	P	3.3V digital I/O V_{DD}
80	SERRN	O	***PCI System Error*** This system error signal is asserted low by the KSZ8842-PMQL.This signal is used to report address parity errors.
81	NC	—	No connect
82	NC	—	No connect
83	NC	—	No connect
84	NC	—	No connect
85	CBE3N	I	***Command and Byte Enable*** These signals are multiplexed on the same PCI pins. During the address phase, these lines define the bus command. During the data phase, these lines are used as Byte Enables. The Byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
86	CBE2N	I	
87	CBE1N	I	
88	CBE0N	I	
89	PAD31	I/O	***PCI Address / Data 31*** Address and data are multiplexed on the all of the PAD pins. The PAD pins carry the physical address during the first clock cycle of a transaction, and carry data during the subsequent clock cycles.
90	DGND	Gnd	Digital core ground
91	VDDC	P	1.2V digital core V_{DD}
92	VDDIO	P	3.3V digital I/O V_{DD}
93	PAD30	I/O	PCI Address / Data 30
94	PAD29	I/O	PCI Address / Data 29
95	PAD28	I/O	PCI Address / Data 28

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Pin Number	Pin Name	Type	Pin Function
96	PAD27	I/O	PCI Address / Data 27
97	PAD26	I/O	PCI Address / Data 26
98	PAD25	I/O	PCI Address / Data 25
99	PAD24	I/O	PCI Address / Data 24
100	PAD23	I/O	PCI Address / Data 23
101	PAD22	I/O	PCI Address / Data 22
102	PAD21	I/O	PCI Address / Data 21
103	PAD20	I/O	PCI Address / Data 20
104	PAD19	I/O	PCI Address / Data 19
105	PAD18	I/O	PCI Address / Data 18
106	PAD17	I/O	PCI Address / Data 17
107	DGND	Gnd	Digital I/O ground
108	VDDIO	P	3.3V digital I/O V_{DD}
109	PAD16	I/O	PCI Address / Data 16
110	PAD15	I/O	PCI Address / Data 15
111	PAD14	I/O	PCI Address / Data 14
112	PAD13	I/O	PCI Address / Data 13
113	PAD12	I/O	PCI Address / Data 12
114	PAD11	I/O	PCI Address / Data 11
115	PAD10	I/O	PCI Address / Data 10
116	PAD9	I/O	PCI Address / Data 9
117	PAD8	I/O	PCI Address / Data 8
118	PAD7	I/O	PCI Address / Data 7
119	PAD6	I/O	PCI Address / Data 6
120	PAD5	I/O	PCI Address / Data 5
121	PAD4	I/O	PCI Address / Data 4
122	PAD3	I/O	PCI Address / Data 3
123	DGND	Gnd	Digital I/O ground
124	DGND	Gnd	Digital core ground
125	VDDIO	P	3.3V digital I/O V_{DD}
126	PAD2	I/O	PCI Address / Data 2
127	PAD1	I/O	PCI Address / Data 1
128	PAD0	I/O	PCI Address / Data 0

Table 1. KSZ8842-PMQL Pin Description

Notes:

P = Power supply.
Gnd = Ground.
I = Input.
O = Output.
I/O = Bi-directional.
Ipd = Input with internal pull-down.
Ipu = Input with internal pull-up.
Opd = Output with internal pull-down.
Opu = Output with internal pull-up.

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Balls Description of KSZ8842-PMBL

<table>
<tr><th>Ball Number</th><th>Ball Name</th><th>Type</th><th>Ball Function</th></tr>
<tr><td>A8</td><td>TEST_EN</td><td>I</td><td>Test Enable.
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>C7</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable.
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>B7
A7
C6
B6
A6
B5</td><td>P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td>Opu
Opu
Opu
Opu
Opu
Opu</td><td>Port 1 and Port 2 LED indicators[1] defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1]</th></tr>
<tr><td>P1LED3[2] /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Act</td><td>100Link/Act</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>10Link/Act</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full duplex</td></tr>
</table>
<table>
<tr><th></th><th colspan="2">Reg. SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[1,0]</th><th>[1,1]</th></tr>
<tr><td>P1LED3[2] P2LED3</td><td>Act</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Notes:
1. Link = On; Activity = Blink; Link/Act = On/Blink; Full Dup/Col = On/Blink;
Full Duplex = On (Full duplex); Off (Half duplex)
Speed = On (100BASE-T); Off (10BASE-T)
2. P1LED3 is ball B3. P2LED3 is ball C3.

Port 1 and Port 2 LED indicators[3] for Repeater mode defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1] [1,0] [1,1]</th></tr>
<tr><td>P1LED3 , P2LED3</td><td>RPT_COL, RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2, P2LED2</td><td>RPT_Link3/RX, RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1, P2LED1</td><td>RPT_Link2/RX, RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0, P2LED0</td><td>RPT_Link1/RX, RPT_ERR1</td><td>—</td></tr>
</table>
Note 3: RPT_COL = Blink; RPT_Link3/RX (Host port) = On/Blink;
RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink;
RPT_ACT = On if any activity; RPT_ERR3 (Host port) = On if any CRC error;
RPT_ERR2 (port 2) = On if any CRC error; RPT_ERR1 (port 1) = On if any CRC error;</td></tr>
<tr><td>A5</td><td>PCLK</td><td>Ipd</td><td>PCI Bus Clock. This Clock provides the timing for all PCI bus phases. The rising edge</td></tr>
</table>

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Ball Number	Ball Name	Type	Ball Function
			defines the start of each phase. The clock maximum frequency is 33MHz.
B4	INTRN	Opd	Interrupt Request. Active Low signal to host CPU to request an interrupt when any one of the interrupt conditions occurs in the registers. This pin should be pull-up externally.
A4	EECS	Opu	EEPROM Chip Select. This signal is used to select an external EEPROM device
C3	P2LED3	Opd	Port 2 LED Indicator See the description in ball B5, B6 and A6.
A3	EEEN	Ipd	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
B3	P1LED3	Opd	Port 1 LED indicator See the description in ball C7, A7 and B7.
B2	EEDO	Opd	EEPROM Data Out: This pin is connected to DI input of the serial EEPROM.
A2	EESK	Opd	EEPROM Serial Clock: A 4µs serial output clock to load configuration data from the serial EEPROM.
A1	EEDI	Ipd	EEPROM Data In: This pin is connected to DO output of the serial EEPROM.
B1	PWRDN	Ipu	Full-chip power-down. Active Low.
C1	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
C2	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
D1	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
D2	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
F2	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX)signal (- differential)
F1	RXP2	I/O	Port 2 physical receive(MDI) or transmit (MDIX) signal (+ differential)
G2	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (- differential)
G1	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
G3	ISET	O	Set physical transmit output current. Pull-down this ball with a 3.01K 1% resistor.
H1	X1	I	25MHz crystal/oscillator clock connections
H2	X2	O	Balls (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is ± 50ppm for both crystal and oscillator.
J1	RSTN	Ipu	Hardware Reset, Active Low RSTN will cause the KSZ8842-PMBL to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 ms.
J2	PAR	O	PCI Parity Even parity computed for PAD [31:0] and CBE[3:0]N, master drives PAR for address and write data phase, target drives PAR for read data phase.
K1	FRAMEN	I/O	PCI Cycle Frame This signal is asserted low to indicate the beginning of the address phase of the bus transaction and de-asserted before the final transfer of the data phase of the transaction in a bus master mode. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.

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Ball Number	Ball Name	Type	Ball Function
K2	IRDYN	I/O	PCI Initiator Ready As a bus master, this signal is asserted low to indicate valid data phases on PAD [31:0] during write data phases, indicates it is ready to accept data during read data phases. As a target, it'll monitor this IRDYN signal that indicates the master has put the data on the bus.
H3	TRDYN	I/O	PCI Target Ready As a bus target, this signal is asserted low to indicate valid data phases on PAD [31:0] during read data phases, indicating it is ready to accept data during write data phases. As a master, it will monitor this TRDYN signal that indicates the target is ready for data during read/write operation.
J3	STOPN	I/O	PCI Stop This signal is asserted low by the target device to stop the current transaction
K3	IDSEL	I/O	PCI Initialization Device Select. This signal is used to select the KSZ8842-PMQL/PMBL during configuration read and write transactions.
H4	DEVSELN	I/O	PCI Device Select This signal is asserted low when it is selected as a target during a bus transaction. As a bus master, the KSZ8842-PMBL samples this signal to insure that the destination address for the data transfer is recognized by a PCI target.
J4	REQN	O	PCI Request The KSZ8842-PMBL will assert this signal low to request PCI bus master operation.
K4	GNTN	I	PCI Grant This signal is asserted low to indicate to the KSZ8842-PMBL that it has been granted the PCI bus master operation.
H5	PERRN	I/O	PCI Parity Error The KSZ8842-PMBL as a master or target will assert this signal low to indicate a parity error on any incoming data. As a bus master, it will monitor this signal on all write operations.
J5	SERRN	O	PCI System Error This system error signal is asserted low by the KSZ8842-PMBL.This signal is used to report address parity errors.
K5	CBE3N	I	Command and Byte Enable These signals are multiplexed on the same PCI pins. During the address phase, these lines define the bus command. During the data phase, these lines are used as Byte Enables. The Byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
K6	CBE2N	I	
J6	CBE1N	I	
H6	CBE0N	I	
K7	PAD31	I/O	PCI Address / Data 31 Address and data are multiplexed on the all of the PAD balls. The PAD pins carry the physical address during the first clock cycle of a transaction, and carry data during the subsequent clock cycles.
J7	PAD30	I/O	PCI Address / Data 30
H7	PAD29	I/O	PCI Address / Data 29
K8	PAD28	I/O	PCI Address / Data 28
J8	PAD27	I/O	PCI Address / Data 27
H8	PAD26	I/O	PCI Address / Data 26
K9	PAD25	I/O	PCI Address / Data 25
J9	PAD24	I/O	PCI Address / Data 24
K10	PAD23	I/O	PCI Address / Data 23

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Ball Number	Ball Name	Type	Ball Function
J10	PAD22	I/O	PCI Address / Data 22
H9	PAD21	I/O	PCI Address / Data 21
H10	PAD20	I/O	PCI Address / Data 20
G8	PAD19	I/O	PCI Address / Data 19
G9	PAD18	I/O	PCI Address / Data 18
G10	PAD17	I/O	PCI Address / Data 17
F8	PAD16	I/O	PCI Address / Data 16
F9	PAD15	I/O	PCI Address / Data 15
F10	PAD14	I/O	PCI Address / Data 14
E8	PAD13	I/O	PCI Address / Data 13
E9	PAD12	I/O	PCI Address / Data 12
E10	PAD11	I/O	PCI Address / Data 11
D10	PAD10	I/O	PCI Address / Data 10
D9	PAD9	I/O	PCI Address / Data 9
D8	PAD8	I/O	PCI Address / Data 8
C10	PAD7	I/O	PCI Address / Data 7
C9	PAD6	I/O	PCI Address / Data 6
C8	PAD5	I/O	PCI Address / Data 5
B10	PAD4	I/O	PCI Address / Data 4
B9	PAD3	I/O	PCI Address / Data 3
B8	PAD2	I/O	PCI Address / Data 2
A10	PAD1	I/O	PCI Address / Data 1
A9	PAD0	I/O	PCI Address / Data 0
C5	VDDC	P	1.2V digital core V_{DD}
C4	VDDCO	P	1.2V Core Voltage Output. (internal 1.2V LDO power supply output) This ball is used to provide 1.2V power supply to all 1.2V power VDDC and VDDA. It is recommended the ball should be connected to 3.3V power rail by a 100ohm resistor for the internal LDO application.
D3, E3, F3	VDDA	P	1.2V analog V_{DD}
D7, E7, F7, G4, G5, G6, G7	VDDIO	P	3.3V digital I/O V_{DD}
E1	VDDATX	P	3.3V analog V_{DD}
E2	VDDARX	P	3.3V analog V_{DD}
D4, D5, D6, E4, E5, E6, F4, F5, F6	GND	Gnd	Ground

Table 2. KSZ8842-PMBL Ball Description

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Functional Description

The KSZ8842-PMQL/PMBL contains one PCI interface unit, two 10/100 physical layer transceivers (PHYs), three MAC units, and a RX/TX DMA channel all integrated with a Layer-2 switch.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption.

Functional Overview: PCI Bus Interface Unit

PCI Bus Interface

The PCI Bus Interface implements PCI v2.2 bus protocols and configuration space. The KSZ8842-PMQL/PMBL supports bus master reads and writes to CPU memory, and CPU access to on-chip register space. When the CPU reads and writes the configuration registers of the KSZ8842-PMQL/PMBL, it is as a slave. So the KSZ8842-PMQL/PMBL can be either a PCI bus master or slave. The PCI Bus Interface is also responsible for managing the DMA interfaces and the host processors access. Arbitration logic within the PCI Bus Interface unit accepts bus requests from the TXDMA logic and RXDMA logic.

The PCI bus interface also manages interrupt generation for a host processor.

TXDMA Logic and TX Buffer Manager

The KSZ8842-PMQL/PMBL supports a multi-frame, multi-fragment DMA gather process. Descriptors representing frames are built and linked in system memory by a host processor. The TXDMA logic is responsible for transferring the multi-fragment frame data from the host memory into the TX buffer.

The KSZ8842-PMQL/PMBL uses 4K bytes of transmit data buffer between the TXDMA logic and transmit MAC. When the TXDMA logic determines there is enough space available in the TX buffer, the TXDMA logic will move any pending frame data into the TX buffer. The management mechanism depends on the transmit descriptor list.

RXDMA Logic and RX Buffer Manager

The KSZ8842-PMQL/PMBL supports a multi-frame, multi-fragment DMA scatter process. Descriptors representing frames are built and linked in system memory by the host processor. The RXDMA logic is responsible for transferring the frame data from the RX buffer to the host memory.

The KSZ8842-PMQL/PMBL uses 4K bytes of receive data buffer between the receive MAC and RXDMA logic. The management mechanism depends on the receive descriptor list.

Functional Overview: Physical Layer Transceiver (PHY)

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external1% 3.01KΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial to parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for

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optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer (Recovery)

The internal PLL clock synthesizer generates 125MHz, 62.5MHz, 41.66MHz, and 25MHz clocks by setting the on-chip bus speed control register OBCR for KSZ8842-PMQL/PMBL system timing. These internal clocks are generated from an external 25MHz crystal or oscillator.

Note: Default setting is 25MHz in OBCR register, recommends the software driver to set it to 125MHz for best performance.

Scrambler/De-scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8842-PMQL/PMBL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

The KSZ8842-PMQL/PMBL features a per port power-down mode. To save power, the user can power-down a port that is not in use by setting bit 11 in either P1CR4 or P1MBCR register for port 1, and set bit 11 in either P2CR4 or P2MBCR register for port 2. To bring the port back up, reset bit 11 in these registers.

In addition, there is a full switch power-down mode by PWRDN pin/ball 36. When this pin/ball is pulled-down, the entire chip powers down. Transitioning this pin/ball from pull-down to pull-up results in a power up and chip reset.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8842-PMQL/PMBL supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8842-PMQL/PMBL device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

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The IEEE 802.3u standard MDI and MDI-X definitions are:

MDI		MDI-X	
RJ45 Pins	**Signals**	**RJ45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 3. MDI/MDI-X Pin Definitions

Straight Cable

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. The following diagram shows a typical straight cable connection between a network interface card (NIC) (MDI) and a switch, or hub (MDI-X).

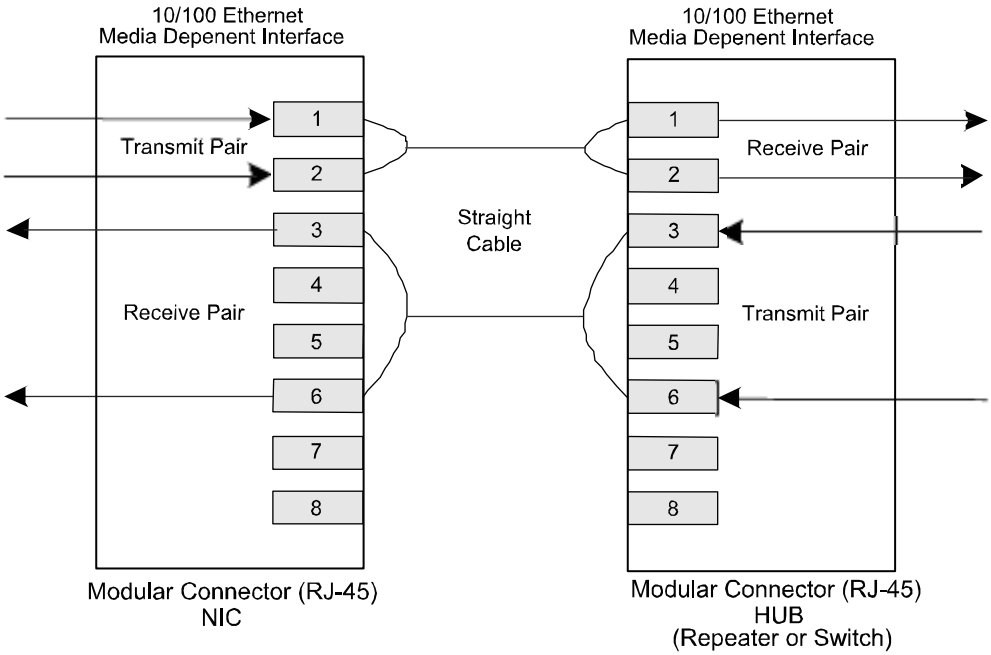

Figure 4. Typical Straight Cable Connection

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Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

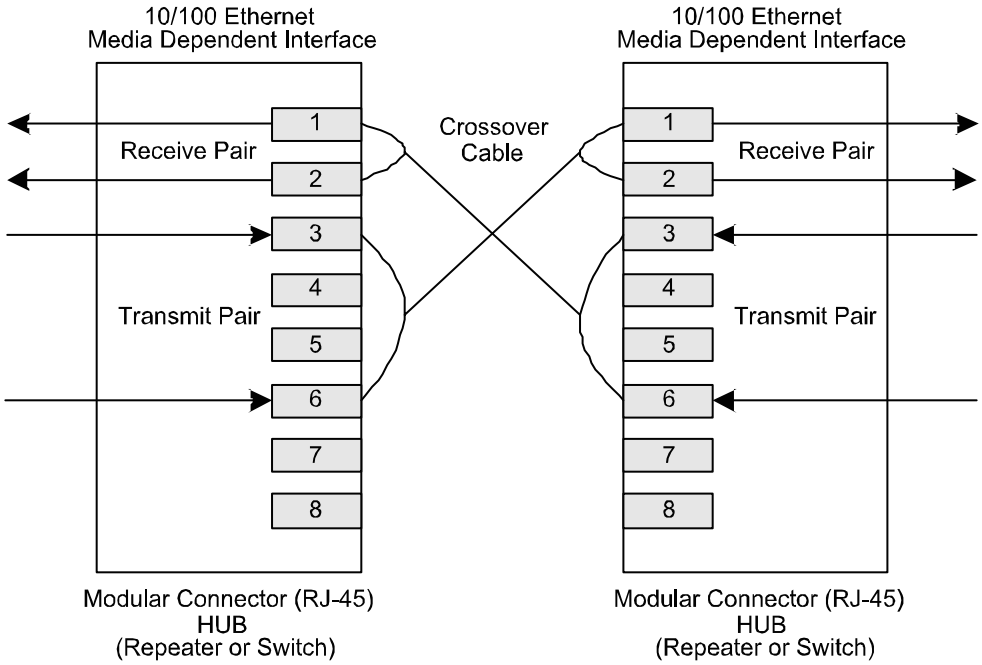

Figure 5. Typical Crossover Cable Connection

Auto Negotiation

The KSZ8842-PMQL/PMBL conforms to the auto negotiation protocol as described by the 802.3 committee to allow the channel to operate at 10Base-T or 100Base-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8842-PMQL/PMBL is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup is shown in the following flow diagram (Figure 6).

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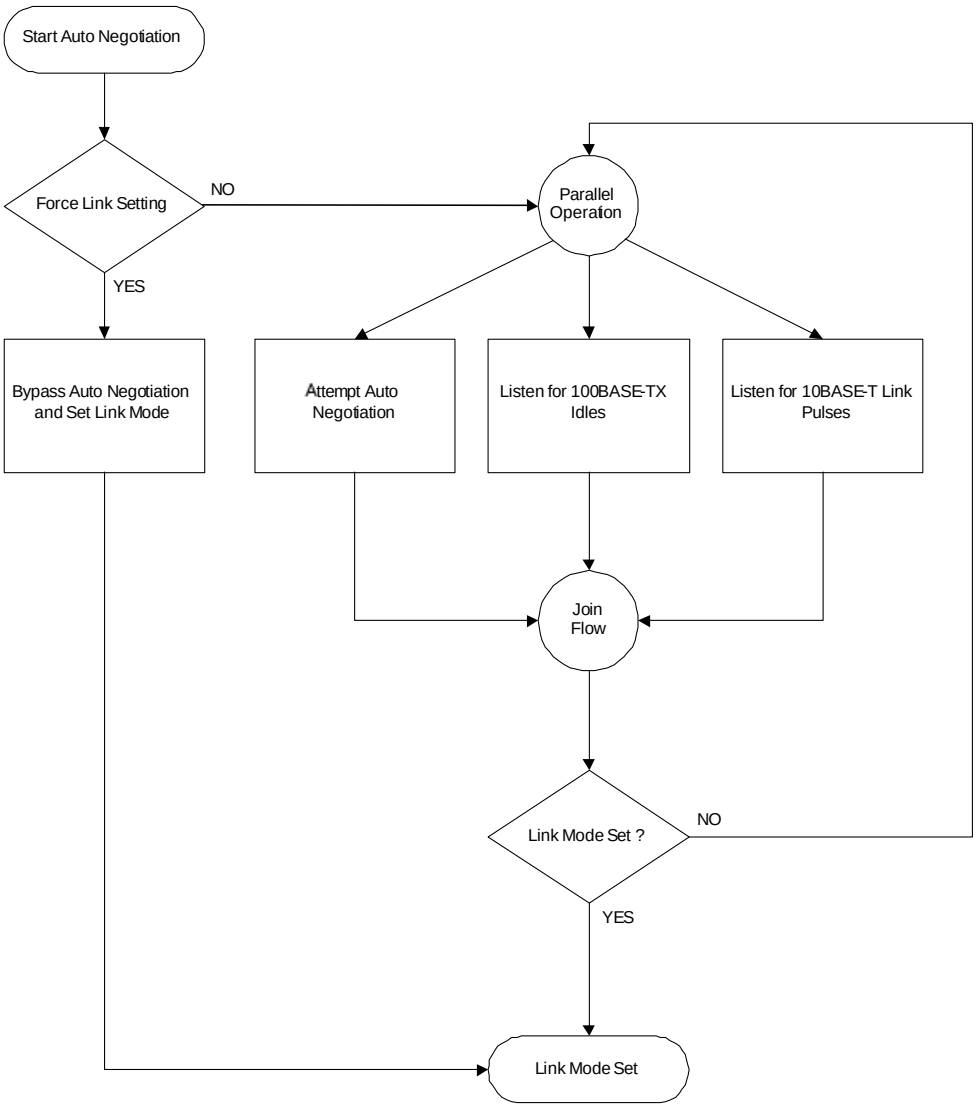

Figure 6. Auto Negotiation and Parallel Operation

LinkMD Cable Diagnostics

The KSZ8842-PMQL/PMBL LinkMD uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Access

LinkMD is initiated by accessing register P1VCT/P2VCT, the LinkMD Control/Status register, in conjunction with register P1CR4/P2CR4, the 100BASE-TX PHY Controller register.

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Usage

LinkMD can be used at any time by making sure Auto MDIX has been disabled. To disable Auto-MDIX, write a '1' to P1CR4[10] for port 1 or P2CR4[10] for port 2 to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1VCT[15] for port 1 or P2VCT[15] for port 2, is set to '1' to start the test on this pair.

When bit P1VCT[15] or P2VCT[15] returns to '0', the test is complete. The test result is returned in bit P1VCT[14-13] or P2VCT[14-13] and the distance is returned in bits P1VCT[8-0] or P2VCT[8-0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

IIf P1VCT[14-13]=11 or P2VCT[14-13]=11, this indicates an invalid test, and occurs when the KSZ8842-PMQL/PMBL is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8842-PMQL/PMBL to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance (in meters) can be approximated by the following formula:

Distance = P1VCT[8-0] x 0.4m

Distance = P1VCT[8-0] x 0.4m

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

Functional Overview: MAC and Switch

Address Lookup

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information.

The KSZ8842-PMQL/PMBL is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal lookup engine updates its table with a new entry if the following conditions are met:

1. The received packet's Source Address (SA) does not exist in the lookup table.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

Migration

The internal lookup engine also monitors whether a station has moved. If a station has moved, it updates the table accordingly. Migration happens when the following conditions are met:

1. The received packet's SA is in the table but the associated source port information is different.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine updates the existing record in the table with the new source port information.

Aging

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and continuously removes aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through Global Register SGCR1[10]).

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Forwarding

The KSZ8842-PMQL/PMBL forwards packets using the algorithm that is depicted in the following flowcharts. Figure 7 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 8. The packet is sent to PTF2.

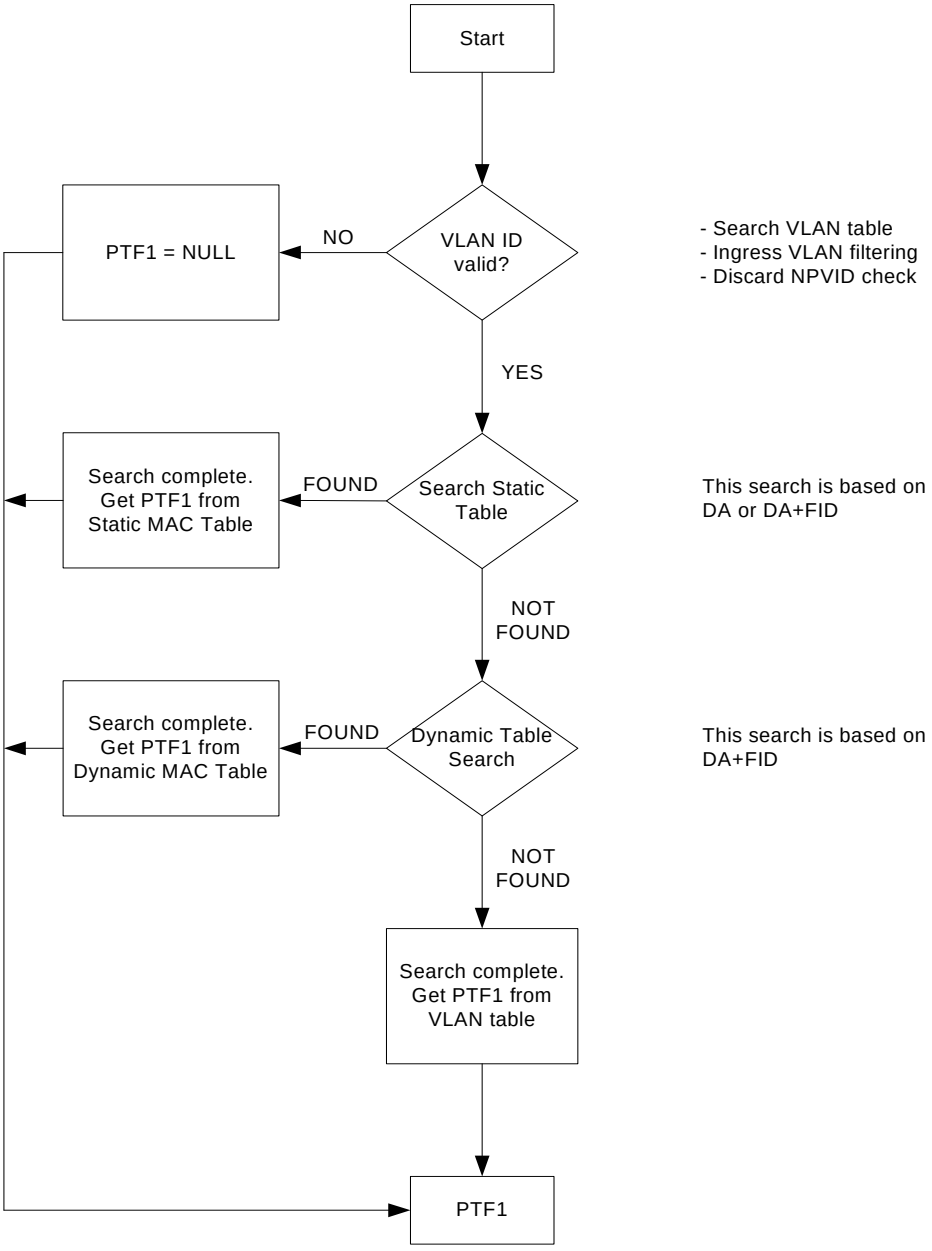

Figure 7. Destination Address Lookup Flow Chart, Stage 1

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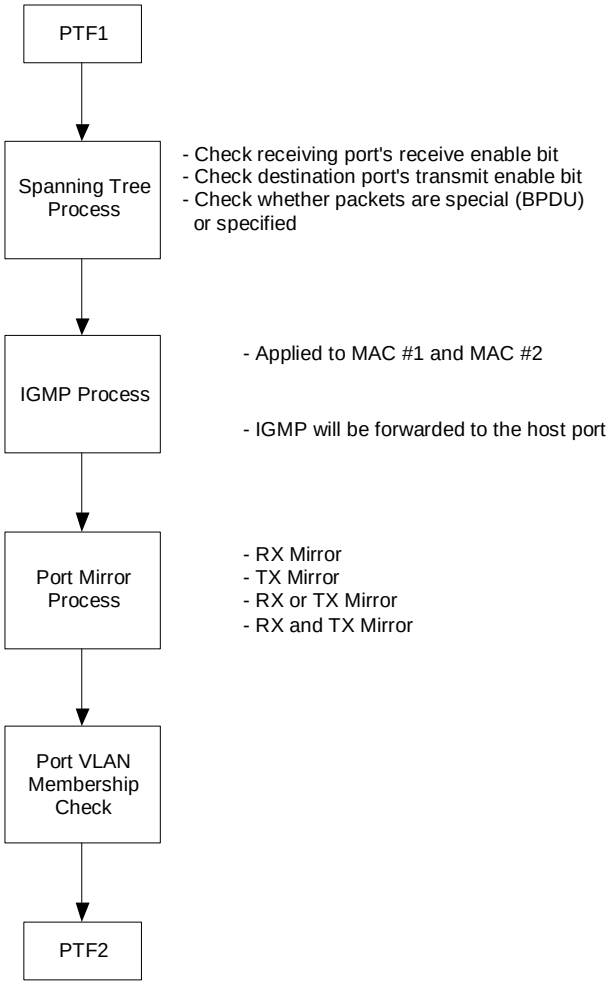

Figure 8. Destination Address Resolution Flow Chart, Stage 2

The KSZ8842-PMQL/PMBL will not forward the following packets:

1. Error packets.
   These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.
2. 802.3x pause frames.
   The KSZ8842-PMQL/PMBL intercepts these packets and performs flow control.
3. "Local" packets.
   Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as "local."

Switching Engine

The KSZ8842-PMQL/PMBL features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The switching engine has a 32KB internal frame buffer. This resource is shared between all the ports. There are a total of 256 buffers available. Each buffer is sized at 128B.

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MAC Operation

The KSZ8842-PMQL/PMBL strictly abides by IEEE 802.3 standards to maximize compatibility. Additionally, there is an added MAC filtering function to filter unicast packets. The MAC filtering function is useful in applications such as VoIP where restricting certain packets reduces congestion and thus improves performance.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the minimum 96-bits time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bits time for IPG is measured from Carrier Sense (CSR) to the next transmit packet.

Back-Off Algorithm

The KSZ8842-PMQL/PMBL implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode, and optional "aggressive mode" back-off. After 16 collisions, the packet is optionally dropped depending on the switch configuration in SGCR1[8].

Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

Illegal Packet Size

The KSZ8842-PMQL/PMBL discards packets that are less than 64 bytes in size and can be programmed to accept packet sizes up to 1536 bytes in SGCR2[1]. The KSZ8842-PMQL/PMBL can also be programmed for special applications to accept packet sizes up to 1916 bytes in SGCR2[2].

Flow Control

The KSZ8842-PMQL/PMBL supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8842-PMQL/PMBL receives a pause control frame, the KSZ8842-PMQL/PMBL will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8842-PMQL/PMBL are transmitted.

On the transmit side, the KSZ8842-PMQL/PMBL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues, and available receive queues.

The KSZ8842-PMQL/PMBL will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8842-PMQL/PMBL issues a flow control frame (XON), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8842-PMQL/PMBL sends out the other flow control frame (XOFF) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

Half-Duplex Backpressure

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same in full-duplex mode. If backpressure is required, the KSZ8842-PMQL/PMBL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8842-PMQL/PMBL discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10 BASE-T or 100 BASE-TX half-duplex modes, the user must enable the following:

1. Aggressive back off (bit 8 in SGCR1)
2. No excessive collision drop (bit 3 in SGCR2)

Note: These bits are not set by default, since this is not the IEEE standard.

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Broadcast Storm Protection

The KSZ8842-PMQL/PMBL has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8842-PMQL/PMBL has the option to include "multicast packets" for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis in P1CR1[7] and P2CR1[7]. The rate is based on a 67ms interval for 100Base-T and a 670ms interval for 10Base-T. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in SGCR3[15:18]. The default setting is 0x63 (99 decimal). This is equal to a rate of 1% minimum size packets, calculated as follows:

148,800 frames/sec X 67 ms/interval X 1% = 99 frames/interval (approx.) = 0x63

Where 148,800 frames/sec is based on 64-byte blocks of 100Base-T packets with 12 bytes of IPG and 8 bytes of preamble between packets.

Repeater Mode

When KSZ8842-PMQL/PMBL is set to repeater mode (SGCR3[7] = 1), it only works on 100BT half-duplex mode. In repeater enabled mode, all ingress packets will broadcast to other two ports without MAC check and learning. Before setting the device to repeater mode, the user has to set bit 13 (100Mbps), bit 12 (auto-negotiation disabled) and bit 8 (half duplex) in both P1MBCR and P2MBCR registers as well as to set bit 6 (host half duplex) in SGCR3 register for repeater mode.

The latency in repeater mode is defined from the 1st bit of DA into the ingress port 1 to the 1st bit of DA out of the egress port 2. The minimum is 270 ns and the maximum is 310 ns (one clock skew of 25 MHz between TX and RX).

Clock Generator

The X1 and X2 pin/balls are connected to a 25MHz crystal. X1 can also serve as the connector to a 3.3V, 25MHz oscillator (as described in the pin/ball description). The PCI Bus Interface supports a maximum speed of 33MHz PCLK (PCI Bus Clock).

Advanced Switch Functions

Spanning Tree Support

To support spanning tree, the host port is the designated port for the processor.

The other ports can be configured in one of the five spanning tree states via "transmit enable", "receive enable" and "learning disable" register settings in registers P1CR2 and P2CR2 for ports 1 and 2, respectively. Table 4 shows the port setting and software actions taken for each of the five spanning tree states.

Disable State	**Port Setting**	**Software Action**
The port should not forward or receive any packets. Learning is disabled.	"transmit enable = 0, receive enable = 0, learning disable = 1"	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the "static MAC table" with "overriding bit" set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State	**Port Setting**	**Software Action**
Only packets to the processor are forwarded.	"transmit enable = 0, receive enable = 0, learning disable = 1"	The processor should not send any packets to the port(s) in this state. The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State	**Port Setting**	**Software Action**
Only packets to and from the processor are	"transmit enable = 0, receive enable = 0, learning disable = 1"	The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those

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forwarded. Learning is disabled.		specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is disabled on the port in this state.
Learning State	**Port Setting**	**Software Action**
Only packets to and from the processor are forwarded. Learning is enabled.	"transmit enable = 0, receive enable = 0, learning disable = 0"	The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is enabled on the port in this state.
Forwarding State	**Port Setting**	**Software Action**
Packets are forwarded and received normally. Learning is enabled.	"transmit enable = 1, receive enable = 1, learning disable = 0"	The processor programs the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. Address learning is enabled on the port in this state.

Table 4. KSZ8841-PMQL/PMBL EEPROM Format

IGMP Support

For Internet Group Management Protocol (IGMP) support in Layer 2, the KSZ8842-PMQL/PMBL provides two components:

"IGMP" Snooping

The KSZ8842-PMQL/PMBL traps IGMP packets and forwards them only to the processor (host port). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

"Multicast Address Insertion" in the Static MAC Table

Once the multicast address is programmed in the Static MAC Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

IPv6 MLD Snooping

The KSZ8842-PMQL/PMBL traps IPv6 Multicast Listener Discovery (MLD) packets and forwards them only to the processor (host port). MLD snooping is controlled by SGCR2[13] (MLD snooping enable) and SGCR2[12] (MLD option).

Setting SGCR2[13] causes the KSZ8842-PMQL/PMBL to trap packets that meet all of the following conditions:

- IPv6 multicast packets
- Hop count limit = 1
- IPv6 next header = 1 or 58 (or = 0 with hop-by-hop next header = 1 or 58)
- If SGCR2[12] =1, IPv6 next header = 43, 44, 50, 51, or 60 (or =0 with hop-by-hop next header = 43, 44, 50, 51, or 60)

Port Mirroring Support

KSZ8842-PMQL/PMBL supports "Port Mirroring" comprehensively as:

"receive only" mirror on a port

All the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "receive sniff" and the host port is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8842-PMQL/PMBL forwards the packet to both port 2 and the host port. The KSZ8842-PMQL/PMBL can optionally even forward "bad" received packets to the "sniffer port".

"transmit only" mirror on a port

All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be "transmit sniff" and the host port is programmed to be the "sniffer port". A packet received on port 2 is destined to port 1

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after the internal lookup. The KSZ8842-PMQL/PMBL forwards the packet to both port 1 and the host port.

“receive and transmit” mirror on two ports

All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the “AND” feature, set register SGCR2, bit 8 to “1”. For example, port 1 is programmed to be “receive sniff”, port 2 is programmed to be “transmit sniff”, and the host port is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8842-PMQL/PMBL forwards the packet to both port 2 and the host port.

Multiple ports can be selected as “receive sniff” or “transmit sniff”. In addition, any port can be selected as the “sniffer port”. All these per port features can be selected through registers P1CR2, P2CR2, and P3CR2 for ports 1, 2, and the host port, respectively.

IEEE 802.1Q VLAN Support

The KSZ8842-PMQL/PMBL supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8842-PMQL/PMBL provides a 16-entry VLAN table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning. (See Tables 12 and 13.)

DA found in Static MAC Table?	Use FID flag?	FID match?	DA+FID found in Dynamic MAC Table?	Action
No	Don’t care	Don’t care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
No	Don’t care	Don’t care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	0	Don’t care	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	1	Yes	Don’t care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]

Table 5. FID+DA Lookup in VLAN Mode

FID+SA found in Dynamic MAC Table?	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

Table 6. FID+SA Lookup in VLAN Mode

QoS Priority Support

The KSZ8842-PMQL/PMBL provides Quality of Service (QoS) for applications such as VoIP and video conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues: Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. Bit 0 of registers P1CR1, P2CR1, and P3CR1 is used to enable split transmit queues for ports 1, 2, and the host port, respectively.

Port-Based Priority

With port-based priority, each ingress port can be individually classified as a high-priority receiving port. All packets

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received at the high-priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bit 4 and 3 of registers P1CR1, P2CR1, and P3CR1 is used to enable port-based priority for ports 1, 2, and the host port, respectively.

802.1p-Based Priority

For 802.1p-based priority, the KSZ8842-PMQL/PMBL examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the “priority mapping” value, as specified by the register SGCR6. The “priority mapping” value is programmable.

Figure 9 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

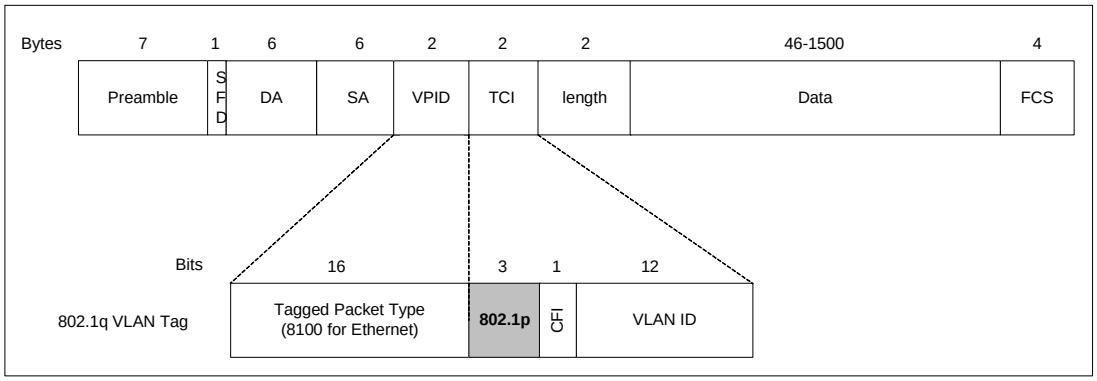

Figure 9. 802.1p Priority Field Format

802.1p based priority is enabled by bit 5 of registers P1CR1, P2CR1, and P3CR1 for ports 1, 2, and the host port, respectively.

The KSZ8842-PMQL/PMBL provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN protocol ID (VPID) and the 2 bytes tag control information field (TCI), is also referred to as the 802.1Q VLAN tag.

Tag insertion is enabled by bit 2 of registers P1CR1, P2CR1, and P3CR1 for ports 1, 2, and the host port, respectively. At the egress port, untagged packets are tagged with the ingress port’s default tag. The default tags are programmed in register sets P1VIDCR, P2VIDCR, AND P3VIDCR for ports 1, 2 and the host port, respectively. The KSZ8842-PMQL/PMBL does not add tags to already tagged packets.

Tag removal is enabled by bit 1 of registers P1CR1, P2CR1, and P3CR1 for ports 1, 2, and the host port, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8842-PMQL/PMBL will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

802.1p priority field re-mapping is a QoS feature that allows the KSZ8842-PMQL/PMBL to set the “User Priority Ceiling” at any ingress port. If the ingress packet’s priority field has a higher priority value than the default tag’s priority field of the ingress port, the packet’s priority field is replaced with the default tag’s priority field. The “User Priority Ceiling” is enabled by bit 3 of registers P1CR2, P2CR2, and P3CR2 for ports 1, 2, and the host port, respectively.

DiffServ based Priority

DiffServ-based priority uses the ToS registers shown in the Priority Control Registers section. The ToS priority control registers implement a fully decoded, 128-bit Differentiated Services Code Point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

Rate Limiting Support

The KSZ8842-PMQL/PMBL supports hardware rate limiting from 64 Kbps to 88 Mbps, independently on the “receive side” and on the “transmit side” on a per port basis. For 10Base-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up Ingress Rate Control Registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up Egress Rate Control Registers. The size of each frame has options to include minimum IFG (Inter Frame Gap) or Preamble byte, in addition to the data field (from packet DA to FCS).

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For ingress rate limiting, KSZ8842-PMQL/PMBL provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8842-PMQL/PMBL counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the Leaky Bucket algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-bursty egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

MAC Filtering Function

Use the static table to assign a dedicated MAC address to a specific port. When a unicast MAC address is not recorded in the static table, it is also not learned in the dynamic MAC table. The KSZ8842-PMQL/PMBL includes an option that can filter or forward unicast packets for an unknown MAC address. This option is enabled by SGCR7[7].

The unicast MAC address filtering function is useful in preventing the broadcast of unicast packets that could degrade the quality of this port in applications such as voice over Internet Protocol (VoIP).

Configuration Interface

The KSZ8842-PMQL/PMBL operates as a managed switch or a repeater, however it cannot be used as an unmanaged switch.

EEPROM Interface

The external serial EEPROM with a standard microwire bus interface is used for non-volatile storage of information such as the host MAC address and ID, (for example, 93C46 or 93C66 EEPROM devices.)

If the EEEN pin/ball is pulled high, the KSZ8842-PMQL/PMBL performs an automatic read of the external EEPROM words 0H to 6H after the de-assertion of Reset. The EEPROM values are placed in certain host-accessible registers. EEPROM read/write functions can also be performed by software read/writes to the EEPCR registers.

The KSZ8842-PMQL/PMBL EEPROM format is given below.

WORD	15 8	7 0
0H	Reserved	
1H	Host MAC Address Byte 2	Host MAC Address Byte 1
2H	Host MAC Address Byte 4	Host MAC Address Byte 3
3H	Host MAC Address Byte 6	Host MAC Address Byte 5
4H	Subsystem ID	
5H	Subsystem Vendor ID	
6H	Reserved	
7H-3FH	Not used by KSZ8842-PMQL/PMBL (available for user to use)	

Table 7. EEPROM Format

Loop back Support

The KSZ8842-PMQL/PMBL provides loop back support for remote diagnostic of failure. In loop back mode, the speed at both PHY ports will be set to 100BASE-TX full-duplex mode. Two types of loop back are supported: Far-end Loop back and Near-end (Remote) Loop back.

Far-end Loop back:

Far-end loop back is conducted between the KSZ8842-PMQL/PMBL's two PHY ports. The loop back path starts at the "Originating" PHY. The originating PHY port's receive inputs (RXP/RXM), wrap around at the "loop back" PHY port's PMD/PMA, and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

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Bit [8] of registers P1CR4 and P2CR4 is used to enable far-end loop back for ports 1 and 2, respectively. Alternatively, Bit [14] of registers P1MBCR and P2MBCR can also be used to enable far-end loop back. When register P2MBCR bit 14 =1 or P2CR4 bit 8 =1, the port 2 far-end loop back path is illustrated in the Figure 11.

Near-end (Remote) Loop back:

Near-end (Remote) loop back is conducted at either PHY port 1 or PHY port 2 of the KSZ8842-PMQL/PMBL. The loop back path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXPx/TXMx).

Bit [1] of registers P1PHYCTRL and P2PHYCTRL is used to enable near-end loop back for ports 1 and 2, respectively. Alternatively, Bit [9] of registers P1SCSLMD and P2SCSLMD can also be used to enable near-end loop back. Both ports 1 and 2 near-end loop back paths are illustrated in the following Figure 10.

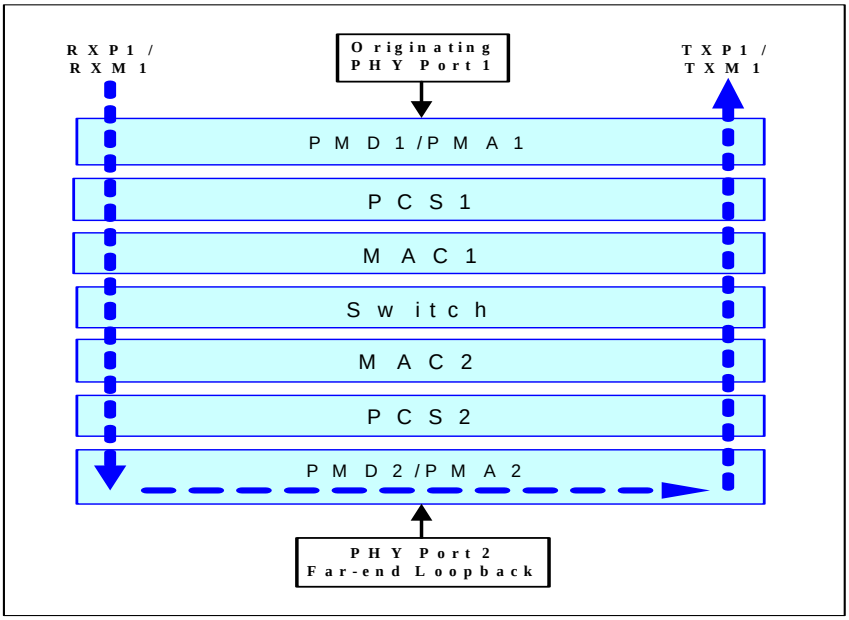

Figure 10. Port 2 Far-End Loop back Path

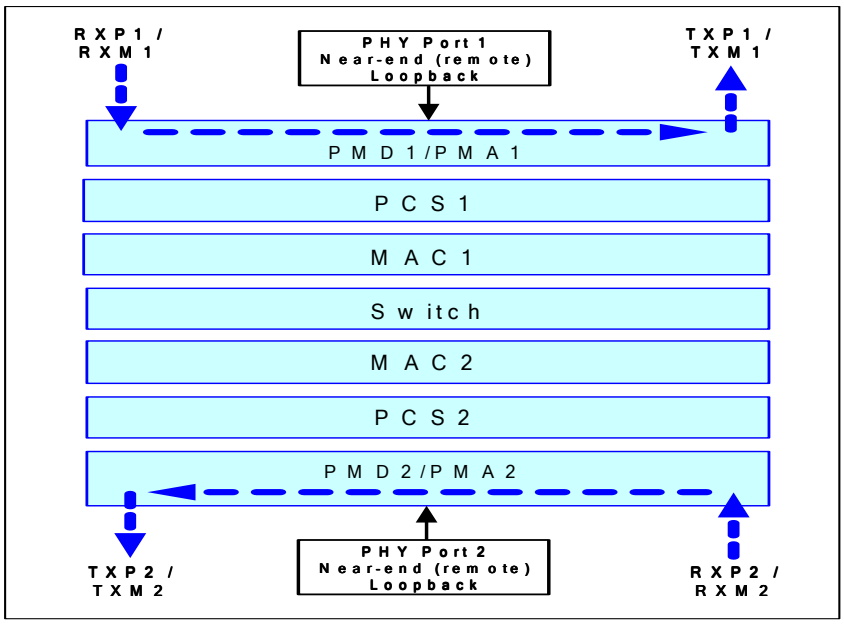

Figure 11. Port 1 and Port 2 Near-End (Remote) Loop back Path

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Host Communication

The descriptor lists and data buffers, collectively called the host communication, manage the actions and status related to RX and TX buffer management. Commands and signals that control the functional operation of the KSZ8842-PMQL/PMBL are also described.

The KSZ8842-PMQL/PMBL and the driver communicate through the two data structures: Command and status registers (CSRs), and Descriptor Lists and Data Buffers.
Note: All unused bits of the data structure in this section are reserved and should be written by the driver as zero.

Host Communication Descriptor Lists and Data Buffers

The KSZ8842-PMQL/PMBL transfers received data frames to the receive buffer in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists (one for receive and one for transmit) for MAC DMA. The base address of each list is written in the TDLB register and in the RDLB register, respectively. A descriptor list is forward linked. The last descriptor may point back to the first entry to create a ring structure. Descriptors are chained by setting the *next address* to the next buffer in both the receive and transmit descriptors.

The descriptor lists reside in the host *physical* memory address space. Each pointer points to one buffer and the second pointer points to the next descriptor. This enables the greatest flexibility for the host to chain any data buffers with discontinuous memory location. This eliminates processor-intensive tasks such as memory copying from the host to memory.

A data buffer contains either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; and buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host physical memory space.

Receive Descriptors (RDES0-RDES3)

Receive descriptor and buffer addresses must be Word aligned. Each receive descriptor provides one frame buffer, one byte count field, and control and status bits.

The following table shows the RDES0 register bit fields.

Bit	Description
31	***OWN Own Bit*** When set, indicates that the descriptor is owned by the KSZ8842-PMQL/PMBL. When reset, indicates that the descriptor is owned by the host. The KSZ8842-PMQL/PMBL clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	***FS First Descriptor*** When set, indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the next buffer contains the beginning of the frame.
29	***LS Last Descriptor*** When set, indicates that the buffer pointed by this descriptor is the last buffer of the frame.
28	***IPE IP Checksum Error*** When set, indicates that the received frame is an IP packet and its IP checksum field does not match. This bit is valid only when last descriptor is set.
27	***TCPE TCP Checksum Error*** When set, indicates that the received frame is a TCP/IP packet and its TCP checksum field does not match. This bit is valid only when last descriptor is set.
26	***UDPE UDP Checksum Error*** When set, indicates that the received frame is an UDP/IP packet and its UDP checksum field does not match. This bit is valid only when last descriptor is set.

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Bit	Description
25	***ES Error Summary*** Indicates the logical OR of the following RDES0 bits: CRC error Frame too long Runt frame This bit is valid only when last descriptor is set.
24	***MF Multicast Frame*** When set, indicates that this frame has a multicast address. This bit is valid only when last descriptor is set.
23 – 20	***SPN Switch Engine Source Port Number*** This field indicates the source port where the packet originated. If bit 20 is set, it indicates the packet was received from port 1. If bit 21 is set, it indicates the packet was received from port 2. This field is valid only when the last descriptor is set. (Bits 23 and 22 are not used, but reserved for backward compatibility and future expansion.)
19	***RE Report on MII Error*** When set, indicates that a receive error in the physical layer was reported during the frame reception.
18	***TL Frame Too Long*** When set, indicates that the frame length exceeds the maximum size of 1518 bytes. This bit is valid only when last descriptor is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.
17	***RF Runt Frame*** When set, indicates that this frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed on to the host only if the pass bad frame bit is set.
16	***CE CRC Error*** When set, indicates that a CRC error occurred on the received frame. This bit is valid only when last descriptor is set.
15	***FT Frame Type*** When set, indicates that the frame is an Ethernet-type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames. This bit is valid only when last descriptor is set.
14 – 11	Reserved
10 – 0	***FL Frame Length*** Indicates the length, in bytes, of the received frame, including the CRC. This field is valid only when last descriptor is set and descriptor error is reset.

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The following table shows the RDES1 register bit fields.

Bit	Description
31 – 26	Reserved
25	***RER Receive End of Ring*** When set, indicates that the descriptor list reached its final descriptor. The KSZ8842-PMQL/PMBL returns to the base address of the list, thus creating a descriptor ring.
24 – 11	Reserved
10 – 0	***RBS Receive Buffer Size*** Indicates the size, in bytes, of the receive data buffer. If the field is 0, the KSZ8842-PMQL/PMBL ignores this buffer and moves to the next descriptor. The buffer size must be a multiple of 4.

The following table shows the RDES2 register bit fields.

Bit	Description
31 – 0	***Buffer Address*** Indicates the physical memory address of the buffer. The buffer address must be Word aligned.

The following table shows the RDES3 register bit fields.

Bit	Description
31 – 0	***Next Descriptor Address*** Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.

Transmit Descriptors (TDES0-TDES3)

Transmit descriptors must be Word aligned. Each descriptor provides one frame buffer, one byte count field, and control and status bits.

The following table shows the TDES0 register bit fields.

Bit	Description
31	***OWN Own Bit*** When set, indicates that the descriptor is owned by the KSZ8842-PMQL/PMBL. When cleared, indicates that the descriptor is owned by the host. The KSZ8842-PMQL/PMBL clears this bit either when it completes the frame transmission or when the buffer allocated in the descriptor is empty. The ownership bit of the first descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between the KSZ8842-PMQL/PMBL fetching a descriptor and the driver setting an ownership bit.
30 – 0	Reserved

The following table shows the TDES1 register bit fields.

Bit	Description
31	***IC Interrupt on Completion*** When set, the KSZ8842-PMQL/PMBL sets transmit interrupt after the present frame has been transmitted. It is valid only when last segment is set.
30	***FS First Segment*** When set, indicates that the buffer contains the first segment of a frame.
29	***LS Last Segment*** When set, indicates that the buffer contains the last segment of a frame.

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Bit	Description
28	***IPCKG IP Checksum Generate*** When set, the KSZ8842-PMQL/PMBL will generate correct IP checksum for outgoing frames that contains IP protocol header. The KSZ8842-PMQL/PMBL supports only a standard IP header, i.e., IP with a 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the IP checksum generate bit in the transmit mode register is not set. This bit should be always set for multiple-segment packets.
27	***TCPCKG TCP Checksum Generate*** When set, the KSZ8842-PMQL/PMBL will generate correct TCP checksum for outgoing frames that contains IP and TCP protocol header. The KSZ8842-PMQL/PMBL supports only a standard IP header, i.e., IP with a 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the TCP checksum generate bit in the transmit mode register is not set. This bit should be always set for multiple-segment packets.
26	***UDPCKG UDP Checksum Generate*** When set, the KSZ8842-PMQL/PMBL will generate correct UDP checksum for outgoing frames that contains a IP and UDP protocol header. The KSZ8842-PMQL/PMBL supports only a standard IP header, i.e., IP with a 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the UDP checksum generate bit in the transmit mode register is not set.
25	***TER Transmit End of Ring*** When set, indicates that the descriptor pointer has reached its final descriptor. The KSZ8842-PMQL/PMBL returns to the base address of the list, forming a descriptor ring.
24	Reserved
23 – 20	***SPN Switch Engine Destination Port Map*** When set, this field indicates the destination port(s) where the packet will be forwarded to. If bit 20 is set, it indicates the packet was received from port 1. If bit 21 is set, it indicates the packet was received from port 2. Setting all ports to 1 will cause the switch engine to broadcast the packet. Setting all bits to 0 has no effect. The switch engine forwards the packet according to its internal switch lookup algorithm. This field is valid only when the last descriptor is set. (Bits 23 and 22 are not used, but reserved for backward compatibility and future expansion.)
19 – 11	Reserved
10 – 0	***TBS Transmit Buffer Size*** Indicates the size, in bytes, of the transmit data buffer. If this field is 0, the KSZ8842-PMQL/PMBL ignores this buffer and moves to the next descriptor.

The following table shows the TDES2 register bit fields.

Bit	Description
31 - 0	***Buffer Address*** Indicates the physical memory address of the buffer. There is no limitation on the transmit buffer address alignment.

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The following table shows the TDES3 register bit fields.

Bit	Description
31 - 0	***Next Descriptor Address*** Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.

PCI Configuration Registers

The KSZ8842-PMQL/PMBL implements 12 configuration registers. These registers are described in the following subsections.

The KSZ8842-PMQL/PMBL enables a full software-driven initialization and configuration. This allows the software to identify and query the KSZ8842-PMQL/PMBL. The KSZ8842-PMQL/PMBL treats configuration space write operations to registers that are reserved as no-ops. That is, the access completes normally on the bus and the data is discarded. Read accesses, to reserved or unimplemented registers, complete normally and a data value of 0 is returned.

Software reset has no effect on the configuration registers. Hardware reset sets the configuration registers to their default values.

Configuration Register	Identifier	I/O Address Offset	Default
Identification	CFID	00H	0x884116C6
Command and Status	CFCS	04H	0x02000000
Revision	CFRV	08H	0x02000010
Latency Timer	CFLT	0CH	0x00000000
Base Memory Address	CBMA	10H	0x00000000
Reserved	–	14H-28H	0x00000000
Subsystem ID	CSID	2CH	0x********
Reserved	–	38H	0x00000000
Interrupt	CFIT	3CH	0x28140100
Reserved	–	40H-4CH	0x00000000

Configuration ID Register (CFID Offset 00H)

The CFID register identifies the KSZ8842-PMQL/PMBL. The following table shows the CFID register bit fields.

Bit	Default	Description
31 - 16	0x8842	Device ID
15 - 0	0x16C6	***Vendor ID*** Specifies the manufacturer of the KSZ8842-PMQL/PMBL.

The following table shows the access rules of the register.

Category	Description
Value after hardware reset	0x884216C6
Write access rules	Write has no effect on the KSZ8842-PMQL/PMBL.

Command and Status Configuration Register (CFCS Offset 04H)

The CFCS register is divided into two sections: a command register (CFCS[15:0]) and a status register (CFCS[31:16]). The command register provides control of the KSZ8842-PMQL/PMBL's ability to generate and respond to PCI cycles. When 0 is written to this register, the KSZ8842-PMQL/PMBL logically disconnects from the PCI bus for all accesses except configuration accesses.

The status register records status information for the PCI bus-related events. The CFCS status bits are not cleared when they are read. Writing 1 to these bits clears them; writing 0 has no effect.

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The following table describes the CFCS register bit fields.

Bit	Type	Default	Description
31	Status	0	***Detected Parity Error*** When set, indicates that the KSZ8842-PMQL/PMBL detected a parity error, even if parity error handling is disabled in parity error response (CFCS[6]).
30	Status	0	***Signal System Error*** When set, indicates that the KSZ8842-PMQL/PMBL asserted the system error SERR_N pin/ball.
29	Status	0	***Received Master Abort*** When set, indicates that the KSZ8842-PMQL/PMBL terminated a master transaction with master abort.
28	Status	0	***Received Target Abort*** When set, indicates that the KSZ8842-PMQL/PMBL master transaction was terminated due to a target abort.
27	Status	0	***Target Abort*** This bit is set by KSZ8842-PMQL/PMBL whenever it terminates with a Target Abort. The CSR registers are all 32-bit Little Endian format. For PCI register Read cycles, the KSZ8842-PMQL/PMBL allows any different combination of CBEN. For PCI register bus cycles, only byte, word (16-bit), or Dword (32-bit) accesses are allowed. Any other combination is illegal and is target aborted.
26 – 25	Status	01	***Device Select Timing*** Indicates the timing of the assertion of device select(DEVSEL_N). These bits are fixed at 01, which indicates a middle assertion of DEVSEL_N.
24	Status	0	***Data Parity Report*** This bit is set when the following conditions are met: The KSZ8842-PMQL/PMBL asserts parity error PERR_N or it senses the assertion of PERR_N by another device. The KSZ8842-PMQL/PMBL operates as a bus master for the operation that caused the error. Parity error response (CFCS[6]) is set.
23 – 22	Reserved	00	Reserved
21	Status	0	66MHz Capable 0 = Not 66MHz capable
20 – 9	Reserved	0x000	Reserved
8	Command	0	***System Error Enable*** When set, the KSZ8842-PMQL/PMBL asserts system error (SERR_N) when it detects a parity error on the address phase.
7	Reserved	0	Reserved
6	Command	0	***Parity Error Response*** When set, the KSZ8842-PMQL/PMBL asserts fatal bus error after it detects a parity error. When reset, any detected parity error is ignored and the KSZ8842-PMQL/PMBL continues normal operation. Parity checking is disabled after hardware reset.
5 – 3	Reserved	000	Reserved

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Bit	Type	Default	Description
2	Command	0	***Master Operation*** When set, the KSZ8842-PMQL/PMBL is capable of acting as a bus master. When reset, the KSZ8842-PMQL/PMBL capability to generate PCI accesses is disabled. For normal operation, this bit must be set.
1	Command	0	***Memory Space Access*** When set, the KSZ8842-PMQL/PMBL responds to memory space accesses. When reset, the KSZ8842-PMQL/PMBL does not respond to memory space accesses.
0	Reserved	0	Reserved

Configuration Revision Register (CFRV Offset 08H)

The CFRV register contains the KSZ8842-PMQL/PMBL revision number. The following table shows the CFRV register bit fields.

Bit	Default	Description
31 – 24	0x02	***Base Class*** Indicates the network controller, and is equal to 2H.
23 – 16	0x00	***Subclass*** Indicates the Fast/Gigabit Ethernet chip, and is equal to 00H.
15 – 8	0x00	Reserved
7 – 4	0x1	***Revision Number*** Indicates the KSZ8842-PMQL/PMBL revision number, and is equal to 1H. This number is incremented for subsequent revision.
3 – 0	0x0	***Step Number*** Indicates the KSZ8842-PMQL/PMBL step number, and is equal to 0H (chip revision A). This number is incremented for subsequent KSZ8842-PMQL/PMBL steps within the current revision.

Configuration Latency Timer Register (CFLT Offset 0CH)

This register configures the cache line size field and the latency timer.

The following table shows the CFLT register bit fields.

Bit	Default	Description
31 – 16	0x00	Reserved
15 – 8	0x00	***Configuration Latency Timer*** Specifies, in units of PCI bus clocks, the value of the latency timer of the KSZ8842-PMQL/PMBL. When the KSZ8842-PMQL/PMBL asserts FRAME_N, it enables its latency timer to count. If the KSZ8842-PMQL/PMBL deasserts FRAME_N prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the KSZ8842-PMQL/PMBL initiates transaction termination as soon as its GNT_N is deasserted.
7 – 0	0x00	***Cache Line Size*** Specifies, in unit of 32-bit words (Dword), the system cache line size.

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Configuration Base Memory Address Register (CBMA Offset 10H)

The CBMA register specifies the base memory address for accessing the KSZ8842-PMQL/PMBL CSRs. This register must be initialized prior to accessing any CSR with memory access.

The following table shows the CBMA register bit fields.

Bit	Default	Description
31 - 11	0	***Configuration Base Memory Address*** Defines the base address assigned for mapping the KSZ8841-PMQL/PMBL CSRs.
10 - 1	0	This field value is 0 when read.
0	0	***Memory Space Indicator*** Determines that the register maps into the Memory space. The value in this field is 0. This is a read-only field.

Subsystem ID Register (CSID Offset 2CH)

The CSID register is a read-only 32-bit register. The content of the CSID is loaded from the EEPROM after a hardware reset. The loading period lasts at least 27,400 PCI cycles when the system is in 33MHz mode, and starts 50 cycles after hardware reset deassertion. If the host accesses the CSID before its content is loaded from the EEPROM, the KSZ8842-PMQL/PMBL responds with retry termination on the PCI bus.

The following table shows the CSID register bit fields.

Bit	Description
31 – 16	***Subsystem ID*** Indicates a 16-bit field containing the subsystem ID.
15 – 0	***Subsystem Vendor ID*** Indicates a 16-bit field containing the subsystem vendor ID.

The following table shows the access rules of the register.

Category	Description
Value after hardware reset	Read from EEPROM.
Write access rules	Write has no effect on the KSZ8842-PMQL/PMBL.

Configuration Interrupt Register (CFIT Offset 3CH)

The CFIT register is divided into two sections: the interrupt line and the interrupt pin/ball. CFIT configures both the system's interrupt and the KSZ8842-PMQL/PMBL interrupt pin/ball connection.

The following table shows the CFIT register bit fields.

Bit	Default	Description
31 – 24	0x28	***MAX_LAT*** This field indicates how often the device needs to gain access to the PCI bus. Time unit is equal to 0.25µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 28H (10µs).
23 – 16	0x14	***MIN_GNT*** This field indicates the burst period length that the device needs. Time unit is equal to 0.25µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 14H (5µs).
15 – 8	0x01	***Interrupt Pin/ball*** Indicates which interrupt pin/ball that the KSZ8842-PMQL/PMBL uses. The KSZ8842-PMQL/PMBL uses INTA# and the read value is 1H.

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Bit	Default	Description
7 – 0	0x00	***Interrupt Line*** Provides interrupt line routing information. The basic input/output system (BIOS) writes the routing information into to this field when it initialized and configures the system. The value in this field indicates which input of the system interrupt controller is connected to the KSZ8842-PMQL/PMBL's interrupt pin/ball. The driver uses this information to determine priority and vector information. Values in this field are system architecture specific.

The following table shows the access rules of the register.

Category	Description
Value after hardware reset	0x281401XX

PCI Control & Status Registers

The PCI CSR registers are all 32 bit in Little Endian format. For PCI register Read cycle, the KSZ8842-PMQL/PMBL allows any different combination of CBEN. For PCI register bus cycles, only byte, word (16-bit), or Dword (32-bit) accesses are allowed. Any other combinations are illegal, and will be target aborted.

MAC DMA Transmit Control Register (MDTXC Offset 0x0000)

The MAC DMA transmit control register establishes the transmit operating modes and commands for the port. This register should be one of the last CSRs to be written as part of the transmit initialization.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 30	-	RO	Reserved
29 – 24	0x00	RW	***MTBS DMA Transmit Burst Size*** This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the MAC DMA burst size is limited only by the amound of data stored in the transmit buffer before issuing a bus request. The MTBS can be programmed with the following permissible values: 0,1, 2, 4, 8, 16, or 32. After reset, the MTBS default is 0, i.e., unlimited.
23 – 19	0x00	RO	Reserved
18	0	RW	***MTUCG MAC Transmit UDP Checksum Generate*** When set, the KSZ8842-PMQL/PMBL will generate correct UDP checksum for outgoing UDP/IP frames at port. When this bit is set, ADD CRC should also turn on.
17	0	RW	***MTTCG MAC Transmit TCP Checksum Generate*** When set, the KSZ8842-PMQL/PMBL will generate correct TCP checksum for outgoing TCP/IP frames at port. When this bit is set, ADD CRC should also turn on.
16	0	RW	***MTICG MAC Transmit IP Checksum Generate*** When set, the KSZ8842-PMQL/PMBL will generate correct IP checksum for outgoing IP frames at port. When this bit is set, ADD CRC should also turn on.
15 – 10	0x00	RO	Reserved

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Bit	Default	R/W	Description
9	0	RW	***MTFCE MAC Transmit Flow Control Enable*** When this bit is set, flow control is enabled. This causes the KSZ8842-PMQL/PMBL to transmit a PAUSE frame from DMA to switch host MAC when the Receive Buffer has reached threshold and this bit is enabled. (SGCR3 bit 5 also needs to be enabled). Note: KSZ8842-PMQL/PMBL is full duplex only for RX/TX buffer.
8 – 3	0x0	RO	Reserved
2	0	RW	***MTEP MAC DMA Transmit Enable Padding*** When set, the KSZ8842-PMQL/PMBL automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit automatically enables Add CRC feature.
1	0	RW	***MTAC MAC DMA Transmit Add CRC*** When set, the KSZ8842-PMQL/PMBL appends the CRC to the end of the transmission frame.
0	0	RW	***MTE MAC DMA TX Enable*** When the bit is set, the MDMA TX block is enabled and placed in a running state. When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The stop transmission command is effective only when the transmission process is in the running state.

MAC DMA Receive Control Register (MDRXC Offset 0x0004)

The MAC DMA receive control register establishes the receive operating modes and commands for the port. This register should be one of the last CSRs to be written as part of the receive initialization.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 30	00	RO	Reserved
29 – 24	0x00	RW	***MRBS DMA Receive Burst Size*** This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the MAC DMA burst size is limited only by the amount of data stored in the receive buffer before issuing a bus request. The MRBS can be programmed with the following permissible values: 0,1, 2, 4, 8, 16, or 32. After reset, the MRBS default is 0, i.e., unlimited.
23 – 19	0x0	RO	Reserved
18	0	RW	***MRUCC MAC Receive UDP Checksum Check*** When set, the KSZ8842-PMQL/PMBL will check for correct UDP checksum for incoming UDP/IP frames at port. Packets received with incorrect UDP checksum will be discarded.
17	0	RW	***MRTCG MAC Receive TCP Checksum Check*** When set, the KSZ8842-PMQL/PMBL will check for correct TCP checksum for incoming TCP/IP frames at port. Packets received with incorrect TCP checksum will be discarded.
16	0	RW	***MRICG MAC Receive IP Checksum Check*** When set, the KSZ8842-PMQL/PMBL will check for correct IP checksum for incoming IP frames at port. Packets received with incorrect IP checksum will be discarded.

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9	0	RW	***MRFCE MAC Receive Flow Control Enable*** When set, flow control is enabled. The KSZ8842-PMQL/PMBL will acknowledge a PAUSE frame from the switch, the outgoing packets will be pending in the transmit buffer until the PAUSE control timer expires. When this bit is cleared, no flow control is enabled. Note: KSZ8842-PMQL/PMBL is full duplex only for RX/TX buffer.
8 – 7	00	RO	Reserved
6	0	RW	***MRB MAC Receive Broadcast*** When set, the MAC receive all broadcast frames.
5	0	RW	***MRM MAC Receive Multicast*** When set, the MAC receive all multicast frames (including broadcast).
4	0	RW	***MRU MAC Receive Unicast*** When set, the MRU MAC receive unicast frames that match the 16 48-bit MAC additional Station Address and the MAC address register if they are set by user.
3	0	RW	***MRE MAC DMA Receive Error Frame*** When set, the KSZ8842-PMQL/PMBL will pass the errors frames received to the host. Error frames include runt frames, oversized frames, CRC errors.
2	0	RW	***MRA MAC DMA Receive All*** When set, the KSZ8842-PMQL/PMBL will receive all incoming frames, regardless of its destination address.
1	0	RW	***DMA Receive Multicast Hash-Table Enable*** When set, the RX function to receive multicast frames that pass the CRC Hash filtering mechanism.
0	0	RW	***MRE MAC DMA RX Enable*** When set, the DMA RX block is enabled and placed in a running state. When reset, the receive process is placed in the stopped state after completing the reception of the current frame. The stop transmission command is effective only when the reception process is in the running state.

MAC DMA Transmit Start Command Register (MDTSC Offset 0x0008)

This register is written by the CPU when packets in the data buffer need to be transmitted.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 0	0x00000000	WO	***WTSC Transmit Start Command*** When written with any value, the Transmit DMA checks for frames to be transmitted. If no descriptor is available, the transmit process returns to suspended state. If descriptiors are available, the transmit process starts or resumes. This bit is self-clearing.

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MAC DMA Receive Start Command Register (MDRSC Offset 0x000C)

This register is written by the CPU when there are frame data in receive buffer to be processed.

The following table shows the register bit fields.

Bit	Default \	R/W	Description
31 – 0	0x00000000	WO	***WRSC Receive Start Command*** When written with any value, the Receive DMA checks for descriptors to be acquired. If no descriptor is available, the receive process returns to suspended state and waits for the next receive restart command. If descriptiors are available, the receive process resumes. This bit is self-clearing.

Transmit Descriptor List Base Address Register (TDLB Offset 0x0010)

This register is used for the Transmit Descriptor List Base Address. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KSZ8842-PMQL/PMBL behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 0	0x0	RW	***WSTL Start of Transmit List*** Note: Write can only occur when the transmit process stopped.

Receive Descriptor List Base Address Register (RDLB Offset 0x0014)

This register is used for the Receive descriptor list base address. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KSZ8842-PMQL/PMBL behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

Bit	Default	Read/ Write	Description
31 – 0	0x0	RW	***WSRL Start of Receive List*** Note: Write can only occur when the transmit process stopped.

Reserved (Offset 0x0018)

The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 0	0x0	RO	Reserved

Reserved (Offset 0x001C)

The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 0	0x0	RO	Reserved

MAC Multicast Table 0 Register (MTR0 Offset 0x0020)

The 64 bit multicast table is used for group address filtering. The hash value is defined as the six most significant bits of the CRC of the DA. The two most significant bits select the register to be used, while the other determines the bit within the register.

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The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 0	0x0	RW	***MTR0 Multicast Table 0*** When appropriate bit is set, the packet received with DA matches the CRC hashing function is received without being filtered. Note: when the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR then all multicast addresses are received regardless of the multicast table value..

MAC Multicast Table 1 Register (MTR1 Offset 0x0024)

The 64 bit multicast table is used for group address filtering. The hash value is defined as the six most significant bits of the CRC of the DA. The two most significant bits select the register to be used, while the other determines the bit within the register.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31-0	0x0	RW	***MTR0 Multicast Table 1*** When appropriate bit is set, the packet received with DA matches the CRC hashing function is received without being filtered. Note: when the receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR then all multicast addresses are received regardless of the multicast table value.

Interrupt Enable Register (INTEN Offset 0x0028)

This register enables the interrupts from the internal or external sources.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31	0	RW	***DMLCIE DMA MAC Link Changed Interrupt Enable*** When this bit is set, the DMA MAC Link Changed Interrupt is enabled. When this bit is reset, the DMA MAC Link Changed Interrupt is disabled.
30	0	RW	***DMTIE DMA MAC Transmit Interrupt Enable*** When this bit is set, the DMA MAC Transmit Interrupt is enabled. When this bit is reset, the DMA MAC Transmit Interrupt is disabled.
29	0	RW	***DMRIE DMA MAC Receive Interrupt Enable*** When this bit is set, the DMA MAC Receive Interrupt is enabled. When this bit is reset, the DMA MAC Receive Interrupt is disabled.
28	0	RW	***DMTBUIE DMA MAC Transmit Buffer Unavailable Interrupt Enable*** When this bit is set, the DMA MAC Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the DMA MAC Transmit Buffer Unavailable Interrupt is disabled.
27	0	RW	***DMRBUIE DMA MAC Receive Buffer Unavailable Interrupt Enable*** When this bit is set, the DMA MAC Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the DMA MAC Receive Buffer Unavailable Interrupt is disabled.
26	0	RW	***DMTPSIE DMA MAC Transmit Process Stopped Interrupt Enable*** When this bit is set, the DMA MAC Transmit Process Stopped Interrupt is enabled. When this bit is reset, the DMA MAC Transmit Process Stopped Interrupt is disabled.

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Bit	Default	R/W	Description
25	0	RW	***DMRPSIE DMA MAC Receive Process Stopped Interrupt Enable*** When this bit is set, the DMA MAC Receive Process Stopped Interrupt is enabled. When this bit is reset, the DMA MAC Receive Process Stopped Interrupt is disabled.
24 – 0	–	RO	Reserved

Interrupt Status Register (INTST Offset 0x002C)

This register contains the status bits for the CPU. When the corresponding bit is set, the CPU is interrupted. The driver usually reads this register during interrupt service routine or polling. The register bits are not cleared when read. Each field can be masked.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31	0	RW	***DMLCS DMA MAC Link Changed Status*** When this bit is set, it indicates that the DMA MAC link status has changed from link up to link down or from link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
30	0	RW	***DMTS DMA MAC Transmit Status*** When this bit is set, it indicates that the DMA MAC has transmitted at least a frame on the DMA port and the MAC is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
29	0	RW	***DMRS DMA MAC Receive Status*** When this bit is set, it indicates that the DMA MAC has received a frame from the DMA port and it is ready for the host to process This edge-triggered interrupt status is cleared by writing 1 to this bit.
28	0	RW	***DMTBUS DMA MAC Transmit Buffer Unavailable Status*** When this bit is set, it indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the KSZ8842-PMQL/PMBL. The transmission process is suspended. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit start command. This edge-triggered interrupt status is cleared by writing 1 to this bit.
27	0	RW	***DMRBUS DMA MAC Receive Buffer Unavailable Status*** When this bit is set, it indicates that the descriptor list is owned by the host and cannot be acquired by the KSZ8842-PMQL/PMBL. The receiving process is suspended. To resume processing receive descriptors, the host should change the ownership of the descriptor and may issue a receive start command. If no receive start command is issued, the receiving process resumes when the next recognized incoming frame is received. After the first assertion, this bit is not asserted for any subsequent not owned receive descriptors fetches. This bit is asserted only when the previous receive descriptor was owned by the KSZ8842-PMQL/PMBL. This edge-triggered interrupt status is cleared by writing 1 to this bit.
26	0	RW	***DMTPSS DMA MAC Transmit Process Stopped Status*** Asserted when the DMA MAC transmit process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
25	0	RW	***DMRPSS DMA MAC Receive Process Stopped Status*** Asserted when the DMA MAC receive process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
24 – 0	–	RO	Reserved

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MAC Additional Station Address Low Register (MAAL0-15)

The KSZ8842-PMQL/PMBL supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KSZ8842-PMQL/PMBL will respond to when receiving frames on the port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31 – 0	–	RW	***MAAL0 MAC Additional Station Address 0 Low 4 bytes*** The least significant word of the additional MAC 0 station address.

MAC Additional Station Address High Register (MAAH0-15)

The KSZ8842-PMQL/PMBL supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KSZ8842-PMQL/PMBL will respond to when receiving frames on the host port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

Bit	Default	R/W	Description
31	0	RW	***MAA0E MAC Additional Station Address 0 Enable*** When set, the additional MAC address is enabled for received frames. When reset, the additional MAC address is disabled.
30 – 16	0x0	RO	Reserved
15 - 0	–	RW	***MAAH0 MAC Additional Station Address 0 High 2 bytes*** The most significant word of the additional MAC 0 station address.

The following table shows the register map for all 16 additional MAC address registers.

Register	IDENTIFIER	OFFSET
ADD MAC Low 0	MAAL0	0x0080
ADD MAC High 0	MAAH0	0x0084
ADD MAC Low 1	MAAL1	0x0088
ADD MAC High 1	MAAH1	0x008C
ADD MAC Low 2	MAAL2	0x0090
ADD MAC High 2	MAAH2	0x0094
ADD MAC Low 3	MAAL3	0x0098
ADD MAC High 3	MAAH3	0x009C
ADD MAC Low 4	MAAL4	0x00A0
ADD MAC High 4	MAAH4	0x00A4
ADD MAC Low 5	MAAL5	0x00A8
ADD MAC High 5	MAAH5	0x00AC
ADD MAC Low 6	MAAL6	0x00B0
ADD MAC High 6	MAAH6	0x00B4
ADD MAC Low 7	MAAL7	0x00B8
ADD MAC High 7	MAAH7	0x00BC
ADD MAC Low 8	MAAL8	0x00C0
ADD MAC High 8	MAAH8	0x00C4

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Register	IDENTIFIER	OFFSET
ADD MAC Low 9	MAAL9	0x00C8
ADD MAC High 9	MAAH9	0x00CC
ADD MAC Low 10	MAAL10	0x00D0
ADD MAC High 10	MAAH10	0x00D4
ADD MAC Low 11	MAAL11	0x00D8
ADD MAC High 11	MAAH11	0x00DC
ADD MAC Low 12	MAAL12	0x00E0
ADD MAC High 12	MAAH12	0x00E4
ADD MAC Low 13	MAAL13	0x00E8
ADD MAC High 13	MAAH13	0x00EC
ADD MAC Low 14	MAAL14	0x00F0
ADD MAC High 14	MAAH14	0x00F4
ADD MAC Low 15	MAAL15	0x00F8
ADD MAC High 15	MAAH15	0x00FC

MAC/PHY and Control Registers

MAC Address Register Low (0x0200): MARL

This register along with the other two MAC address registers are loaded starting at word location 0x10 of the EEPROM upon hardware reset. The register can be modified by the software driver, but will not modify the original MAC address value in the EEPROM. The MAC address is used to define the individual destination address that the KSZ8842-PMQL/PMBL host port will respond to when receiving unicast frames. This MAC address will become the source address when sending unicast frames from the host port to port-1 or port-2. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields for low word of MAC address.

Bit	Default	R/W	Description
15 – 0	–	RW	***MARL MAC Address Low*** The least significant word of the MAC address

MAC Address Register Middle (0x0202): MARM

This register along with the other two MAC address registers are loaded starting at word location 0x10 of the EEPROM upon hardware reset. The register can be modified by the software driver, but will not modify the original MAC address value in the EEPROM. MAC address is used to define the individual destination address the KSZ8842-PMQL/PMBL will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

Bit	Default	R/W	Description
15 – 0	–	RW	***MARM MAC Address Middle*** The middle word of the MAC address

MAC Address Register High (0x0204): MARH

This register along with the other two MAC address registers are loaded starting at word location 0x10 of the EEPROM upon hardware reset. The register can be modified by software driver, but will not modify the original MAC address value in the EEPROM. MAC address is used to define the individual destination address the KSZ8842-PMQL/PMBL will

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respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

Bit	Default	R/W	Description
15-0	–	RW	***MARH MAC Address High*** The Most significant word of the MAC address

Reserved (Offset 0x0206 - 0x020A

The following table shows the register bit fields.

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

On-Chip Bus Control Register (Offset 0x0210): OBCR

This register controls the on-chip bus speed for the KSZ8842-PMQL/PMBL. It is used for reduced power consumption when the external host CPU is running at a slow frequency. The default of the on-chip bus speed is 25MHz. When the external host CPU is running at a higher clock rate, adjust the on-chip bus for the best performance.

The following table shows the register bit fields.

Bit	Default	R/W	Description
15 – 2	–	RO	Reserved
1 – 0	0x3	RW	***OBSC On-Chip Bus Speed Control*** 00: 125MHz 01: 62.5MHz 10: 41.66MHz 11: 25MHz

EEPROM Control Register (Offset 0x0212): EEPCR

KSZ8842-PMQL/PMBL supports designs with and without an EEPROM system design. To support an external EEPROM, tie the EEPROM Enable (EEEN) pin/ball to High; otherwise, tie it to Low or no connect. The KSZ8842-PMQL/PMBL allows software to access (read and write) the EEPROM directly; that is, the EEPROM access timing can be fully controlled by the software if the EEPROM Software Access bit 4 in EEPCR is set.

The following table shows the register bit fields.

Bit	Default	R/W	Description
15 – 5	0	RO	Reserved
4	0	RW	***EESA EEPROM Software Access*** 1 = Enable software to access EEPROM through bit 3 to bit 0. 0 = Disable software to access EEPROM.
3	00	RO	***EECB EEPROM Status Bits*** Bit 3: Data Out from EEPROM. This bit directly reflects the value of the EEDI pin/ball.
2	00	RW	***EECB EEPROM Control Bits*** Bit 2: Data In to EEPROM. This bit directly controls the device's the EEDO pin/ball.
1	00	RW	***EECB EEPROM Control Bits*** Bit 1: Serial Clock. This bit directly controls the device's the EESK pin/ball.
0	00	RW	***EECB EEPROM Control Bits*** Bit 0: Chip Select. This bit directly controls the device's the EECS pin/ball.

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Memory BIST Info Register (Offset 0x0214): MBIR

The following table shows the register bit fields.

Bit	Default	R/W	Description
15 – 13	0x0	RO	Reserved
12	–	RO	***TXMBF TX Memory Bits Finish*** When set, it indicates the Memory Built In Self Test has completed for the TX Memory.
11	–	RO	***TXMBFA TX Memory Bits Fail*** When set, it indicates the Memory Built In Self Test has failed.
10 – 5	–	RO	Reserved
4	–	RO	***RXMBF RX Memory Bits Finish*** When set, it indicates the Memory Built In Self Test has completed for the RX Memory.
3	–	RO	***RXMBFA RX Memory Bits Fail*** When set, it indicates the Memory Built In Self Test has failed.
2 – 0	–	RO	Reserved

Global Reset Register (Offset 0x0216): GRR

This register holds control information programmed by the CPU to control the global soft reset function.

Bit	Default	R/W	Description
15 – 1	0x00	RO	Reserved
0	0	RW	***Global Soft Reset*** 1 = Software reset active 0 = Software reset inactive Set two times to finish the software reset, this soft reset bit will reset PCI control/status registers only.

Switch Registers

Switch ID and Enable Register (Offset 0x0400): SIDER

This register contains the switch ID, and the switch-enable control.

Bit	Default	R/W	Description
15 – 8	0x88	RO	***Family ID*** Chip family
7 – 4	0x4	RO	***Chip ID***
3 – 1	000	RO	***Revision ID***
0	–	RW	***Start Switch*** 1 = start the chip

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Switch Global Control Register 1 (Offset 0x0402): SGCR1

This register contains the global control for the switch function.

Bit	Default	R/Write	Description
15	0	RW	**Pass all frames** 1 = switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with Sniffer mode only.
14	0	RW	**Reserved.** For factory test purposes only. Always write 0.
13	1	RW	**IEEE 802.3x Transmit direction flow control enable** 1 = will enable transmit direction flow control feature. 0 = will not enable transmit direction flow control feature. Switch will not generate any flow control packets.
12	1	RW	**IEEE 802.3x Receive direction flow control enable** 1 = will enable receive direction flow control feature. 0 = will not enable receive direction flow control feature. Switch will not react to any received flow control packets.
11	1	RW	**Frame Length field check** 1 = will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500).
10	1	RW	**Aging enable** 1 = enable age function in the chip 0 = disable age function in the chip
9	0	RW	**Fast age enable** 1 = turn on fast age (800µs)
8	0	RW	**Aggressive back off enable** 1 = enable more aggressive back off algorithm in half duplex mode to enhance performance. This is not an IEEE standard.
6 – 4	0x4	RW	Reserved
3	0x0	RW	Reserved
3	1	RW	**Pass flow control packet** 1 = switch will not filter 802.1x “flow control” packets.
2	1	RW	Reserved
1	0	RW	Reserved
0	0	RW	**Link change age** 1 = link change from “link” to “no link” will cause fast aging (<800µs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 ± 75 seconds). **Note:** If any port is unplugged, all addresses will be automatically aged out.

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Switch Global Control Register 2 (Offset 0x0404): SGCR2

This register contains the global control for the switch function.

Bit	Default	R/W	Description
15	0	RW	***802.1Q VLAN enable*** 1 = 802.1Q VLAN mode is turned on. VLAN table needs to set up before the operation. 0 = 802.1Q VLAN is disabled.
14	0	RW	***IGMP snoop enable*** 1 = IGMP snoop is enabled. All the IGMP packets will be forwarded to the host port. 0 = IGMP snoop is disabled.
13	0	RW	***IPv6 MLD snooping enable*** 1 = enable IPv6 MLD snooping
12	0	RW	***IPv6 MLD snooping option*** 1 = enable IPv6 MLD snooping option.
11	0	RW	***Priority Scheme select*** 0 = always TX higher priority packets first 1 = Weighted Fair Queuing enable. When all 4 queues has packets waiting to TX, the bandwidth allocation is q3:q2:q1:q0 = 8:4:2:1. If any queues is empty, the highest non-empty queue will get one more weighting. For example, if q2 is empty, q3:q2:q1:q0 will become (8+1): 0 :2 : 1.
10 – 9	0	RW	Reserved. For factory test purposes only. Always write 0.
8	0	RW	***Sniff mode select*** 1 = will do RX AND TX sniff (both source port and destination port need to match) 0 = will do RX OR TX sniff (Either source port or destination port needs to match). This is the mode used to implement rx only sniff.
7	1	RW	***Unicast port-VLAN mismatch discard*** 1 = all packets can not cross VLAN boundary 0 = unicast packets (excluding unknown/multicast/broadcast) can cross VLAN boundary
6	1	RW	***Multicast storm protection disable*** 1 = “Broadcast Storm Protection” does not include multicast packets. Only DA = FFFFFFFFFFFF packets will be regulated. 0 = “Broadcast Storm Protection” includes DA = FFFFFFFFFFFF and DA[40] = 1 packets.
5	1	RW	***Back pressure mode*** 1 = carrier sense based backpressure is selected 0 = collision based backpressure is selected
4	1	RW	***Flow control and back pressure fair mode*** 1 = fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. 0 = in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be “fair” to the flow control port.

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Bit	Default	R/W	Description
3	0	RW	***No excessive collision drop*** 1 = the switch will not drop packets when 16 or more collisions occur. 0 = the switch will drop packets when 16 or more collisions occur.
2	0	RW	***Huge packet support*** 1 = will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of the same register. 0 = the max packet size will be determined by bit 1 of this register.
1	0	RW	***Legal Maximum Packet size check enable*** 0 = will accept packet sizes up to 1536 bytes (inclusive). 1 = 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.
0	1	RW	***Priority Buffer reserve*** 1 = each ports pre-allocated 48 buffers, used exclusively for high priority packets(q3,q2,q1). Effective only when multiple queues feature is turned on. 0 = each ports pre-allocated 48 buffers, used for all priority packets (q3,q2,q1,q0).

Switch Global Control Register 3 (Offset 0x0406): SGCR3

This register contains the global control for the switch function.

Bit	Default	R/W	Description
15 – 8	0x63	RW	***Broadcast storm protection rate*** Bit [7:0] These bits, along with SGCR3[2:0], determines how many “64-byte blocks” of packet data are allowed on an input port in a preset period. The period is 67ms for 100Base-T or 670ms for 10Base-T. The default is 1%.
7	0	RW	***Repeater mode*** 1 = enable repeater mode 0 = normal mode Note: The Repeater only supports 100Base-T, halfduplex modes. When set to repeater mode, need to disable follow control in register MDTXC[9]
6	0	RW	***Switch host port duplex mode*** 1 = enable switch host interface half duplex mode. 0 = enable switch host interface full duplex mode. (Keep default value to match DMA MAC to the full duplex mode only).
5	0	RW	***Switch host port flow control enable*** 1 = enable full duplex flow control on Switch host interface. 0 = disable full duplex flow control on Switch host interface.
4	0	RW	Reserved (must be 0)
3	0	RW	***Null VID replacement*** 1 = replaces NULL VID with port VID(12 bits) 0 = no replacement for NULL VID
2 – 0	000	RW	Broadcast storm protection rate Bit [10:8] These bits, along with SGCR3[15-8], determines how many “64-byte blocks” of packet data allowed on an input port in a preset period. The period is 67ms for 100Base-T or 670ms for 10Base-T. The default is 1%.

Rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx.) = 0x63

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Switch Global Control Register 4 (Offset 0x0408): SGCR4

This register contains the global control for the switch function.

Bit	Default	R/W	Description
15 – 0	0x2400	RW	Reserved. For factory testing purposes only.

Switch Global Control Register 5 (Offset 0x040A): SGCR5

This register contains the global control for the switch function.

<table>
<tr><th>Bit</th><th>Default</th><th>R/W</th><th>Description</th></tr>
<tr><td>15</td><td>0</td><td>RW</td><td>LEDSEL1
See description for bit 9.</td></tr>
<tr><td>14</td><td>0</td><td>RW</td><td>Reserved</td></tr>
<tr><td>13</td><td>0</td><td>RW</td><td>Reserved</td></tr>
<tr><td>12</td><td>0</td><td>RW</td><td>Testing mode
Reserved , must be 0</td></tr>
<tr><td>11 – 10</td><td>0</td><td>RW</td><td>Reserved</td></tr>
<tr><td>9</td><td>0</td><td>RW</td><td>LEDSEL0
The two register bits LEDSEL1 and LEDSEL0, are used to select the LED mode.
Port x LED Indicators as Switch mode defined as below:
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[0, 0]</td><td>[0, 1]</td></tr>
<tr><td>PxLED3</td><td>—</td><td>—</td></tr>
<tr><td>PxLED2</td><td>LINK/ACT</td><td>100LINK/ACT</td></tr>
<tr><td>PxLED1</td><td>FULL_DPX/COL</td><td>10LINK/ACT</td></tr>
<tr><td>PxLED0</td><td>SPEED</td><td>FULL_DPX</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">[LEDSEL1, LEDSEL0]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>PxLED3</td><td>ACT</td><td>—</td></tr>
<tr><td>PxLED2</td><td>LINK</td><td>—</td></tr>
<tr><td>PxLED1</td><td>FULL_DPX/COL</td><td>—</td></tr>
<tr><td>PxLED0</td><td>SPEED</td><td>—</td></tr>
</table>
Port 1 and port 2 LED indicators as Repeater mode defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1] [1,0] [1,1]</td></tr>
<tr><td>P1LED3</td><td>RPT_COL</td><td>—</td></tr>
<tr><td>P1LED2</td><td>RPT_Link3/RX</td><td>—</td></tr>
<tr><td>P1LED1</td><td>RPT_Link2/RX</td><td>—</td></tr>
<tr><td>P1LED0</td><td>RPT_Link1/RX</td><td>—</td></tr>
</table>
</td></tr>
</table>

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Bit	Default	R/W	Description
			<table><tr><td></td><td colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</td></tr><tr><td></td><td>[0,0] Default</td><td>[0,1] [1,0] [1,1]</td></tr><tr><td>P2LED3</td><td>RPT_ACT</td><td>—</td></tr><tr><td>P2LED2</td><td>RPT_ERR3</td><td>—</td></tr><tr><td>P2LED1</td><td>RPT_ERR2</td><td>—</td></tr><tr><td>P2LED0</td><td>RPT_ERR1</td><td>—</td></tr></table> Note: See pin/ball description for detail definition
8	0	RW	Reserved
7 – 0	0x24	RW	Reserved. For factory testing purposes only.

Switch Global Control Register 6 (Offset 0x0410): SGCR6

This register contains the global control for the switch function.

Bit	Default	R/W	Description
15:14	0x3	RW	***Tag_0x7*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x7.
13:12	0x3	RW	***Tag_0x6*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x6.
11:10	0x2	RW	***Tag_0x5*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x5.
9:8	0x2	RW	***Tag_0x4*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x4.
7:6	0x1	RW	***Tag_0x3*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x3.
5:4	0x1	RW	***Tag_0x2*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x2.
3:2	0x0	RW	***Tag_0x1*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x1.
1:0	0x0	RW	***Tag_0x0*** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x0.

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Switch Global Control Register 7 (0x0412): SGCR7

This register contains the global control for the switch function.

Bit	Default	R/W	Description
15 – 8	0	RW	
7	0	RW	***Unknown Default Port Enable*** Send packets with unknown destination address to specified ports in bits [2:0]. 1 = enable to send unknown DA packet
6 – 3	0x0	RW	For factory test only. Always write 0.
2 – 0	0x7	RW	***Unknown Packet Default Port(s)*** Specify which ports to send packets with unknown destination addresses. Feature is enabled by bit [7]. Bit 2: for the host port Bit 1: for the port 2 Bit 0: for the port 1

Reserved (Offset 0x0414 - 0x046F)

MAC Address Register 1 (Offset 0x0470): MACAR1

This register contains the MAC address for the switch function. This MAC address is used to send the PAUSE frame.

Bit	Default	R/W	Description
15 – 0	0x0010	RW	***MACA[47:32]*** Specify host MAC address 1. This value must be the same as MAC Address Register High (0x0204): MARH.

MAC Address Register 2 (Offset 0x0472): MACAR2

This register contains the MAC address for the switch function. This MAC address is used to send the PAUSE frame.

Bit	Default	R/W	Description
15 – 0	0xA1FF	RW	***MACA[31:16]*** Specify host MAC address 2. This value must be the same as MAC Address Register Middle (0x0202): MARM.

MAC Address Register 3 (Offset 0x0474): MACAR3

This register contains the MAC address for the switch function. This MAC address is used to send the PAUSE frame.

Bit	Default	R/W	Description
15 – 0	0xFFFF	RW	MACA[15:0] Specify host MAC address 3. This value must be the same as MAC Address Register Low (0x0200): MARL.

Reserved (Offset 0x0476 - 0x047F)

This register is reserved.

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

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Priority Control Register 1 (Offset 0x0480): TOSR1

This register contains the TOS priority control for the switch function.

The IPv4/Ipv6 TOS priority control registers implement a fully decoded 64 DSCP (Differentiated Services Code Point) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bits in the DSCP register to determine the priority.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[15:14]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x1C.
13:12	0	RW	***DSCP[13:12]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x18.
11:10	0	RW	***DSCP[11:10]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x14.
9:8	0	RW	***DSCP[9:8]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x10.
7:6	0	RW	***DSCP[7:6]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x0C.
5:4	0	RW	***DSCP[5:4]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x08.
3:2	0	RW	**DSCP[3:2]** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x04.
1:0	0	RW	***DSCP[1:0]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x00.

TOS Priority Control Register 2 (Offset 0x482): TOSR2

This register contains the TOS priority control for the switch function.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[31:30]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x3C.
13:12	0	RW	***DSCP[29:28]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x38.
11:10	0	RW	***DSCP[27:26]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x34.
9:8	0	RW	***DSCP[25:24]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x30.
7:6	0	RW	***DSCP[23:22]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x2C.

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Bit	Default	R/W	Description
5:4	0	RW	***DSCP[21:20]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x28.
3:2	0	RW	***DSCP[19:18]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x24.
1:0	0	RW	***DSCP[17:16]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x20.

TOS Priority Control Register 3 (Offset 0x484): TOSR3

This register contains the TOS priority control for the switch function.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[47:46]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x5C.
13:12	0	RW	***DSCP[45:44]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x58.
11:10	0	RW	***DSCP[43:42]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x54.
9:8	0	RW	***DSCP[41:40]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x50.
7:6	0	RW	***DSCP[39:38]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x4C.
5:4	0	RW	***DSCP[37:36]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x48.
3:2	0	RW	***DSCP[35:34]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x44.
1:0	0	RW	***DSCP[33:32]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x40.

TOS Priority Control Register 4 (Offset 0x486): TOSR4

This register contains the TOS priority control for the switch function.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[63:62]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x7C.
13:12	0	RW	***DSCP[61:60]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x78.

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Bit	Default	R/W	Description
11:10	0	RW	***DSCP[59:58]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x74.
9:8	0	RW	***DSCP[57:56]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x70.
7:6	0	RW	***DSCP[55:54]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x6C.
5:4	0	RW	***DSCP[53:52]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x68.
3:2	0	RW	***DSCP[51:50]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x64.
1:0	0	RW	***DSCP[49:48]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x60.

TOS Priority Control Register 5 (Offset 0x488): TOSR5

This register contains the TOS priority control for the switch function.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[79:78]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x9C.
13:12	0	RW	***DSCP[77:76]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x98.
11:10	0	RW	***DSCP[75:74]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x94.
9:8	0	RW	***DSCP[73:72]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x90.
7:6	0	RW	***DSCP[71:70]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x8C.
5:4	0	RW	***DSCP[69:68]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x88.
3:2	0	RW	***DSCP[67:66]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x84.
1:0	0	RW	***DSCP[65:64]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0x80.

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TOS Priority Control Register 6 (Offset 0x48A): TOSR6

This register contains the TOS priority control for the switch function.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[95:94]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xbC.
13:12	0	RW	***DSCP[93:92]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xb8.
11:10	0	RW	***DSCP[91:90]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xb4.
9:8	0	RW	***DSCP[89:88]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xb0.
7:6	0	RW	***DSCP[87:86]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xaC.
5:4	0	RW	***DSCP[85:84]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xa8.
3:2	0	RW	***DSCP[83:82]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xa4.
1:0	0	RW	***DSCP[81:80]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xa0.

TOS Priority Control Register 7 (Offset 0x490): TOSR7

This register contains the TOS priority control for the switch function.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[111:110]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xdC.
13:12	0	RW	***DSCP[109:108]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xd8.
11:10	0	RW	***DSCP[107:106]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xd4.
9:8	0	RW	***DSCP[105:104]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xd0.
7:6	0	RW	***DSCP[103:102]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xcC.
5:4	0	RW	***DSCP[101:100]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xc8.

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Bit	Default	R/W	Description
3:2	0	RW	***DSCP[99:98]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xc4.
1:0	0	RW	***DSCP[97:96]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xc0.

TOS Priority Control Register 8 (Offset 0x492): TOSR8

This register contains the TOS priority control for the switch function.

Bit	Default	R/W	Description
15:14	0	RW	***DSCP[127:126]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xfC.
13:12	0	RW	***DSCP[125:124]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xf8.
11:10	0	RW	***DSCP[123:122]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xf4.
9:8	0	RW	***DSCP[121:120]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xf0.
7:6	0	RW	***DSCP[119:118]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xeC.
5:4	0	RW	***DSCP[117:116]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xe8.
3:2	0	RW	***DSCP[115:114]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xe4.
1:0	0	RW	***DSCP[113:112]*** The value in this field is used as the frame's priority when bits [7:2] of it IP TOS/DiffServ/Traffic Class value is 0xe0.

Reserved (Offset 0x0494 - 0x049A)

This register is reserved.

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

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Indirect Access Control Register (Offset 0x04A0): IACR

This register contains the indirect control for the switch function.

Bit	Default	R/W	Description
15 – 13	000	RW	Reserved
12	0	RW	***Read High. Write Low*** 1 = read cycle 0 = write cycle
11:10	00	RW	***Table select*** 00 = static MAC address table selected 01 = VLAN table selected 10 = dynamic address table selected 11 = MIB counter selected
9 – 0	0x000	RW	***Indirect address*** Bit 9-0 of indirect address

Note: (1) write IACR will actually trigger a command.
Read or write access is determined by Register bit 12.

Indirect Access Data Register 1 (Offset 0x04A2): IADR1

This register contains the indirect data for the switch function.

Bit	Default	R/W	Description
15 – 8	0x000	RO	Reserved
7	0	RO	***CPU Read Status*** Only for dynamic and statistics counter reads. 1 = read is still in progress 0 = read has completed
6 – 3	0x0	RO	Reserved
2 – 0	000	RO	***Indirect data.*** Bit 66-64 of indirect data

Indirect Access Data Register 2 (Offset 0x04A4): IADR2

This register contains the indirect data for the switch function.

Bit	Default	R/W	Description
15 – 0	0x0000	RW	***Indirect data*** Bit 47-32 of indirect data

Indirect Access Data Register 3 (Offset 0x04A6): IADR3

This register contains the indirect data for the switch function.

Bit	Default	R/W	Description
15 – 0	0x0000	RW	***Indirect data*** Bit 63-48 of indirect data

Indirect Access Data Register 4 (Offset 0x04A8): IADR4

This register contains the indirect data for the switch function.

Bit	Default	R/W	Description
15 – 0	0x0000	RW	***Indirect data*** Bit 15-0 of indirect data

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Indirect Access Data Register 5 (Offset 0x04AA): IADR5

This register contains the indirect data for the switch function.

Bit	Default	R/W	Description
15 – 0	0x0000	RW	***Indirect data*** Bit 31-16 of indirect data

Reserved (Offset 0x04B0 - 0x04BA)

Reserved (Offset 0x04C0 –0x04CF)

PHY 1 MII Basic Control Register (Offset 0x04D0): P1MBCR

This register contains the MII control for the switch port 1 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Soft reset*** Not supported	
14	0	RW	***Loop back*** 1 = perform loop back as follows: Start: RXP1/RXM1 (port 2) Loop back: PMD/PMA of port 1's PHY End: TXP1/TXM1 (port 2) 0 = normal operation.	P1CR4, bit 8
13	0	RW	***Force 100*** 1 = 100 Mbps if AN is disabled (bit 12) 0 = 10 Mbps if AN is disabled (bit 12)	P1CR4, bit 6
12	1	RW	***AN enable*** 1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	P1CR4, bit 7
11	0	RW	***Power down*** 1 = Power down the PHY 1 0 = Normal operation	P1CR4, bit 11
10	0	RO	***Isolate*** Not supported	
9	0	RW	***Restart AN*** 1 = Restart auto-negotiation 0 = Normal operation	P1CR4, bit 13
8	0	RW	***Force full duplex*** 1 = Full duplex if AN is disabled (bit 12) 0 = Half duplex if AN is disabled (bit 12)	P1CR4, bit 5
7	0	RO	***Collision test*** Not supported	
6	0	RO	Reserved	
5	0	R/W	***HP_mdix*** 1 = HP Auto MDIX mode 0 = Micrel Auto MDIX mode	P1SR, bit 15
4	0	RW	***Force MDIX*** 1 = Force MDIX 0 = Normal operation	P1CR4, bit 9

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Bit	Default	R/W	Description	Is the same as:
3	0	RW	***Disable MDIX*** 1 = Disable auto MDIX 0 = Normal operation	P1CR4, bit 10
2	0	RW	***Disable far end fault*** 1 = Disable far end fault detection 0 = Normal operation	P1CR4, bit 12
1	0	RW	***Disable transmit*** 1 = Disable transmit 0 = Normal operation	P1CR4, bit 14
0	0	RW	***Disable LED*** 1 = Disable LED 0 = Normal operation	P1CR4, bit 15

PHY 1 MII Basic Status Register (Offset 0x04D2): P1MBSR

This register contains the MII control for the switch port 1 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***T4 capable*** 1 = 100 BaseT4 capable 0 = Not 100 BaseT4 capable	
14	1	RO	***100 Full capable*** 1 = 100BaseTX full duplex capable 0 = Not capable of 100BaseTX full duplex	Always 1
13	1	RO	***100 Half capable*** 1 = 100BaseTX half duplex capable 0 = Not 100BaseTX half duplex capable	Always 1
12	1	RO	***10 Full capable*** 1 = 10BaseT full duplex capable 0 = Not 10BaseT full duplex capable	Always 1
11	1	RO	***10 Half capable*** 1 = 10BaseT half duplex capable 0 = Not 10BaseT half duplex capable	Always 1
10 – 7	0	RO	Reserved	
6	0	RO	***Preamble suppressed*** Not supported	
5	0	RO	***AN complete*** 1 = Auto-negotiation complete 0 = Auto-negotiation not completed	P1SR, bit 6
4	0	RO	***Far end fault*** 1 = Far end fault detected 0 = No far end fault detected	P1SR, bit 8
3	1	RO	***AN capable*** 1 = Auto-negotiation capable 0 = Not auto-negotiation capable	P1CR4, bit 7
2	0	RO	***Link status*** 1 = Link is up 0 = Link is down	P1SR, bit 5

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Bit	Default	R/W	Description	Is the same as:
1	0	RO	***Jabber test*** Not supported	
0	0	RO	***Extended capable*** 1 = Extended register capable 0 = Not extended register capable	

PHY 1 PHYID Low Register (Offset 0x04D4): PHY1ILR

This register contains the PHY ID (low) for the switch port 1 function.

Bit	Default	R/W	Description
15 – 0	0x1430	RO	***PHYID low*** Low order PHYID bits

PHY 1 PHYID High Register (Offset 0x04D6): PHY1IHR

This register contains the PHY ID (high) for the switch port 1 function.

Bit	Default	R/W	Description
15 – 0	0x0022	RO	***PHYID high*** High order PHYID bits

PHY 1 Auto-Negotiation Advertisement Register (Offset 0x04D8): P1ANAR

This register contains the auto-negotiation advertisement for the switch port 1 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Next page*** Not supported	
14	0	RO	Reserved	
13	0	RO	***Remote fault*** Not supported	
12:11	0	RO	Reserved	
10	1	RW	***Pause (follow control capability)*** 1 = Advertise pause ability 0 = Do not advertise pause ability	P1CR4, bit 4
9	0	RW	Reserved	
8	1	RW	***Adv 100 Full*** 1 = Advertise 100 full duplex ability 0 = Do not advertise 100 full duplex ability	P1CR4, bit 3
7	1	RW	***Adv 100 Half*** 1 = Advertise 100 half duplex ability 0 = Do not advertise 100 half duplex ability	P1CR4, bit 2
6	1	RW	***Adv 10 Full*** 1 = Advertise 10 full duplex ability 0 = Do not advertise 10 full duplex ability	P1CR4, bit 1
5	1	RW	***Adv 10 Half*** 1 = Advertise 10 half duplex ability 0 = Do not advertise 10 half duplex ability	P1CR4, bit 0
4 – 0	0_0001	RO	***Selector field*** 802.3	

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PHY 1 Auto-Negotiation Link Partner Ability Register (Offset 0x04DA): P1ANLPR

This register contains the auto-negotiation link partner ability for the switch port 1 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Next page*** Not supported	
14	0	RO	***LP ACK*** Not supported	
13	0	RO	***Remote fault*** Not supported	
12:11	0	RO	Reserved	
10	0	RO	***Pause*** Link partner pause capability	P1SR, bit 4
9	0	RO	Reserved	
8	0	RO	***Adv 100 Full*** Link partner 100 full capability	P1SR, bit 3
7	0	RO	***Adv 100 Half*** Link partner 100 half capability	P1SR, bit 2
6	0	RO	***Adv 10 Full*** Link partner 10 full capability	P1SR, bit 1
5	0	RO	***Adv 10 Half*** Link partner 10 half capability	P1SR, bit 0
4 – 0	0_0000	RO	Reserved	

PHY 2 MII Basic Control Register (Offset 0x04E0): P2MBCR

This register contains the MII control for the switch port 2 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Soft reset*** Not supported	
14	0	RW	***Loop back*** 1 = perform loop back, as indicated: Start: RXP2/RXM2 (port 1) Loop back: PMD/PMA of port 2's PHY End: TXP2/TXM2 (port 1) 0 = normal operation.	P2CR4, bit 8
13	0	RW	***Force 100*** 1 = 100 Mbps if AN is disabled (bit 12) 0 = 10 Mbps if AN is disabled (bit 12)	P2CR4, bit 6
12	1	RW	***AN enable*** 1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	
11	0	RW	***Power down*** 1 = Power down the PHY 2 0 = Normal operation	P2CR4, bit 11
10	0	RO	***Isolate*** Not supported	

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Bit	Default	R/W	Description	Is the same as:
9	0	RW	***Restart AN*** 1 = Restart auto-negotiation 0 = Normal operation	P2CR4, bit 13
8	0	RW	***Force full duplex*** 1 = Full duplex if AN is disabled (bit 12) 0 = Half duplex if AN is disabled (bit 12)	P2CR4, bit 5
7	0	RO	***Collision test*** Not supported	
6	0	RO	Reserved	
5	0	R/W	***HP_mdix*** 1 = HP Auto MDIX mode 0 = Micrel Auto MDIX mode	P2SR, bit 15
4	0	RW	***Force MDIX*** 1 = Force MDIX 0 = Normal operation	P2CR4, bit 9
3	0	RW	***Disable MDIX*** 1 = Disable auto MDIX 0 = Normal operation	P2CR4, bit 10
2	0	RW	***Disable far end fault*** 1 = Disable far end fault detection 0 = Normal operation	P2CR4, bit 12
1	0	RW	***Disable transmit*** 1 = Disable transmit 0 = Normal operation	P2CR4, bit 14
0	0	RW	***Disable LED*** 1 = Disable LED 0 = Normal operation	P2CR4, bit 15

PHY 2 MII Basic Status Register (Offset 0x04E2): P2MBSR

This register contains the MII control for the switch port 2 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***T4 capable*** 1 = 100 BaseT4 capable 0 = Not 100 BaseT4 capable	
14	1	RO	***100 Full capable*** 1 = 100BaseTX full duplex capable 0 = Not capable of 100BaseTX full duplex	Always 1
13	1	RO	***100 Half capable*** 1 = 100BaseTX half duplex capable 0 = Not 100BaseTX half duplex capable	Always 1
12	1	RO	***10 Full capable*** 1 = 10BaseT full duplex capable 0 = Not 10BaseT full duplex capable	Always 1
11	1	RO	***10 Half capable*** 1 = 10BaseT half duplex capable 0 = Not 10BaseT half duplex capable	Always 1

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Bit	Default	R/W	Description	Is the same as:
10-7	0	RO	Reserved	
6	0	RO	***Preamble suppressed*** Not supported	
5	0	RO	***AN complete*** 1 = Auto-negotiation complete 0 = Auto-negotiation not completed	P2SR, bit 6
4	0	RO	***Far end fault*** 1 = Far end fault detected 0 = No far end fault detected	P2SR, bit 8
3	1	RO	***AN capable*** 1 = Auto-negotiation capable 0 = Not auto-negotiation capable	P2CR4, bit 7
2	0	RO	***Link status*** 1 = Link is up 0 = Link is down	P2SR, bit 5
1	0	RO	***Jabber test*** Not supported	
0	0	RO	***Extended capable*** 1 = Extended register capable 0 = Not extended register capable	

PHY 2 PHYID Low Register (Offset 0x04E4): PHY2ILR

This register contains the PHY ID (low) for the switch port 2 function.

Bit	Default	R/W	Description
15 – 0	0x1430	RO	***PHYID low*** Low order PHYID bits

PHY 2 PHYID High Register (Offset 0x04E6): PHY2IHR

This register contains the PHY ID (high) for the switch port 2 function.

Bit	Default	R/W	Description
15 – 0	0x0022	RO	***PHYID high*** High order PHYID bits

PHY 2 Auto-Negotiation Advertisement Register (Offset 0x04E8): P2ANAR

This register contains the auto-negotiation advertisement for the switch port 2 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Next page*** Not supported	
14	0	RO	Reserved	
13	0	RO	***Remote fault*** Not supported	
12:11	0	RO	Reserved	
10	1	RW	***Pause*** 1 = Advertise pause ability 0 = Do not advertise pause ability	P2CR4, bit 4
9	0	RW	Reserved	

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Bit	Default	R/W	Description	Is the same as:
8	1	RW	***Adv 100 Full*** 1 = Advertise 100 full duplex ability 0 = Do not advertise 100 full duplex ability	P2CR4, bit 3
7	1	RW	***Adv 100 Half*** 1 = Advertise 100 half duplex ability 0 = Do not advertise 100 half duplex ability	P2CR4, bit 2
6	1	RW	***Adv 10 Full*** 1 = Advertise 10 full duplex ability 0 = Do not advertise 10 full duplex ability	P2CR4, bit 1
5	1	RW	***Adv 10 Half*** 1 = Advertise 10 half duplex ability 0 = Do not advertise 10 half duplex ability	P2CR4, bit 0
4 – 0	00001	RO	***Selector field*** 802.3	

PHY 2 Auto-Negotiation Link Partner Ability Register (Offset 0x04EA): P2ANLPR

This register contains the auto-negotiation link partner ability for the switch port 2 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Next page*** Not supported	
14	0	RO	***LP ACK*** Not supported	
13	0	RO	***Remote fault*** Not supported	
12:11	0	RO	Reserved	
10	0	RO	***Pause*** Link partner pause capability	P2SR, bit 4
9	0	RO	Reserved	
8	0	RO	***Adv 100 Full*** Link partner 100 full capability	P2SR, bit 3
7	0	RO	***Adv 100 Half*** Link partner 100 half capability	P2SR, bit 2
6	0	RO	***Adv 10 Full*** Link partner 10 full capability	P2SR, bit 1
5	0	RO	***Adv 10 Half*** Link partner 10 half capability	P2SR, bit 0
4 – 0	0_0000	RO	Reserved	

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PHY1 LinkMD Control/Status (Offset 0x04F0): P1VCT

This register contains the LinkMD control and status of PHY 1:

Bit	Default	R/W	Description	Is the same as:
15	0 (Self_Clear)	RW	***Vct_enable*** 1 = the cable diagnostic test is enabled. It'll be self-cleared after VCT test is done 0 = it indicates the cable diagnostic test is completed and the status information is valid for read	P1SCSLMD, bit 12
14:13	0	RO	***Vct_result*** [00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test is failed	P1SCSLMD, bits 14-13
12	-	RO	***Vct 10M short*** 1 = Less than 10 meter short	P1SCSLMD, bit 15
11 – 9	0	RO	Reserved	
8 – 0	0	RO	***Vct_fault_count*** Distance to the fault. The distance is approximately 0.4m X vct_fault_count	P1SCSLMD, bits 8-0

PHY1 Special Control/Status Register (Offset 0x04F2): P1PHYCTRL

This register contains the control and status information of PHY1:

Bit	Default	R/W	Description	Is the same as:
15 – 6	0	RO	Reserved	
5	0	RO	***Polarity reverse (polrvs)*** 1 = polarity is reversed 0 = polarity is not reversed	P1SR, bit 13
4	0	RO	***MDIX Status (mdix_st)*** 1 = MDI 0 = MDIX	P1SR, bit 7
3	0	RW	***Force Link (force_lnk)*** 1 = force link pass 0 = normal operation	P1SCSLMD, bit 11
2	1	RW	***Power Saving (pwrsave)*** 1 = disable 0 = enable power saving	P1SCSLMD, bit 10
1	0	RW	***Remote loop back (near end loop back)*** 1 = Loop back at PMD/PMA of port 1's PHY 0 = normal operation.	P1SCSLMD, bit 9
0	0	RW	Reserved	

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PHY2 LinkMD Control/Status (Offset 0x04F4): P2VCT

This register contains the LinkMD control and status of PHY 2:

Bit	Default	R/W	Description	Is the same as:
15	0 (Self_Clear)	RW	***Vct_enable*** 1 = the cable diagnostic test is enabled. It'll be self-cleared after VCT test is done 0 = it indicates the cable diagnostic test is completed and the status information is valid for read	P2SCSLMD, bit 12
14:13	0	RO	***Vct_result*** [00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test is failed	P2SCSLMD, bits 14-13
12	–	RO	***Vct 10M short*** 1 = Less than 10 meter short	P2SCSLMD, bit 15
11 – 9	0	RO	Reserved	
8 – 0	0	RO	***Vct_fault_count*** Distance to the fault. The distance is approximately 0.4m X vct_fault_count	P2SCSLMD, bits 8-0

PHY2 Special Control/Status Register (Offset 0x04F6): P2PHYCTRL

This register contains the control and status information of PHY2:

Bit	Default	R/W	Description	Is the same as:
15 – 6	0	RO	Reserved	
5	0	RO	***Polarity reverse (polrvs)*** 1 = polarity is reversed 0 = polarity is not reversed	P2SR, bit 13
4	0	RO	***MDIX Status (mdix_st)*** 1 = MDI 0 = MDIX	P2SR, bit 7
3	0	RW	***Force Link (force_lnk)*** 1 = force link pass 0 = normal operation	P2SCSLMD, bit 11
2	1	RW	***Power Saving (pwrsave)*** 1 = Disable 0 = Enable power saving	P2SCSLMD, bit 10
1	0	RW	***Remote loop back (near end loop back)*** 1 = Loop back at PMD/PMA of port 2's PHY 0 = normal operation.	P2SCSLMD, bit 9
0	0	RW	Reserved	

Reserved (Offset 0x04F8 - 0x04FA)

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

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Port 1 Control Register 1 (Offset 0x0500): P1CR1

This register contains the global per port control for the switch port 1 function.

Bit	Default	R/W	Description
15 – 8	0x00	RO	Reserved
7	0	RW	***Broadcast storm protection enable*** 1 = enable broadcast storm protection for ingress packets on the port 0 = disable broadcast storm protection
6	0	RW	***Diffserv priority classification enable*** 1 = enable diffserv priority classification for ingress packets on port 0 = disable diffserv function
5	0	RW	***802.1p priority classification enable*** 1 = enable 802.1p priority classification for ingress packets on port 0 = disable 802.1p
4:3	0	RW	***Port based priority classification*** 00 = ingress packets on port 1 will be classified as priority 0 queue if "Diffserv" or "802.1p" classification is not enabled or fails to classify. 01 = ingress packets on port 1 will be classified as priority 1 queue if "Diffserv" or "802.1p" classification is not enabled or fails to classify. 10 = ingress packets on port 1 will be classified as priority 2 queue if "Diffserv" or "802.1p" classification is not enabled or fails to classify. 11 = ingress packets on port 1 will be classified as priority 3 queue if "Diffserv" or "802.1p" classification is not enabled or fails to classify. Note: "Diffserv", "802.1p" and port priority can be enabled at the same time. The OR'ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	***Tag insertion*** 1 = when packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port's "port VID". 0 = disable tag insertion
1	0	RW	***Tag removal*** 1 = when packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = disable tag removal
0	0	RW	***TX Multiple Queues Select Enable*** 1 = the port output queue is split into four priority queues. 0 = single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

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Port 1 Control Register 2 (Offset 0x0502): P1CR2

This register contains the global per port control for the switch port 1 function.

Bit	Default	R/W	Description
15	0	RW	Reserved
14	0	RW	***Ingress VLAN filtering*** 1 = the switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port. 0 = no ingress VLAN filtering.
13	0	RW	***Discard Non PVID packets*** 1 = the switch will discard packets whose VID does not match ingress port default VID. 0 = no packets will be discarded.
12	0	RW	***Force flow control*** 1 = will always enable flow control on the port, regardless of AN result. 0 = the flow control is enabled based on AN result.
11	0	RW	***Back pressure enable*** 1 = enable port's half duplex back pressure 0 = disable port's half duplex back pressure.
10	1	RW	***Transmit enable*** 1 = enable packet transmission on the port 0 = disable packet transmission on the port
9	1	RW	***Receive enable*** 1 = enable packet reception on the port 0 = disable packet reception on the port
8	0	RW	***Learning disable*** 1 = disable switch address learning capability 0 = enable switch address learning
7	0	RW	***Sniffer port*** 1 = Port is designated as sniffer port and will transmit packets that are monitored. 0 = Port is a normal port
6	0	RW	***Receive sniff*** 1 = All the packets received on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port" 0 = no receive monitoring
5	0	RW	***Transmit sniff*** 1 = All the packets transmitted on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port" 0 = no transmit monitoring
4	0	RW	Reserved
3	0	R/W	***User Priority Field*** 1 = if the packet's "user priority field" is greater than the "user priority bits" in port 1's VID Control register bits [15:13], replace the packet's "user priority field" with the "user priority bits" in port 1's VID Control register bits [15:13]. 0 = do not compare and replace the packet's 'user priority field"

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Bit	Default	R/W	Description
2 – 0	111	RW	***Port VLAN membership*** Define the port's Port VLAN membership. Bit 2 stands for the host port, bit 1 for port 2, and bit 0 for port 1. The Port can only communicate within the membership. An '1' includes a port in the membership; an '0' excludes a port from the membership.

Port 1 VID Control Register (Offset 0x0504): P1VIDCR

This register contains the global per port control for the switch port 1 function.

Bit	Default	R/W	Description
15-13	000	RW	User Priority bits Port 1 tag [15-13] for priority
12	0	RW	CFI bit Port 1 tag [12] for CFI
11-0	0x001	RW	VID Port 1 tag [11-0] for VID

Note: P1VIDCR serve two purposes:

(1) Associated with the ingress untagged packets, and used for egress tagging.

(2) Default VID for the ingress untagged or null-VID-tagged packets, and used for address look up.

Port 1 Control Register 3 (Offset 0x0506): P1CR3

This register contains the port 1 control register for the switch port 1 function.

Bit	Default	R/W	Description
15 – 5	00000000000	RO	Reserved
4	0	RW	Reserved
3:2	00	RW	***Ingress Limit Mode.*** These bits determine what kinds of frames are limited and counted against Ingress limiting as follows: 00 = limit and count all frames 01 = limit and count Broadcast, Multicast, and flooded unicast frames 10 = limit and count Broadcast and Multicast frames only 11 = limit and count Broadcast frames only
1	0	RW	***Count IFG bytes*** 1 = each frame's minimum inter frame gap (IFG) bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. 0 = IFG bytes are not counted
0	0	RW	***Count Preamble bytes*** 1 = each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. 0 = preamble bytes are not counted

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Port 1 Ingress Rate Control Register (Offset 0x0508): P1IRCR

This register contains the port 1 ingress rate control register for the switch port 1 function.

Bit	Default	R/W	Description
15 – 12	0x0	RW	***Ingress Pri3 Rate*** Priority 3 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 =Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).
11 – 8	0x0	RW	***Ingress Pri2 Rate*** Priority 2 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).

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Bit	Default	R/W	Description
7 – 4	0x0	RW	***Ingress Pri1 Rate*** Priority 1 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).
3 – 0	0x0	RW	***Ingress Pri0 Rate*** Priority 0 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).

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Port 1 Egress Rate Control Register (Offset 0x050A): P1ERCR

This register contains the port 1 egress rate control register for the switch port 1 function.

Bit	Default	R/W	Description
15 – 12	0x0	RW	***Egress Pri3 Rate*** Egress data rate limit for priority 3 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
11 – 8	0x0	RW	***Egress Pri2 Rate*** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps

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Bit	Default	R/W	Description
			1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
7 – 4	0x0	RW	***Egress Pri1 Rate*** Egress data rate limit for priority 1 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
3 – 0	0x0	RW	***Egress Pri0 Rate*** Egress data rate limit for priority 0 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps

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Bit	Default	R/W	Description
			1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

Port 1 PHY Special Control/Status, LinkMD (Offset 0x0510): P1SCSLMD

This register contains the port LinkMD control register for the switch port 1 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Vct 10M short*** Less than 10 meter short	P1VCT, bit 12
14 – 13	0	RO	***Vct result*** [00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test is failed	P1VCT, bits 14-13
12	0	RW SC	***Vct enable*** 1 = the cable diagnostic test is enabled. It'll be self-cleared after VCT test is done 0 = it indicates the cable diagnostic test is completed and the status information is valid for read	P1VCT, bit 15
11	0	RW	***Force Link*** 1 = Force link pass 0 = Normal Operation	P1PHYCTRL, bit 3
10	1	RW	***Power Saving*** 1 = Disable 0 = Enable power saving	P1PHYCTRL, bit 2
9	0	RW	***Remote loop back*** 1 = Loop back at PMD/PMA of port 1's PHY 0 = normal operation.	P1PHYCTRL, bit 1
8 – 0	0x000	RO	***VCT fault count*** Distance to the fault. The distance is approximately 0.4mXvct_fault_count	P1VCT, bits 8-0

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Port 1 Control Register 4 (Offset 0x0512): P1CR4

This register contains the global per port control for the switch port 1 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RW	***LED off*** 1 = Turn off all port 1's LEDs (LED1_3, LED1_2, LED1_1, LED1_0). These pin/balls will be driven high if this bit is set to one. 0 = normal operation	P1MBCR, bit 0
14	0	RW	***Txids*** 1 = disable port's transmitter 0 = normal operation	P1MBCR, bit 1
13	0	RW	***Restart AN*** 1 = restart auto-negotiation 0 = normal operation	P1MBCR, bit 9
12	0	RW	***Disable Far end fault*** 1 = disable far end fault detection & pattern transmission. 0 = enable far end fault detection & pattern transmission.	P1MBCR, bit 2
11	0	RW	***Power down*** 1 = power down 0 = normal operation	P1MBCR, bit 11
10	0	RW	***Disable auto MDI/MDIX*** 1 = disable auto MDI/MDIX function 0 = enable auto MDI/MDIX function	P1MBCR, bit 3
9	0	RW	***Force MDIX*** 1 = If auto MDI/MDIX is disabled, force PHY into MDIX mode 0 = Do not force PHY into MDIX mode	P1MBCR, bit 4
8	0		***Loop back*** 1 = perform loop back, as indicated: Start: RXP2/RXM2 (port 2) Loop back: PMD/PMA of port 1's PHY End: TXP2/TXM2 (port 2) 0 = normal operation	P1MBCR, bit 14
7	1	RW	***Auto Negotiation Enable*** 0 = disable auto negotiation, speed and duplex are decided by bit 6 and 5 of the same register. 1 = auto negotiation is ON	P1MBCR, bit 12
6	0	RW	***Force Speed*** 1 = force 100Base-T if AN is disabled (bit 7) 0 = force 10Base-T if AN is disabled (bit 7)	P1MBCR, bit 13
5	0	RW	***Force duplex*** 1 = force full duplex if (1) AN is disabled or (2) AN is enabled but failed. 0 = force half duplex if (1) AN is disabled or (2) AN is enabled but failed.	P1MBCR, bit 9

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Bit	Default	R/W	Description	Is the same as:
4	1	RW	***Advertised flow control capability*** 1 = advertise flow control (pause) capability 0 = suppress flow control (pause) capability from transmission to link partner	P1ANAR, bit 4
3	1	RW	***Advertised 100BT Full duplex capability*** 1 = advertise 100Base-T Full duplex capability 0 = suppress 100Base-T Full duplex capability from transmission to link partner	P1ANAR, bit 3
2	1	RW	***Advertised 100BT half duplex capability*** 1 = advertise 100Base-T Half duplex capability 0 = suppress 100Base-T Half duplex capability from transmission to link partner	P1ANAR, bit 2
1	1	RW	***Advertised 10BT Full duplex capability*** 1 = advertise 10Base-T Full duplex capability 0 = suppress 10Base-T Full duplex capability from transmission to link partner	P1ANAR, bit 1
0	1	RW	***Advertised 10BT half duplex capability*** 1 = advertise 10Base-T Half duplex capability 0 = suppress 10Base-T Half duplex capability from transmission to link partner	P1ANAR, bit 0

Port 1 Status Register (Offset 0x0514): P1SR

This register contains the global per port status for the switch port 1 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RW	***HP_mdix*** 1 = HP Auto MDIX mode 0 = Micrel Auto MDIX mode	P1MBCR, bit 5
14	0	RO	Reserved	
13	0	RO	***Polarity reverse*** 1 = polarity is reversed 0 = polarity is not reversed	P1PHYCTRL, bit 5
12	0	RO	***Receive flow control enable*** 1 = Receive flow control feature is active 0 = Receive flow control feature is inactive	
11	0	RO	***Transmit flow control enable*** 1 = transmit flow control feature is active 0 = transmit flow control feature is inactive	
10	0	RO	***Operation Speed*** 1 = link speed is 100Mbps 0 = link speed is 10Mbps	
9	0	RO	***Operation duplex*** 1 = link duplex is full 0 = link duplex is half	
8	0	RO	***Far end fault*** 1 = Far end fault status detected 0 = no Far end fault status detected	P1MBSR, bit 4

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Bit	Default	R/W	Description	Is the same as:
7	0	RO	***MDIX status*** 1 = MDI 0 = MDIx	P1PHYCTRL,7 bit 4
6	0	RO	***AN done*** 1 = AN done 0 = AN not done	P1MBSR, bit 5
5	0	RO	***Link good*** 1 = Link good 0 = Link not good	P1MBSR, bit 2
4	0	RO	***Partner flow control capability*** 1 = link partner flow control (pause) capable 0 = link partner not flow control (pause) capable	P1ANLPR, bit 10
3	0	RO	***Partner 100BT full duplex capability*** 1 = link partner 100Base-T full duplex capable 0 = link partner not 100Base-T full duplex capable	P1ANLPR, bit 8
2	0	RO	***Partner 100BT half duplex capability*** 1 = link partner 100Base-T half duplex capable 0 = link partner not 100Base-T half duplex capable	P1ANLPR, bit 7
1	0	RO	***Partner 10BT full duplex capability*** 1 = link partner 10Base-T full duplex capable 0 = link partner not 10Base-T full duplex capable	P1ANLPR, bit 6
0	0	RO	***Partner 10BT half duplex capability*** 1 = link partner 10Base-T half duplex capable 0 = link partner not 10Base-T half duplex capable	P1ANLPR, bit 5

Port 1 Reserved (Offset 0x0516 – 0x051A)

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

Port 2 Control Register 1 (Offset 0x0520): P2CR1

This register contains the global per port control for the switch port 2 function.

Bit	Default	R/W	Description
15 – 8	0x00	RO	Reserved
7	0	RW	***Broadcast storm protection enable*** 1 = enable broadcast storm protection for ingress packets on the port 0 = disable broadcast storm protection
6	0	RW	***Diffserv priority classification enable*** 1 = enable diffserv priority classification for ingress packets on port 0 = disable diffserv function
5	0	RW	***802.1p priority classification enable*** 1 = enable 802.1p priority classification for ingress packets on port 0 = disable 802.1p
4 – 3	00	RW	***Port based priority classification*** 00 = ingress packets on port 1 will be classified as priority 0 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. 01 ingress packets on port 1 will be classified as priority 1 queue if

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Bit	Default	R/W	Description
			"Diffserv" or "802.1p" classification is not enabled or fails to classify. 10 = ingress packets on port 1 will be classified as priority 2 queue if "Diffserv" or "802.1p" classification is not enabled or fails to classify. 11 = ingress packets on port 1 will be classified as priority 3 queue if "Diffserv" or "802.1p" classification is not enabled or fails to classify. Note: "Diffserv", "802.1p" and port priority can be enabled at the same time. The OR'ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	***Tag insertion*** 1 = when packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port's "port VID". 0 = disable tag insertion
1	0	RW	***Tag removal*** 1 = when packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = disable tag removal
0	0	RW	***TX Multiple Queues Select Enable*** 1 = the port output queue is split into four priority queues. 0 = single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

Port 2 Control Register 2 (Offset 0x0522): P2CR2

This register contains the global per port control for the switch port 2 function.

Bit	Default	R/W	Description
15	reserved	reserved	Reserved
14	0	RW	***Ingress VLAN filtering*** 1 = the switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port. 0 = no ingress VLAN filtering.
13	0	RW	***Discard Non PVID packets*** 1 = the switch will discard packets whose VID does not match ingress port default VID. 0 = no packets will be discarded.
12	0	RW	***Force flow control*** 1 = will always enable flow control on the port, regardless of AN result. 0 = the flow control is enabled based on AN result.
11	0	RW	***Back pressure enable*** 1 = enable port's half duplex back pressure 0 = disable port's half duplex back pressure.
10	1	RW	***Transmit enable*** 1 = enable packet transmission on the port 0 = disable packet transmission on the port
9	1	RW	***Receive enable*** 1 = enable packet reception on the port 0 = disable packet reception on the port

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Bit	Default	R/W	Description
8	0	RW	***Learning disable*** 1 = disable switch address learning capability 0 = enable switch address learning
7	0	RW	***Sniffer port*** 1 = Port is designated as sniffer port and will transmit packets that are monitored. 0 = Port is a normal port
6	0	RW	***Receive sniff*** 1 = All the packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = no receive monitoring
5	0	RW	***Transmit sniff*** 1 = All the packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = no transmit monitoring
4	0	RW	Reserved
3	0	R/W	***User Priority Field*** 1 = if the packet’s “user priority field” is greater than the “user priority bits” in port 2’s VID Control register bits [15:13], replace the packet’s “user priority field” with the “user priority bits” in port 2’s VID Control register bits [15:13]. 0 = do not compare and replace the packet’s ‘user priority field”
2 – 0	111	RW	***Port VLAN membership*** Define the port’s Port VLAN membership. Bit 2 stands for port 3, bit 1 for port 2, and bit 0 for port 1. The Port can only communicate within the membership. An ‘1’ includes a port in the membership; an ‘0’ excludes a port from the membership.

Port 2 VID Control Register (Offset 0x0524): P2VIDCR

This register contains the global per port control for the switch port 2 function.

Bit	Default	R/W	Description
15 – 13	000	RW	User Priority bits Port 2 tag [15-13] for priority
12	0	RW	CFI bit Port 2 tag [12] for CFI
11 – 0	0x001	RW	VID bits Port 2 tag [11-0] for VID

Note: P2VIDCR serve two purposes:

(1) Associated with the ingress untagged packets, and used for egress tagging.

(2) Default VID for the ingress untagged or null-VID-tagged packets, and used for address look up.

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Port 2 Control Register 3 (Offset 0x0526): P2CR3

This register contains the control register for the switch port 2 function.

Bit	Default	R/W	Description
15 – 5	000	RO	Reserved
4			
3 – 2	00	RW	***Ingress Limit Mode*** These bits determine what kinds of frames are limited and counted against Ingress limiting as follows: 00 = Limit and count all frames 01 = Limit and count Broadcast, Multicast, and flooded unicast frames 10 = Limit and count Broadcast and Multicast frames only 11 = Limit and count Broadcast frames only
1	0	RW	***Count IFG bytes*** 1 = each frame's minimum inter frame gap (IFG) bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. 0 = IFG bytes are not counted
0	0	RW	Count Preamble bytes. 1 = each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. 0 = preamble bytes are not counted

Port 2 Ingress Rate Control Register (Offset 0x0528): P2IRCR

This register contains the port 2 ingress rate control register for the switch port 2 function.

Bit	Default	R/W	Description
15 – 12	0x0	RW	***Ingress Pri3 Rate*** Priority 3 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).

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Bit	Default	R/W	Description
11 – 8	0x0	RW	***Ingress Pri2 Rate*** Priority 2 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).
7 – 4	0x0	RW	***Ingress Pri1 Rate*** Priority 1 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).

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Bit	Default	R/W	Description
3 – 0	0x0	RW	***Ingress Pri0 Rate*** Priority 0 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).

Port 2 Egress Rate Control Register (Offset 0x052A): P2ERCR

This register contains the port 2 egress rate control register for the switch port 2 function.

Bit	Default	Def	R/W	Description
15 – 12	0x0	0	RW	***Egress Pri3 Rate*** Egress data rate limit for priority 3 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps

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Bit	Default	Def	R/W	Description
				Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
11 – 8	0x0	0	RW	***Egress Pri2 Rate*** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
7 – 4	0x0	0	RW	***Egress Pri2 Rate*** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps

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Bit	Default	Def	R/W	Description
				1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
3 – 0	0x0	0	RW	***Egress Pri0 Rate*** Egress data rate limit for priority 0 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

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Port 2 PHY Special Control/Status, LinkMD (Offset 0x0530): P2SCSLMD

This register contains the port 2 LinkMD control register for the switch port 2 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RO	***Vct 10M short*** Less than 10 meter short	P2VCT, bit 12
14:13	0	RO	***Vct result*** [00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test is failed	P2VCT, bits 14-13
12	0	RW SC (self-clear)	***Vct enable*** 1 = the cable diagnostic test is enabled. It'll be self-cleared after VCT test is done 0 = it indicates the cable diagnostic test is completed and the status information is valid for read	P2VCT, bit 15
11	0	RW	***Force Link*** 1 = Force link pass 0 = Normal Operation	P2PHYCTRL, bit 3
10	1	RW	***Power Saving*** 1 = Disable 0 = Enable power saving	P2PHYCTRL, bit 2
9	0	RW	***Remote loop back >>*** 1 = Loop back at PMD/PMA of port 2's PHY End: TXP2/TXM2 (port 2) 0 = normal operation.	P2PHYCTRL, bit 1
8 – 0	0	RO	***VCT fault count*** Distance to the fault. It's approximately 0.4m*vct_fault_count	P2VCT, bits 8-0

Port 2 Control Register 4 (Offset 0x0532): P2CR4

This register contains the global per port control for the switch port 2 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RW	***LED off*** 1 = Turn off all port 2's LEDs (LED2_3, LED2_2, LED2_1, LED2_0. These pin/balls will be driven high if this bit is set to one. 0 = normal operation	P2MBCR, bit 0
14	0	RW	***Txids*** 1 = disable port's transmitter 0 = normal operation	P2MBCR, bit 1
13	0	RW	***Restart AN*** 1 = restart auto-negotiation 0 = normal operation	P2MBCR, bit 9
12	0	RW	***Disable Far end fault*** 1 = disable far end fault detection & pattern transmission. 0 = enable far end fault detection & pattern transmission.	P2MBCR, bit 2

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Bit	Default	R/W	Description	Is the same as:
11	0	RW	***Power down*** 1 = power down 0 = normal operation	P2MBCR, bit 11
10	0	RW	***Disable auto MDI/MDIX*** 1 = disable auto MDI/MDIX function 0 = enable auto MDI/MDIX function	P2MBCR, bit 3
9	0	RW	***Force MDIX*** 1 = If auto MDI/MDIX is disabled, force PHY into MDIX mode 0 = Do not force PHY into MDIX mode	P2MBCR, bit 4
8	0	RW	***Loop back*** 1 = perform loop back, as indicated: Start: RXP1/RXM1 (port 1) Loop back: PMD/PMA of port 2's PHY End: TXP1/TXM1 (port 1) 0 = normal operation	P2MBCR, bit 14
7	1	RW	***Auto Negotiation Enable*** 0 = disable auto negotiation, speed and duplex are decided by bit 6 and 5 of the same register. 1 = auto negotiation is ON	P2MBCR, bit 12
6	0	RW	***Force Speed*** 1 = force 100Base-T if AN is disabled (bit 7) 0 = force 10Base-T if AN is disabled (bit 7)	P2MBCR, bit 13
5	0	RW	***Force duplex*** 1 = force full duplex if (1) AN is disabled or (2) AN is enabled but failed. 0 = force half duplex if (1) AN is disabled or (2) AN is enabled but failed.	P2MBCR, bit 9
4	1	RW	***Advertised flow control capability*** 1 = advertise flow control (pause) capability 0 = suppress flow control (pause) capability from transmission to link partner	P1ANAR, bit 4
3	1	RW	***Advertised 100BT Full duplex capability*** 1 = advertise 100Base-T Full duplex capability 0 = suppress 100Base-T Full duplex capability from transmission to link partner	P1ANAR, bit 3
2	1	RW	***Advertised 100BT half duplex capability*** 1 = advertise 100Base-T Half duplex capability 0 = suppress 100Base-T Half duplex capability from transmission to link partner	P1ANAR, bit 2
1	1	RW	***Advertised 10BT Full duplex capability*** 1 = advertise 10Base-T Full duplex capability 0 = suppress 10Base-T Full duplex capability from transmission to link partner	P1ANAR, bit 1
0	1	RW	***Advertised 10BT half duplex capability*** 1 = advertise 10Base-T Half duplex capability 0 = suppress 10Base-T Half duplex capability from transmission to link partner	P1ANAR, bit 0

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Port 2 Status Register (Offset 0x0534): P2SR

This register contains the global per port status for the switch port 2 function.

Bit	Default	R/W	Description	Is the same as:
15	0	RW	***HP_mdix*** 1 = HP Auto MDIX mode 0 = Micrel Auto MDIX mode	P2MBCR, bit 5
14	0	RO	Reserved	
13	0	RO	***Polarity reverse*** 1 = polarity is reversed 0 = polarity is not reversed	P2PHYCTRL, bit 5
12	0	RO	***Receive flow control enable*** 1 = Receive flow control feature is active 0 = Receive flow control feature is inactive	
11	0	RO	***Transmit flow control enable*** 1 = transmit flow control feature is active 0 = transmit flow control feature is inactive	
10	0	RO	***Operation Speed*** 1 = link speed is 100Mbps 0 = link speed is 10Mbps	
9	0	RO	***Operation duplex*** 1 = link duplex is full 0 = link duplex is half	
8	0	RO	***Far end fault*** 1 = Far end fault status detected 0 = no Far end fault status detected	P2MBCR, bit 4
7	0	RO	***MDIX status*** 1 = MDIX 0 = MDI	P2PHYCTRL, bit 4
6	0	RO	***AN done*** 1 = AN done 0 = AN not done	P2MBSR, bit 5
5	0	RO	***Link good*** 1 = Link good 0 = Link not good	P2MBSR, bit 2
4	0	RO	***Partner flow control capability*** 1 = link partner flow control (pause) capable 0 = link partner not flow control (pause) capable	P2ANLPR, bit 10
3	0	RO	***Partner 100BT full duplex capability*** 1 = link partner 100Base-T full duplex capable 0 = link partner not 100Base-T full duplex capable	P2ANLPR, bit 8
2	0	RO	***Partner 100BT half duplex capability*** 1 = link partner 100Base-T half duplex capable 0 = link partner not 100Base-T half duplex capable	P2ANLPR, bit 7
1	0	RO	***Partner 10BT full duplex capability*** 1 = link partner 10Base-T full duplex capable 0 = link partner not 10Base-T full duplex capable	P2ANLPR, bit 6

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Bit	Default	R/W	Description	Is the same as:
0	0	RO	***Partner 10BT half duplex capability*** 1 = link partner 10Base-T half duplex capable 0 = link partner not 10Base-T half duplex capable	P2ANLPR, bit 5

Port 2 Reserved (Offset 0x0536 – 0x053A)

This register is reserved.

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

Host Control Register 1 (Offset 0x0540): P3CR1

This register contains the global per port control for the switch host port function.

Bit	Default	R/W	Description
15 – 8	0x00	RO	Reserved
7	0	RW	***Broadcast storm protection enable*** 1 = enable broadcast storm protection for ingress packets on the port 0 = disable broadcast storm protection
6	0	RW	***Diffserv priority classification enable*** 1 = enable diffserv priority classification for ingress packets on port 0 = disable diffserv function
5	0	RW	***802.1p priority classification enable*** 1 = enable 802.1p priority classification for ingress packets on port 0 = disable 802.1p
4 – 3	00	RW	***Port based priority classification*** 00 = ingress packets on port 1 will be classified as priority 0 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. 01 = ingress packets on port 1 will be classified as priority 1 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. 10 = ingress packets on port 1 will be classified as priority 2 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. 11 = ingress packets on port 1 will be classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “Diffserv”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	***Tag insertion*** 1 = when packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = disable tag insertion
1	0	RW	***Tag removal*** 1 = when packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = disable tag removal
0	0	RW	***TX Multiple Queues Select Enable*** 1 = the port output queue is split into fourpriority queues. 0 = single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

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Host Control Register 2 (Offset 0x0542): P3CR2

This register contains the global per port control for the switch host port function.

Bit	Default	R/W	Description
15	0	RW	reserved
14	0	RW	***Ingress VLAN filtering*** 1 = the switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port. 0 = no ingress VLAN filtering.
13	0	RW	***Discard Non PVID packets*** 1 = the switch will discard packets whose VID does not match ingress port default VID. 0 = no packets will be discarded.
12	0	RW	Reserved. For factory testing purpose only. Always write 0.
11	0	RW	Reserved Must be 0
10	1	RW	***Transmit enable*** 1 = enable packet transmission on the port 0 = disable packet transmission on the port
9	1	RW	***Receive enable*** 1 = enable packet reception on the port 0 = disable packet reception on the port
8	0	RW	***Learning disable*** 1 = disable switch address learning capability 0 = enable switch address learning
7	0	RW	Sniffer port 1 = Port is designated as sniffer port and will transmit packets that are monitored. 0 = Port is a normal port
6	0	RW	***Receive sniff*** 1 = All the packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = no receive monitoring
5	0	RW	***Transmit sniff*** 1 = All the packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port” 0 = no transmit monitoring
4	0	RW	Reserved
3	0	R/W	***User Priority Field*** 1 = if the packet’s “user priority field” is greater than the “user priority bits” in host’s VID Control register bits [15:13], replace the packet’s “user priority field” with the “user priority bits” in host’s VID Control register bits [15:13]. 0 = do not compare and replace the packet’s ‘user priority field”
2 – 0	111	RW	***Port VLAN membership*** Define the port’s Port VLAN membership. Bit 2 stands for host port, bit 1 for port 2, and bit 0 for port 1. The Port can only communicate within the membership. An ‘1’ includes a port in the membership; an ‘0’ excludes a port from the membership.

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Host VID Control Register (Offset 0x0544): P3VIDCR

This register contains the global per port control for the switch host port function.

Bit	Default	R/W	Description
15-13	000	RW	***User Priority bits*** Host Port default tag bits [15-13] for user priority
12	0	RW	***CFI bit*** Host Port default tag bit 12 for CFI
11-0	0x001	RW	***VID bits*** Host Port default tag bits [11-0] for VID

Note: P3VIDCR serve two purposes:

(1) Associated with the ingress untagged packets, and used for egress tagging.

(2) Default VID for the ingress untagged or null-VID-tagged packets, and used for address look up.

Host Control Register 3 (Offset 0x0546): P3CR3

This register contains the host port control register for the switch host port function.

Bit	Default	Name	R/W	Description
15 – 5	000	Reserved	RO	Reserved
4	0	Reserved		
3-2	00	0	RW	***Ingress Limit Mode*** These bits determine what kinds of frames are limited and counted against Ingress limiting as follows: 00 = Limit and count all frames 01 = Limit and count Broadcast, Multicast, and flooded unicast frames 10 = Limit and count Broadcast and Multicast frames only 11 = Limit and count Broadcast frames only
1	0	0	RW	***Count IFG bytes*** 1 = each frame's minimum inter frame gap (IFG) bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. 0 = IFG bytes are not counted
0	0	0	RW	***Count Preamble bytes*** 1 = each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. 0 = preamble bytes are not counted

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Host Ingress Rate Control Register (Offset 0x0548): P3IRCR

This register contains the host port ingress rate control register for the switch host port function.

Bit	Default	Name	R/W	Description
15 – 12	0x0	0	RW	***Ingress Pri3 Rate*** Priority 3 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).
11 – 8	0x0	0	RW	***Ingress Pri2 Rate*** Priority 2 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).

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Bit	Default	Name	R/W	Description
7 – 4	0x0	0	RW	***Ingress Pri1 Rate*** Priority 1 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).
3 – 0	0x0	0	RW	***Ingress Pri0 Rate*** Priority 0 frames will be discarded after the ingress rate selected as shown below, is reached or exceeded: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited).

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Host Egress Rate Control Register (Offset 0x054A): P3ERCR

This register contains the host port egress rate control register for the switch host port function.

Bit	Default	Name	R/W	Description
15 – 12	0x0	0	RW	***Egress Pri3 Rate*** Egress data rate limit for priority 3 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
11 – 8	0x0	0	RW	***Egress Pri2 Rate*** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps

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Bit	Default	Name	R/W	Description
				Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
7 – 4	0x0	0	RW	***Egress Pri1 Rate*** Egress data rate limit for priority 1 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
3 – 0	0x0	0	RW	***Egress Pri0 Rate*** Egress data rate limit for priority 0 frames. Output traffic from this priority queue is shaped according to the egress rate selected as shown below: 0000 = Not limited (Default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps

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Bit	Default	Name	R/W	Description
				1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10Base-T, rate settings above 10Mbps are set to the default value 0000 (Not limited). Note: When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

Reserved (Offset 0x0550)

This register is reserved.

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

Reserved (Offset 0x0554)

This register is reserved.

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

Reserved (Offset 0x0556)

This register is reserved.

Bit	Default	R/W	Description
15 – 0	0x0000	RO	Reserved

Reserved (Offset 0x0560)

This register is reserved for internal testing.

Bit	Default	R/W	Description
15 – 10	0x00	RO	Reserved
9 – 0	–	RO	Reserved

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MIB (Management Information Base) Counters

The KSZ8842-PMQL/PMBL provides 32 MIB counters for port 1, port 2, and the host port. These counters are used to monitor the port activity for network management. The MIB counters are formatted “per port” as shown in Table 8, and “per all port dropped packet” as shown in Table 8.

Bit	Name	R/W	Description	Default
31	Overflow	RO	1 = counter overflow. 0 = no counter overflow.	0
30	Count valid	RO	1 = counter value is valid. 0 = counter value is not valid.	0
29-0	Counter values	RO	Counter value	0

Table 8. Format of Per Port MIB Counters

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for both Ethernet ports are:

Port 1, base address of the MIB counter is 0x00 and range is (0x00-0x1f) as shown in Table 9.

Port 2, base address of the MIB counter is 0x20 and range is (0x20-0x3f) as refer in Table 9.

Host port, base address of the MIB counter is 0x40 and range is (0x40-0x5f) as refer in Table 9.

Per Port MIB counters read/write functions use Access Control register IACR (0x04A0) bit 12. The base address offset and address range for port 1 is 0x00 and range is (0x00-0x1F) that can be changed in register IACR (0x04A0) bits[9:0]. The data of MIB counters are from the Indirect Access data register IADR4 (0x04A8) and IADR5 (0x04AA) based on Table 9.

Offset	Counter Name	Description
0x0 (base address)	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 or 1522 bytes)
0x5	RxJabbers	Rx packets longer than 1522 bytes w/ either CRC errors, alignment errors, or symbol errors (depends on max packet size setting)
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on max packet size setting)
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting)
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in EtherType field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in

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Offset	Counter Name	Description
		length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting)
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multicast packets)
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	**TxDeferred**	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	**Successfully Tx frames on a port for which Tx is inhibited by more than one collision**

Table 9. Port 1s “Per Port” MIB Counters Indirect Memory Offsets

Format of “All Port Dropped Packet” MIB Counters

Bit	Default	R/W	Description
30 – 16	–	N/A	Reserved
15 – 0	–	RO	Counter Value

Table 10. “All Port Dropped Packet” MIB Counters Format

Note: “All Port Dropped Packet” MIB Counters do not indicate overflow or validity; therefore, the application must keep track of overflow and valid
conditions.

“All Port Dropped Packet” MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 11.

Offset	Counter Name	Description
0x100	Port1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port2 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port2 RX Drop Packets	RX packets dropped due to lack of resources

Table 11. “All Port Dropped Packet” MIB Counters Indirect Memory Offsets

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Examples:

1. MIB Counter Read (read port 1 “Rx64Octets” counter at indirect address offset 0x0E)
   Write to reg. IACR with 0x1c0e (set indirect address and trigger a read MIB counters operation)
   Then
   Read reg. IADR5 (MIB counter value 31-16) // If bit 31 =1, there was a counter overflow
   // If bit 30 =0, restart (reread) from this register
   Read reg. IADR4 (MIB counter value 15-0)
2. MIB Counter Read (read port 2 “Rx64Octets” counter at indirect address offset 0x2E)
   Write to reg. IACR with 0x1c2e (set indirect address and trigger a read MIB counters operation)
   Then
   Read reg. IADR5 (MIB counter value 31-16) // If bit 31 =1, there was a counter overflow
   // If bit 30 =0, restart (reread) from this register
   Read reg. IADR4 (MIB counter value 15-0)
3. MIB Counter Read (read “Port1 TX Drop Packets” counter at indirect address offset 0x100)
   Write to reg. IACR with 0x1d00 (set indirect address and trigger a read MIB counters operation)
   Then
   Read reg. IADR4 (MIB counter value 15-0)

Additional MIB Information

Per Port MIB counters are designed as “read clear”. That is, these counters will be cleared after they are read.

All Port Dropped Packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

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Static MAC Address Table

The KSZ8842-PMQL/PMBL supports both a static and a dynamic MAC address table. In response to a Destination Address (DA) look up, The KSZ8842-PMQL/PMBL searches both tables to make a packet forwarding decision. In response to a Source Address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. These entries in the static table will not be aged out by the KSZ8842-PMQL/PMBL.

Bit	Default	R/W	Description
57 – 54	0000	RW	***FID*** Filter VLAN ID - identifies one of the 16 active VLANs.
53	0	R/W	***Use FID*** 1 =specifies the use of FID+MAC for static table look ups 0 = specifies only the use of MAC for static table look ups
52	0	R/W	***Override*** 1 = overrides the port setting “transmit enable=0” or “receive enable=0” setting. 0 = specifies no override
51	0	R/W	***Valid*** 1 = specifies that this entry is valid, the look up result will be used 0 = specifies that this entry is not valid
50 – 48	000	R/W	***Forwarding ports*** These 3 bits control the forwarding port(s): 000 ,no forward 001, forward to port 1 010, forward to port 2 100, forward to port 3 011, forward to port 1 and port 2 110, forward to port 2 and port 3 101, forward to port 1 and port 3 111, broadcasting (excluding the ingress port)
47 – 0	0	R/W	***MAC address*** 48 bits MAC Address

Table 12. Static MAC Table Format (8 Entries)

Examples:

1. Static Address Table Read (read the second entry at indirect address offset 0x01)

   Write to reg. IACR with 0x1001 (set indirect address and trigger a read static MAC table operation)

   Then

   Read reg. IADR3 (static MAC table bits 57-48)
   Read reg. IADR2 (static MAC table bits 47-32)
   Read reg. IADR5 (static MAC table bits 31-16)
   Read reg. IADR4 (static MAC table bits 15-0)

2. Static Address Table Write (write the eighth entry at indirect address offset 0x07)

   Write to reg. IADR3 (static MAC table bits 57-48)
   Write to reg. IADR2 (static MAC table bits 47-32)
   Write to reg. IADR5 (static MAC table bits 31-16)
   Write to reg. IADR4 (static MAC table bits 15-0)
   Write to reg. IACR with 0x0007 (set indirect address and trigger a write static MAC table operation)

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Dynamic MAC Address Table

The Dynamic MAC address is a read only table.

Bit	Default	R/W	Description
71		RO	***Data not ready*** 1 = specifies that the entry is not ready, continue retrying until bit is set to 0 0 = specifies that the entry is ready
70 – 67		RO	Reserved
66	1	RO	***MAC empty*** 1 = specifies that there is no valid entry in the table 0 = specifies that there are valid entries in the table
65 – 56	00_0000_0000	RO	***No of valid entries*** Indicates how many valid entries in the table 0x3ff means 1 K entries 0x001 means 2 entries 0x000 and bit 66 = 0 means 1 entry 0x000 and bit 66 = 1 means 0 entry
55 – 54		RO	***Time Stamp*** Specifies the 2-bit counter for internal aging.
53 – 52	00	RO	***Source port*** Identifies the source port where FID+MAC is learned: 00, port 1 01, port 2 10, port 3
51 – 48	0x0	RO	***FID*** Specifies the filter ID.
47 – 0	0x000_0000_0000	RO	***MAC Address*** Specifies the 48-bit MAC address.

Table 13. Dynamic MAC Address Table Format (1024 Entries)

Example:

Dynamic MAC Address Table Read (read the first entry at indirect address offset 0 and retrieve the MAC table size)

Write to reg. IACR with 0x1800 (set indirect address and trigger a read dynamic MAC table operation)

Then

Read reg. IADR1 (dynamic MAC table bits 71-64) // If bit 71 =1, restart (reread) from this register

Read reg. IADR3 (dynamic MAC table bits 63-48)

Read reg. IADR2 (dynamic MAC table bits 47-32)

Read reg. IADR5 (dynamic MAC table bits 31-16)

Read reg. IADR4 (dynamic MAC table bits 15-0)

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VLAN Table

The KSZ8842-PMQL/PMBL uses the VLAN table to perform look ups. If 802.1Q VLAN mode is enabled (SGCR2[15]), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (filter ID), VID (VLAN ID), and VLAN membership as described in table 14:

Bit	Default	R/W	Description
19	1	RW	***Valid*** 1 = specifies that this entry is valid, the look up result will be used 0 = specifies that this entry is not valid
18 – 16	111	R/W	***Membership*** Specifies which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example: 101 means port 3 and 1 are in this VLAN.
15 – 12	0x0	R/W	***FID*** Specifies the Filter ID. The KSZ8842-PMQL/PMBL supports 16 active VLANs represented by these four bit fields. The FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.
11 – 0	0x001	R/W	***VID*** Specifies the IEEE 802.1Q 12 bits VLAN ID.

Table 14. VLAN Table Format (16 Entries)

If 802.1Q VLAN mode is enabled, KSZ8842-PMQL/PMBL will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non null VID, the VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

Examples:

1. VLAN Table Read (read the third entry, at the indirect address offset 0x02)

   Write to reg. IACR with 0x1402 (set indirect address and trigger a read VLAN table operation)

   Then

   Read reg. IADR5 (VLAN table bits 19-16)

   Read reg. IADR4 (VLAN table bits 15-0)

2. VLAN Table Write (write the seventh entry, at the indirect address offset 0x06)

   Write to reg. IADR5 (VLAN table bits 19-16)

   Write to reg. IADR4 (VLAN table bits 15-0)

   Write to reg. IACR with 0x1406 (set indirect address and trigger a read VLAN table operation)

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Absolute Maximum Ratings[1]

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... –0.5V to +4.0V
Input Voltage (all inputs). ..... –0.5V to +5.0V
Output Voltage (all outputs) ..... –0.5V to +4.0V
Lead Temperature (soldering, 10sec.) ..... 270°C
Storage Temperature (T_s) ..... –55°C to +150°C

Operating Ratings[2]

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... +3.1V to +3.5V
Ambient Temp. of MQL/MBL(T_A) ..... 0°C to +70°C
Ambient Temp. of MQLI/MBL AM(T_A) . -40°C to +85°C
Junction Temperature (T_J) ..... 125°C
Package Thermal Resistance[3]
PQFP (θ_{JA}) No Air Flow ..... 42.91°C/W
PQFP (θ_{JC}) No Air Flow ..... 19.6°C/W
LFBGA (θ_{JA}) No Air Flow ..... 38.50°C/W
LFBGA (θ_{JC}) No Air Flow ..... 12.50°C/W

Electrical Characteristics[4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current 100BASE-TX Operation (All Ports @ 100% Utilization)						
I_{DDXIO}	100BASE-TX (Analog Core + PLL + Digital Core + Transceiver + Digital I/O)	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V		122		mA
10BASE-T Operation (All Ports @ 100% Utilization)						
I_{DDXIO}	100BASE-T (Analog Core + PLL + Digital Core + Transceiver + Digital I/O)	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V		90		mA
TTL Inputs						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ V_{DDIO}	–10		10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –8mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.4	V
I_{OZ}	Output Tri-state Leakage				10	µA
100Base-TX Transmit (measured differentially after 1:1 transformer) V_{DDATX} = 3.3V only						
V_O	Peak Differential Output Voltage	100Ω termination on the differential output.	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination on the differential output.			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of I_{SET}			0.5		V
	Output Jitter	Peak to peak		0.7	1.4	ns
10Base-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
10Base-T Transmit (measured differentially after 1:1 transformer) V_{DDATX} = 3.3V only						
V_P	Peak Differential Output Voltage	100Ω termination on the differential output.		2.4		V
	Jitter Added	100Ω termination on the differential output.		1.8	±3.5	ns

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Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than those listed in the table above may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD})
3. No (HS) heat spreader in this package. The thermal junction to ambient (θ_{JA}) and the thermal junction to case (θ_{JC}) are under air velocity 0m/s.
4. Specification for packaged product only. A single port's transformer consumes an additional 45mA at 3.3V for 100BASE-T and 70mA at 3.3V for 10BASE-T.

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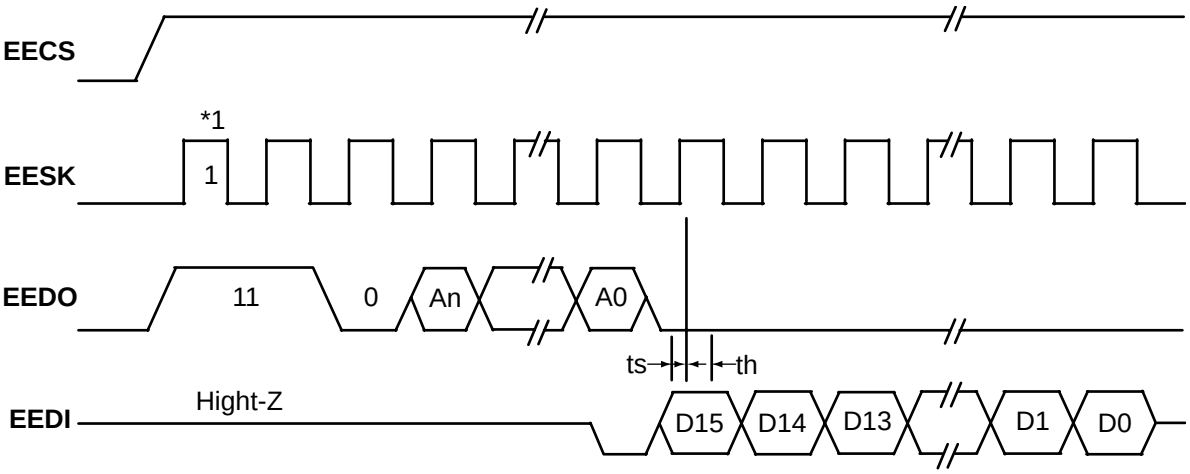
Timing Diagrams

For PCI Timing, please refer to PCI specification version 2.2.

EEPROM Timing



*1 Start bit

Figure 12. EEPROM Read Cycle Timing Diagram

Timing Parameter	Description	Min	Typ	Max	Unit
t_{cyc}	Clock cycle		4000		ns
t_s	Setup time	20			ns
t_h	Hold time	20			ns

Table 15. EEPROM Timing Parameters

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Auto Negotiation Timing

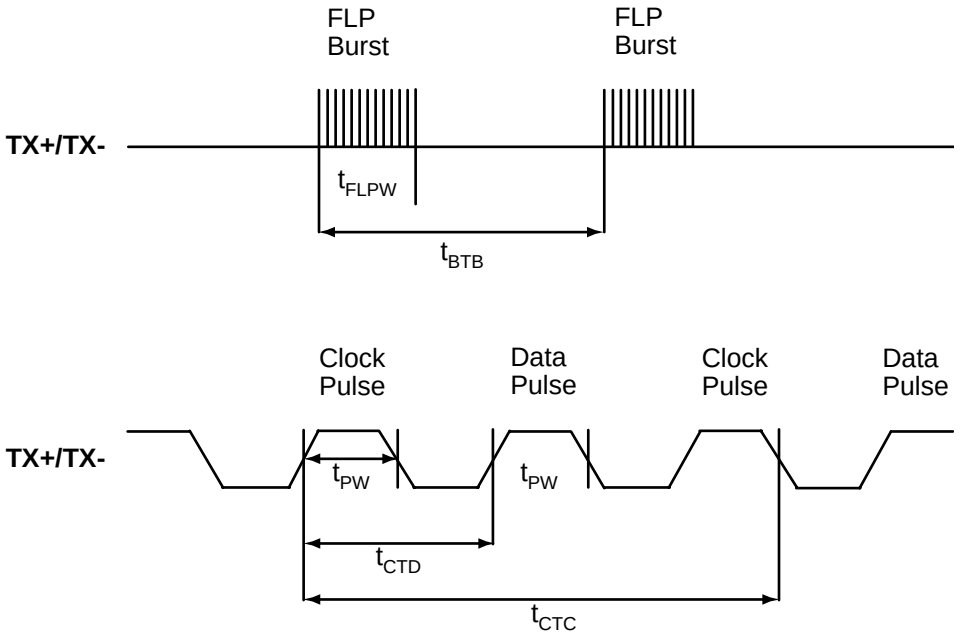

Figure 13. Auto-Negotiation Timing

Timing Parameter	Description	Min	Typ	Max	Unit
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of Clock/Data pulses per burst	17		33	

Table 16. Auto Negotiation Parameters

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Reset Timing

As long as the stable supply voltages to reset High timing (minimum of 10ms) are met, there is no power-sequencing requirement for the KSZ8842-PMQL/PMBL supply voltages 3.3V.

The reset timing requirement is summarized in the Figure 14 and Table 17.

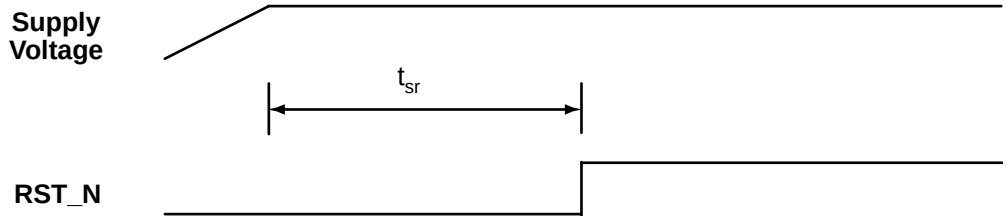

Figure 14. Reset Timing

Symbol	Parameter	Min	Max	Unit
t_{sr}	Stable supply voltages to reset High	10		ms

Table 17. Reset Timing Parameters

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Selection of Isolation Transformers

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 18 gives recommended transformer characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min)	350μH	100mV, 100kHz, 8mA
Leakage inductance (max)	0.4μH	1MHz (min)
Inter-winding capacitance (max)	12pF	
D.C. resistance (max)	0.9Ω	
Insertion loss (max)	1.0dB	0MHz – 65MHz
HIPOT (min)	1500Vrms	

Table 18. Transformer Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Pulse	H1102	Yes	1
Pulse (low cost)	H1260	Yes	1
Transpower	HB726	Yes	1
Bel Fuse	S558-5999-U7	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1
TDK (Mag Jack)	TLA-6T718	Yes	1

Table 19. Qualified Single Port Magnetics

Selection of Reference Crystal

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm
Load capacitance (max)	20	pF
Series resistance	25	Ω

Table 20. Typical Reference Crystal Characteristics

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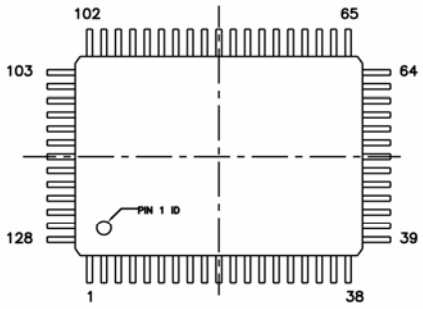
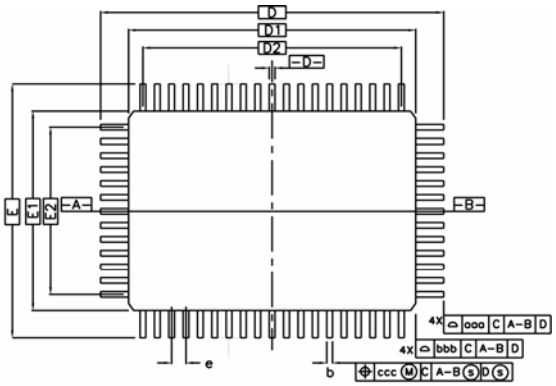
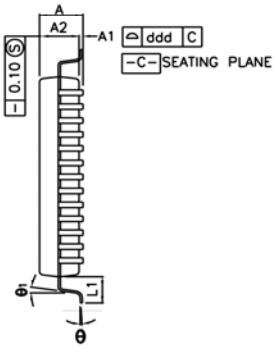
Package Information



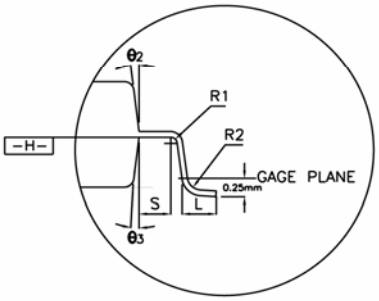
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAILED VIEW

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.

Figure 15. 128-Pin PQFP

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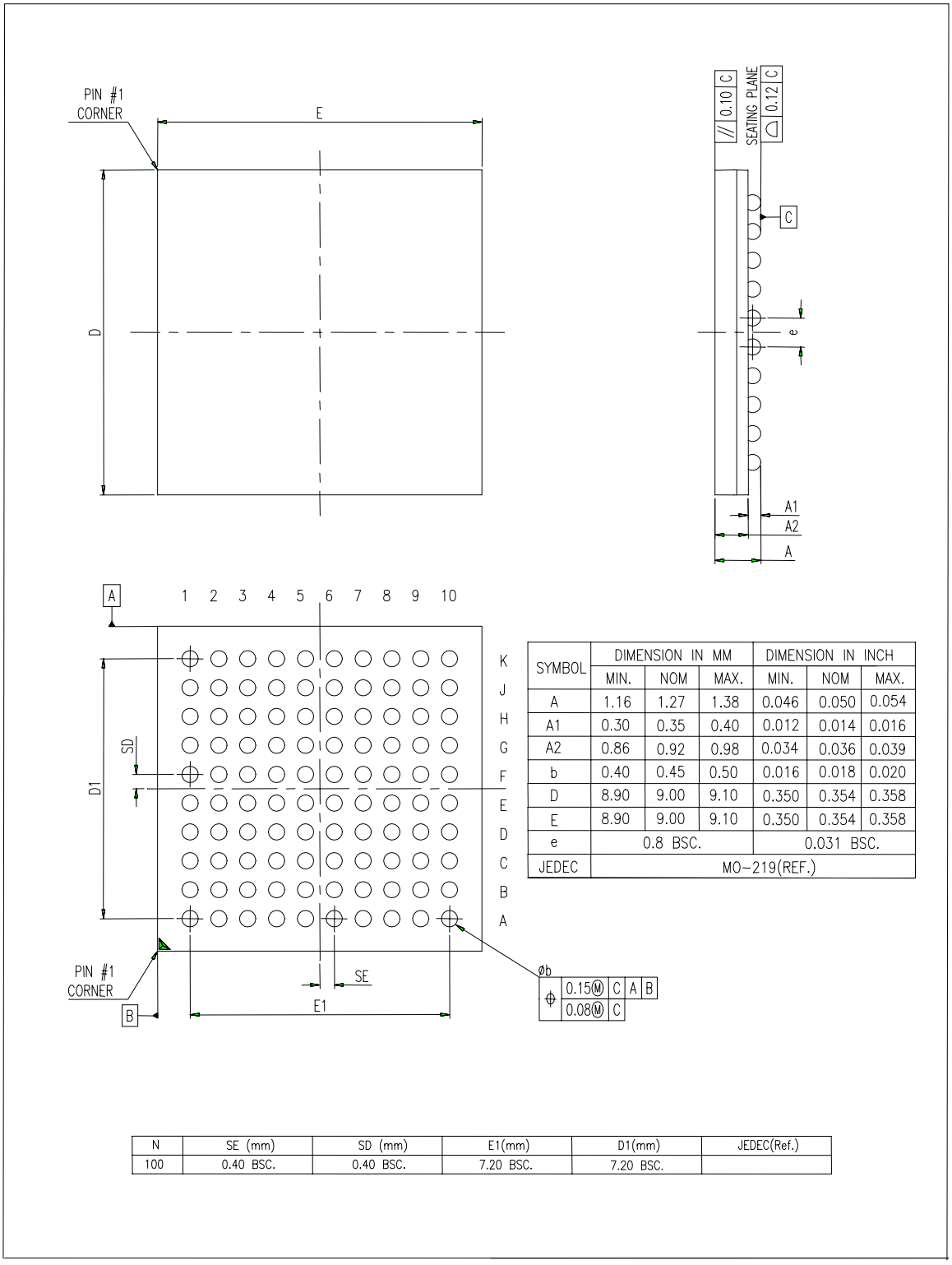
Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	1.16	1.27	1.38	0.046	0.050	0.054
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	0.86	0.92	0.98	0.034	0.036	0.039
b	0.40	0.45	0.50	0.016	0.018	0.020
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
e	0.8 BSC.			0.031 BSC.		
JEDEC	MO-219(REF.)					

N	SE (mm)	SD (mm)	E1(mm)	D1(mm)	JEDEC(Ref.)
100	0.40 BSC.	0.40 BSC.	7.20 BSC.	7.20 BSC.	

Figure 16. 100-Ball LFBGA

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Acronyms and Glossary

BPDU	Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS	Complementary Metal Oxide Semiconductor.	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC	Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
DA	Destination Address	The address to send packets.
DMA	Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EISA	Extended Industry Standard Architecture	A bus architecture designed for PCs using 80x86 processors, or an Intel 80386, 80486 or Pentium microprocessor. EISA buses are 32 bits wide and support multiprocessing.
EMI	Electro-Magnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS	Frame Check Sequence	See CRC.
FID	Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IPG	Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISI	Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
ISA	Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
MDI	Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or crossover, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore 'media dependent.'
MDI-X	Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB	Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical),

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		and can also change operating parameters in network nodes (static forwarding addresses).
MII	Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC	Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
PLL	Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
PME	Power Management Event	An occurrence that affects the directing of power to different components of a system.
SA	Source Address	The address from which information has been sent.
TDR	Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal -- or part of the signal -- to return.
UTP	Unshielded Twisted Pair	Commonly a cable containing 4 twisted pairs of wires. The wires are twisted in such a manner as to cancel electrical interference generated in each wire, therefore shielding is not required.
VLAN	Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

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