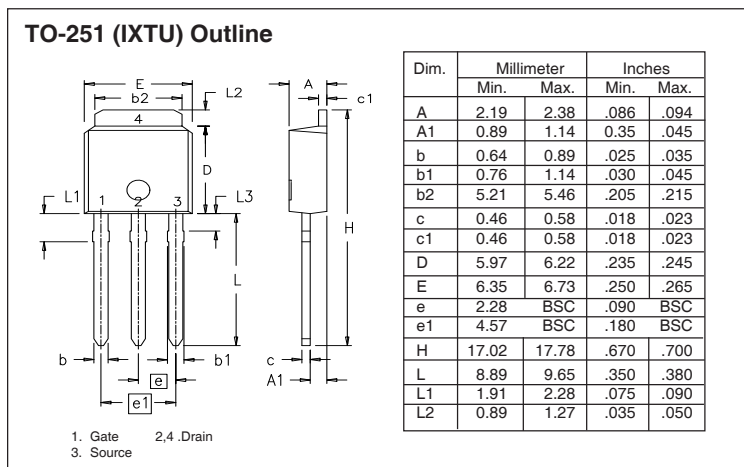


Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 100\text{V}$, $I_D = 100\text{mA}$, Note 1	100	200	mS
C_{iss}	$V_{GS} = -10\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		100	pF
C_{oss}			12	pF
C_{rss}			2	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = \pm 5\text{V}$, $V_{DS} = 50\text{V}$, $I_D = 50\text{mA}$ $R_G = 30\Omega$ (External)		7	ns
t_r			10	ns
$t_{d(off)}$			34	ns
t_f			64	ns
$Q_{g(on)}$	$V_{GS} = \pm 5\text{V}$, $V_{DS} = 500\text{V}$, $I_D = 50\text{mA}$		5.8	nC
Q_{gs}			3.6	nC
Q_{gd}			0.4	nC
R_{thJC}	TO-220			5.0 $^\circ\text{C/W}$
R_{thCS}			0.50	$^\circ\text{C/W}$

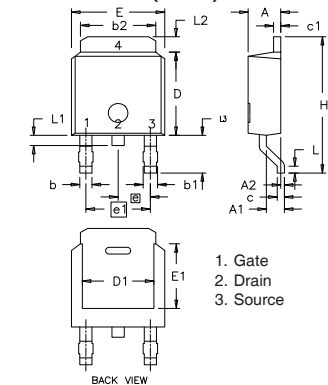
Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{SD}	$I_F = 100\text{mA}$, $V_{GS} = -10\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 750\text{mA}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 25\text{V}$, $V_{GS} = -10\text{V}$			1.5 μs

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

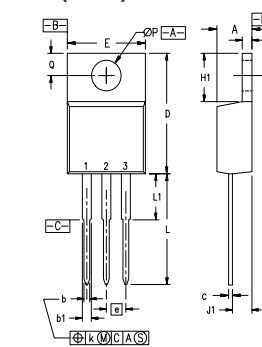


TO-252 AA (IXTY) Outline



Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28	BSC	0.090	BSC
e1	4.57	BSC	0.180	BSC
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

TO-220 (IXTP) Outline



Pins: 1 - Gate 2 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338 B2
by one or more of the following U.S. patents: 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

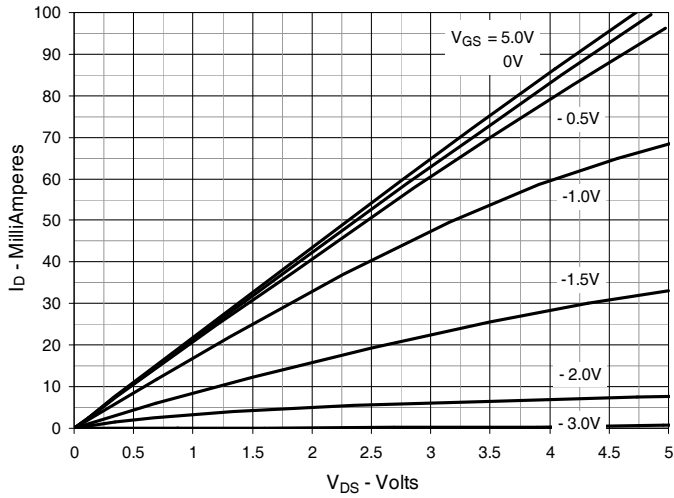


Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

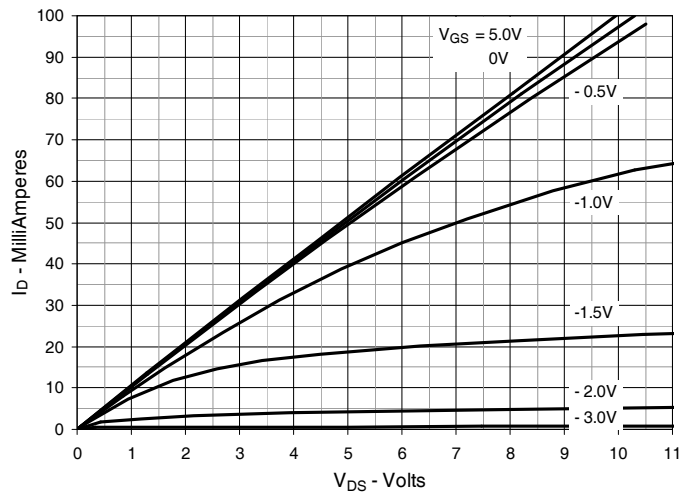


Fig. 3. Drain Current @ $T_J = 25^\circ\text{C}$

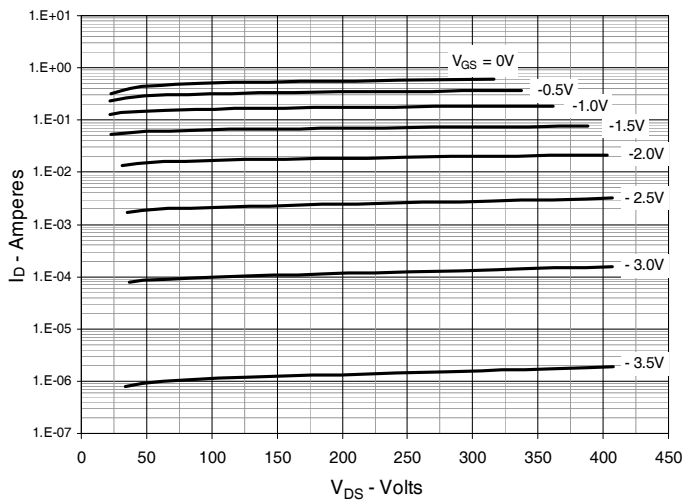


Fig. 4. Drain Current @ $T_J = 100^\circ\text{C}$

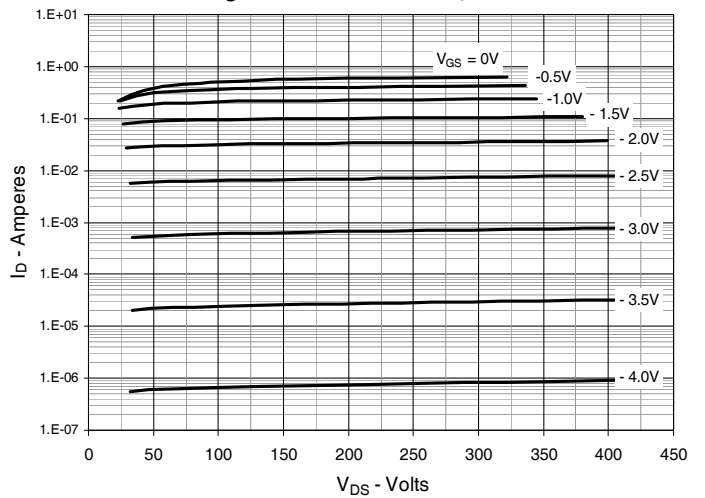


Fig. 5. Dynamic Resistance vs. Gate Voltage

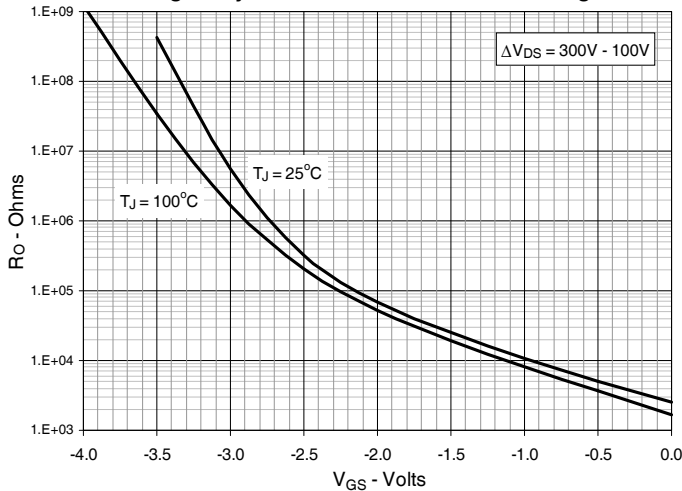


Fig. 6. Normalized $R_{DS(on)}$ vs. Junction Temperature

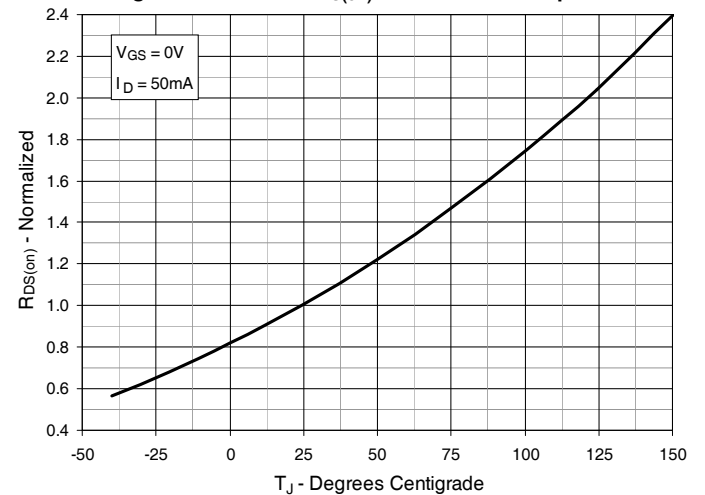


Fig. 7. $R_{DS(on)}$ Normalized to $I_D = 50\text{mA}$ Value vs. Drain Current

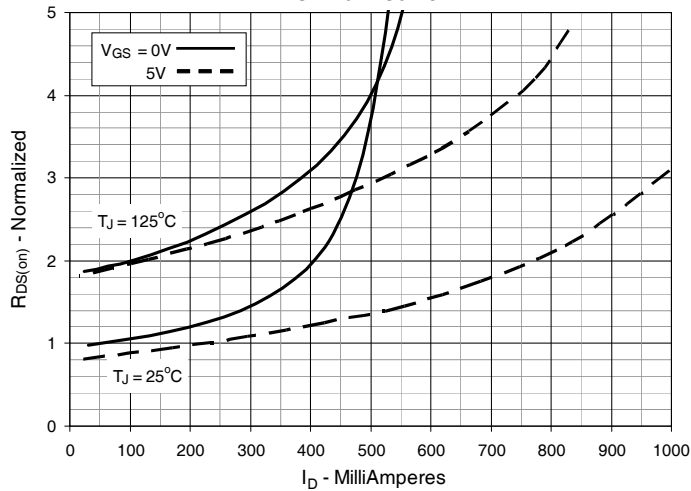


Fig. 8. Input Admittance

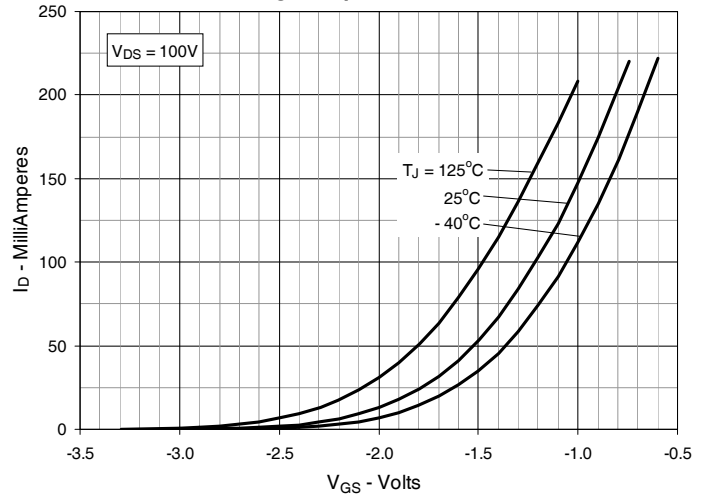


Fig. 9. Transconductance

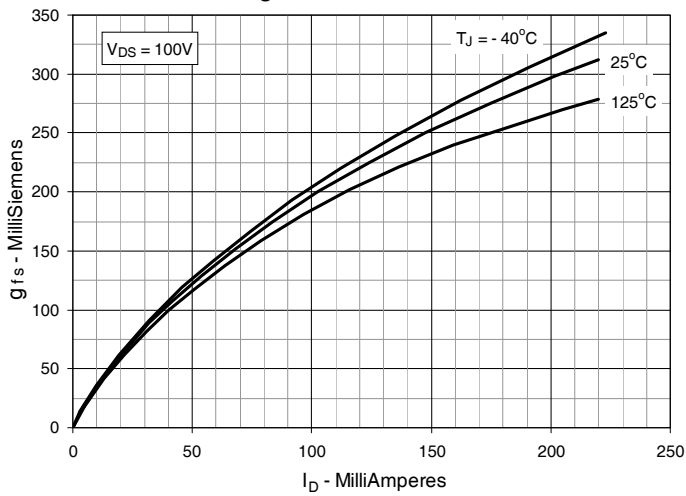


Fig. 10. Forward Voltage Drop of Intrinsic Diode

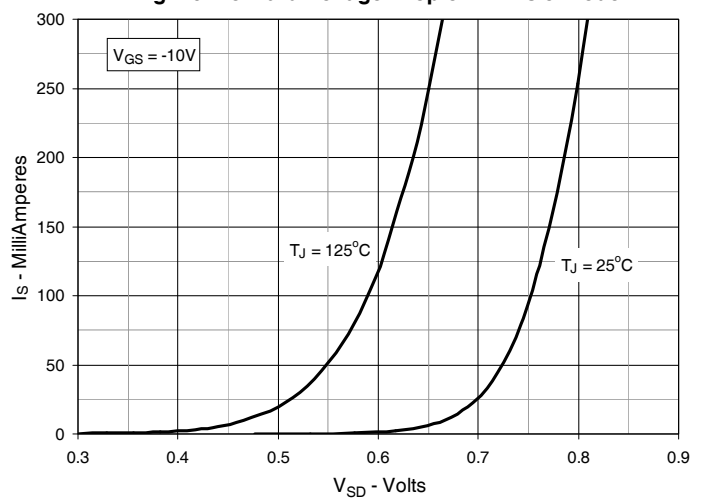


Fig. 11. Capacitance

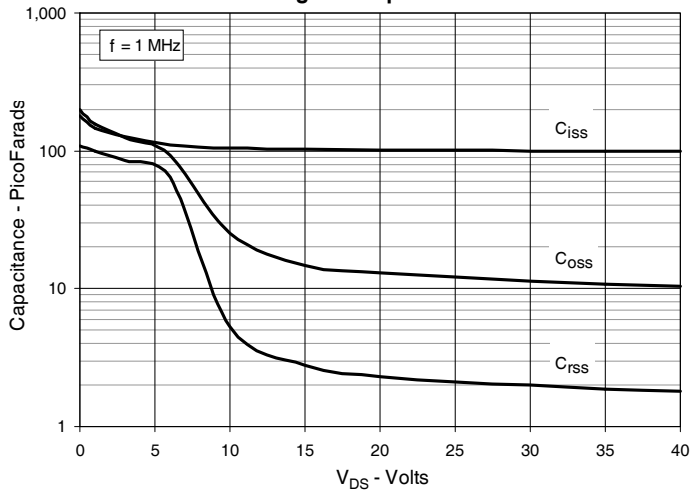


Fig. 12. Gate Charge

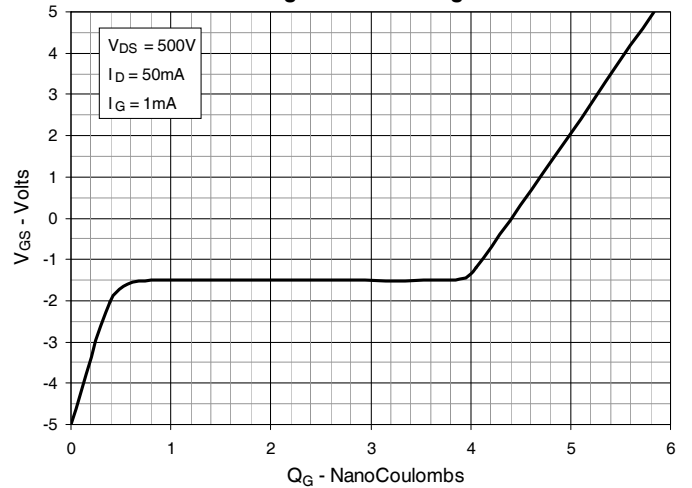


Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$

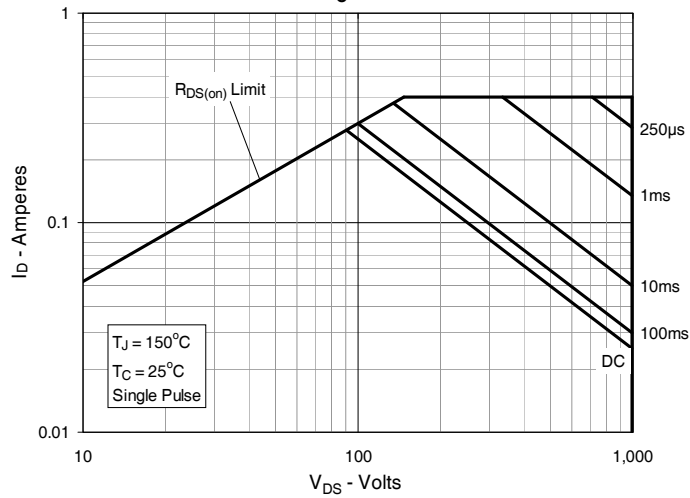


Fig. 14. Forward-Bias Safe Operating Area
@ $T_C = 75^\circ\text{C}$

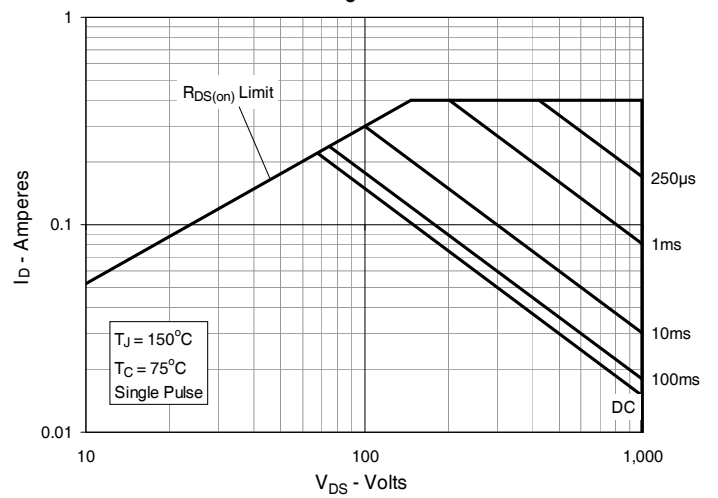


Fig. 15. Maximum Transient Thermal Impedance

