ISP1104

Advanced Universal Serial Bus transceiver

Rev. 02 — 14 October 2003 **Product data**

1. General description

The ISP1104 Universal Serial Bus (USB) transceiver is compliant with the *Universal Serial Bus Specification Rev. 2.0*. The ISP1104 can transmit and receive USB data at full-speed (12 Mbit/s). It allows single and differential input modes selectable by a MODE input.

It allows USB Application Specific Integrated Circuits (ASICs) and Programmable Logic Devices (PLDs) with power supply voltages from 1.65 V to 3.6 V to interface with the physical layer of the USB. It has an integrated 5 V-to-3.3 V voltage regulator for direct powering via the USB supply line V_{BUS}. It has an integrated voltage detector to detect the presence of the V_{BUS} line voltage ($V_{CC(5.0)}$). When V_{BUS} ($V_{CC(5.0)}$) is lost, the D+ and D− pins can be shared with other serial protocols.

The ISP1104 is available in HBCC16 package.

The ISP1104 is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, personal digital assistants and information appliances.

2. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports full-speed (12 Mbit/s) serial data rate
- Integrated 5 V-to-3.3 V voltage regulator for powering via USB line V_{BUS}
- V_{BUS} voltage presence indication on pin VBUSDET
- Used as USB device transceiver or USB transceiver
- Stable RCV output during single-ended zero (SE0) condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports I/O voltage range from 1.65 V to 3.6 V
- ±12 kV ESD protection at pins D+, D-, $V_{CC(5.0)}$ and GND
- Full industrial operating temperature range from −40 °C to +85 °C
- Available in HBCC16 lead-free and halogen-free package.

3. Applications

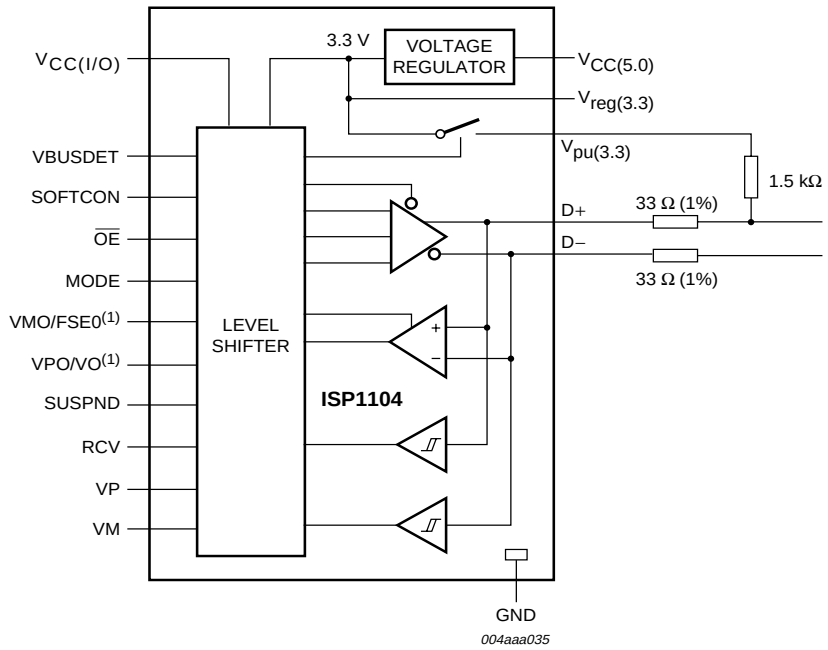
- Portable electronic devices, such as:
  - Mobile phone
  - Digital Still Camera (DSC)
  - Personal Digital Assistant (PDA)
  - Information Appliance (IA).

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1104W	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2

5. Block diagram



(1) Pin function depends on the device function, see Section 7.2.

Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

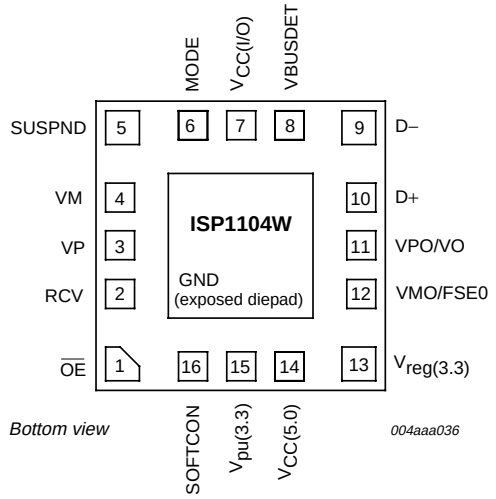


Fig 2. Pin configuration HBCC16.

6.2 Pin description

Table 2: Pin description

Symbol[1]	Pin	Type	Description
$\overline{OE}$	1	I	input for output enable (CMOS level with respect to $V_{CC(I/O)}$, active LOW); enables the transceiver to transmit data on the USB bus input pad; push pull; CMOS
RCV	2	O	differential data receiver output (CMOS level with respect to $V_{CC(I/O)}$); driven LOW when input SUSPND is HIGH; the output state of RCV is preserved and stable during an SE0 condition output pad; push pull; 4 mA output drive; CMOS
VP	3	O	single-ended D+ receiver output (CMOS level with respect to $V_{CC(I/O)}$); for external detection of SE0, error conditions and speed of connected device; driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$ output pad; push pull; 4 mA output drive; CMOS
VM	4	O	single-ended D– receiver output (CMOS level with respect to $V_{CC(I/O)}$); for external detection of SE0, error conditions and speed of connected device; driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$ output pad; push pull; 4 mA output drive; CMOS

Table 2: Pin description *...continued*

Symbol[1]	Pin	Type	Description
SUSPND	5	I	suspend input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level input pad; push pull; CMOS
MODE	6	I	mode input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables the differential input mode (pins VPO and VMO) whereas a LOW level enables a single-ended input mode (pins VO and FSE0); see Table 4 and Table 5 input pad; push pull; CMOS
$V_{CC(I/O)}$	7	-	supply voltage for digital I/O pins (1.65 V to 3.6 V); when $V_{CC(I/O)}$ is not connected, the pins D+ and D– are in three-state; this supply pin is totally independent of $V_{CC(5.0)}$ and $V_{reg(3.3)}$ and must never exceed the $V_{reg(3.3)}$ voltage
VBUSDET	8	O	V_{BUS} indicator output (CMOS level with respect to $V_{CC(I/O)}$); when V_{BUS} > 4.1 V, then VBUSDET = HIGH and when V_{BUS} < 3.6 V, then VBUSDET = LOW output pad; push pull; 4 mA output drive; CMOS
D–	9	AI/O	negative USB data bus connection (analog, differential)
D+	10	AI/O	positive USB data bus connection (analog, differential); connect a 1.5 kΩ resistor to pin $V_{pu(3.3)}$
VPO/VO	11	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger); see Table 4 and Table 5 input pad; push pull; CMOS
VMO/FSE0	12	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger); see Table 4 and Table 5 input pad; push pull; CMOS
$V_{reg(3.3)}$	13	-	regulated supply voltage output (3.0 V to 3.6 V); a decoupling capacitor of at least 0.1 µF is required
$V_{CC(5.0)}$	14	-	supply voltage input (4.0 V to 5.5 V); can be connected directly to the USB supply line V_{BUS}
$V_{pu(3.3)}$	15	-	pull-up supply voltage (3.3 V ± 10 %); connect an external 1.5 kΩ resistor on pin D+ (full-speed); pin function is controlled by input SOFTCON **SOFTCON = LOW —** $V_{pu(3.3)}$ floating (high impedance); ensures zero pull-up current **SOFTCON = HIGH —** $V_{pu(3.3)}$ = 3.3 V; internally connected to $V_{reg(3.3)}$
SOFTCON	16	I	software controlled USB connection input; a HIGH level applies 3.3 V to pin $V_{pu(3.3)}$, which is connected to an external 1.5 kΩ pull-up resistor; this allows USB connect or disconnect signalling to be controlled by software input pad; push pull; CMOS
GND	exposed die pad	-	ground supply; down bonded to the exposed die pad (heatsink); to be connected to the PCB ground

[1] Symbol names with an overscore (for example, $\overline{NAME}$) indicate active LOW signals.

7. Functional description

7.1 Function selection

Table 3: Function table

SUSPND	$\overline{OE}$	D+ and D−	RCV	VP/VM	Function
L	L	driving/ receiving	active	active	normal driving (differential receiver active)
L	H	receiving[1]	active	active	receiving
H	L	driving	inactive[2]	active	driving during 'suspend' (differential receiver inactive)
H	H	high-Z[1]	inactive[2]	active	low-power state

[1] Signal levels on pins D+ and D− are determined by other USB devices and external pull-up or pull-down resistors.

[2] In the suspend mode (pin SUSPND = HIGH), the differential receiver is inactive and the output RCV is always LOW. Out-of-suspend (K) signalling is detected via the single-ended receivers VP and VM.

7.2 Operating functions

Table 4: Driving function using single-ended input data interface (pin $\overline{OE}$ = L and pin MODE = L)

FSE0	VO	Data
L	L	differential logic 0
L	H	differential logic 1
H	L	SE0
H	H	SE0

Table 5: Driving function using differential input data interface (pin $\overline{OE}$ = L and pin MODE = H)

VMO	VPO	Data
L	L	SE0
L	H	differential logic 1
H	L	differential logic 0
H	H	illegal state

Table 6: Receiving function (pin $\overline{OE}$ = H)

D+ and D−	RCV	VP[1]	VM[1]
differential logic 0	L	L	H
differential logic 1	H	H	L
SE0	RCV*[2]	L	L

[1] VP = VM = H indicates the sharing mode ($V_{CC(5.0)}$ is disconnected).

[2] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is stable during the SE0 period.

7.3 Power supply configurations

The ISP1104 can be used with different power supply configurations, which can be changed dynamically. Table 8 provides an overview of power supply configurations.

Normal mode — Both $V_{CC(I/O)}$ and $V_{CC(5.0)}$ are connected. For 5 V operation, $V_{CC(5.0)}$ is connected to a 5 V source (4.0 V to 5.5 V). The internal voltage regulator then produces 3.3 V for USB connections. $V_{CC(I/O)}$ is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.

Disable mode — $V_{CC(I/O)}$ is not connected and $V_{CC(5.0)}$ is connected. In this mode, the internal circuits of the ISP1104 ensure that the D+ and D– pins are in three-state and the power consumption drops to the low-power (suspended) state level. Some hysteresis is built into the detection of $V_{CC(I/O)}$ lost.

Sharing mode — $V_{CC(I/O)}$ is connected and $V_{CC(5.0)}$ < 3.6 V to differentiate between the USB mode and other modes when sharing the V_{BUS}. In this mode, pins D+ and D– are made three-state and the ISP1104 allows external signals of up to 3.6 V to share the D+ and D– lines. The internal circuits of the ISP1104 ensure that virtually no current (maximum 10 μA) is drawn via the D+ and D– lines. The power consumption through pin $V_{CC(I/O)}$ and pin $V_{CC(5.0)}$ drops to the low-power (suspended) state level. Pins VP and VM are driven HIGH and pins VBUSDET and RCV are driven LOW to indicate this mode. Some hysteresis is built into the detection of $V_{CC(5.0)}$ lost.

Table 7: Pin states in disable or sharing mode

Pin	Disable mode	Sharing mode
$V_{CC(5.0)}$	5 V input	<3.6 V
$V_{reg(3.3)}$	3.3 V output	pulled-down
$V_{CC(I/O)}$	not present	1.65 V to 3.6 V input
$V_{pu(3.3)}$	high impedance (off)	high impedance (off)
D+, D–	high impedance	high impedance
VP, VM	invalid[1]	H
RCV	invalid[1]	L
VBUSDET	invalid[1]	L
VPO/VO, VMO/FSE0, MODE, SUSPND, $\overline{OE}$, SOFTCON	high impedance	high impedance

[1] High impedance or driven LOW.

Table 8: Power supply configuration overview

$V_{CC(5.0)}$	$V_{CC(I/O)}$	Configuration	Special characteristics
connected	connected	normal mode	-
connected	not connected	disable mode	D+, D– and $V_{pu(3.3)}$ high impedance; VP, VM, RCV: invalid[1][2]
not connected or <3.6 V	connected	sharing mode	D+, D– and $V_{pu(3.3)}$ high impedance; VP, VM driven HIGH; RCV driven LOW; VBUSDET driven LOW; $V_{reg(3.3)}$ pulled-down

[1] High impedance or driven LOW.

[2] $V_{reg(3.3)}$ may not be operational.

8. Electrostatic discharge (ESD)

8.1 ESD protection

The pins that are connected to the USB connector (D+, D−, $V_{CC(5.0)}$ and GND) have a minimum of ±12 kV ESD protection. The ±12 kV measurement is limited by the test equipment. Capacitors of 4.7 µF connected from $V_{reg(3.3)}$ to GND and $V_{CC(5.0)}$ to GND are required to achieve this ±12 kV ESD protection (see Figure 3).

The ISP1104 can withstand ±12 kV using the Human Body Model and ±5 kV using the Contact Discharge Method as specified in *IEC 61000-4-2*.

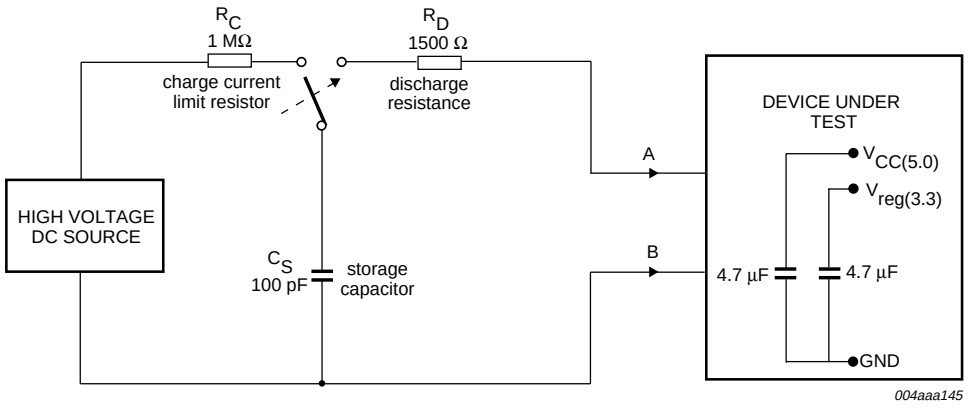


Fig 3. Human Body ESD test model.

8.2 ESD test conditions

A detailed report on test set-up and results is available on request.

9. Limiting values

Table 9: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(5.0)}$	supply voltage			–0.5	+6.0	V
$V_{CC(I/O)}$	I/O supply voltage			–0.5	+4.6	V
V_I	DC input voltage			–0.5	$V_{CC(I/O)}$ + 0.5	V
I_{lu}	latch-up current	V_I = –1.8 V to +5.4 V		-	100	mA
V_{esd}	electrostatic discharge voltage	on pins D+, D–, $V_{CC(5.0)}$ and GND; I_{LI} < 1 µA	[1][2]	–12000	+12000	V
		on other pins; I_{LI} < 1 µA		–2000	+2000	V
T_{stg}	storage temperature			–40	+125	°C

[1] Testing equipment limits measurement to only ±12 kV. Capacitors needed on $V_{CC(5.0)}$ and $V_{reg(3.3)}$ (see Section 8).

[2] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model).

10. Recommended operating conditions

Table 10: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5.0)}$	supply voltage		4.0	5.0	5.5	V
$V_{CC(I/O)}$	I/O supply voltage		1.65	-	3.6	V
V_I	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{I(AI/O)}$	input voltage on AI/O pins	pins D+ and D–	0	-	3.6	V
T_{amb}	ambient temperature		–40	-	+85	°C

11. Static characteristics

Table 11: Static characteristics: supply pins

$V_{CC(5.0)}$ = 4.0 V to 5.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{reg(3.3)}$	regulated supply voltage output	internal regulator option; $I_{load} \leq 300$ µA	[1][2]	3.0	3.3	3.6	V
I_{CC}	operating supply current	transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins D+ and D–	[3]	-	4	8	mA
$I_{CC(I/O)}$	operating I/O supply current	transmitting and receiving at 12 Mbit/s	[3]	-	1	2	mA
$I_{CC(idle)}$	supply current during full-speed idle and SE0	idle: V_{D+} > 2.7 V, V_{D-} < 0.3 V; SE0: V_{D+} < 0.3 V, V_{D-} < 0.3 V	[4]	-	-	500	µA
$I_{CC(I/O)(static)}$	static I/O supply current	idle, SE0 or suspend		-	-	20	µA
$I_{CC(susp)}$	suspend supply current	SUSPND = H	[4]	-	-	100	µA
$I_{CC-I/O(dis)}$	disable current from V_{CC} to $V_{CC(I/O)}$	$V_{CC(I/O)}$ not connected	[4]	-	-	100	µA
$I_{CC(I/O)(sharing)}$	sharing mode I/O supply current	$V_{CC(5.0)}$ not connected		-	-	20	µA

Table 11: Static characteristics: supply pins *...continued*

$V_{CC(5.0)}$ = 4.0 V to 5.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{Dx(sharing)}$	sharing mode load current on pins D+ and D–	$V_{CC(5.0)}$ not connected; SOFTCON = L; V_{Dx} = 3.6 V	-	-	10	µA
$V_{CC(5.0)th}$	supply voltage detection threshold	1.65 V ≤ $V_{CC(I/O)}$ ≤ 3.6 V				
		supply lost	-	-	3.6	V
		supply present	4.1	-	-	V
$V_{CC(5.0)hys}$	supply voltage detection hysteresis	$V_{CC(I/O)}$ = 1.8 V	-	70	-	mV
$V_{CC(I/O)th}$	I/O supply voltage detection threshold	$V_{reg(3.3)}$ = 2.7 V to 3.6 V				
		supply lost	-	-	0.5	V
		supply present	1.4	-	-	V
$V_{CC(I/O)hys}$	I/O supply voltage detection hysteresis	$V_{reg(3.3)}$ = 3.3 V	-	0.45	-	V

[1] I_{load} includes the pull-up resistor current via pin $V_{pu(3.3)}$.

[2] The minimum voltage is 2.7 V in the suspend mode.

[3] Characterized only, not tested in production.

[4] Excluding any load current and $V_{pu(3.3)}$ or V_{sw} source current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typ.).

Table 12: Static characteristics: digital pins

$V_{CC(I/O)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 V to 3.6 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.6V_{CC(I/O)}$	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	$V_{CC(I/O)}$ − 0.15	-	-	V
		I_{OH} = 2 mA	$V_{CC(I/O)}$ − 0.4	-	-	V
Leakage current						
I_{LI}	input leakage current	[1]	–1	-	+1	µA
Capacitance						
C_{IN}	input capacitance	pin to GND	-	-	10	pF
Example 1: $V_{CC(I/O)}$ = 1.8 V ± 0.15 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.5	V
V_{IH}	HIGH-level input voltage		1.2	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V

Table 12: Static characteristics: digital pins...*continued*

$V_{CC(I/O)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	1.5	-	-	V
		I_{OH} = 2 mA	1.25	-	-	V
Example 2: $V_{CC(I/O)}$ = 2.5 V ± 0.2 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.7	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.15	-	-	V
		I_{OH} = 2 mA	1.9	-	-	V
Example 3: $V_{CC(I/O)}$ = 3.3 V ± 0.3 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.9	V
V_{IH}	HIGH-level input voltage		2.15	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.85	-	-	V
		I_{OH} = 2 mA	2.6	-	-	V

[1] If $V_{CC(I/O)} \geq V_{reg(3.3)}$, then the leakage current will be higher than the specified value.

Table 13: Static characteristics: analog I/O pins D+ and D−

$V_{CC(5.0)}$ = 4.0 V to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input levels							
Differential receiver							
V_{DI}	differential input sensitivity	$\|V_{I(D+)} - V_{I(D-)}\|$		0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range		0.8	-	2.5	V
Single-ended receiver							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Output levels							
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to +3.6 V		-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	[1]	2.8	-	3.6	V
Leakage current							
I_{LZ}	OFF-state leakage current			−1	-	+1	µA

Table 13: Static characteristics: analog I/O pins D+ and D–…continued

$V_{CC(5.0)}$ = 4.0 V to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Capacitance							
C_{IN}	transceiver capacitance	pin to GND		-	-	20	pF
Resistance							
Z_{DRV}	driver output impedance	steady-state drive	[2]	34	39	44	Ω
Z_{INP}	input impedance			10	-	-	MΩ
R_{SW}	internal switch resistance at pin $V_{pu(3.3)}$			-	-	10	Ω
Termination							
V_{TERM}	termination voltage for upstream port pull-up (R_{pu})		[3][4]	3.0	-	3.6	V

[1] $V_{OH(min)} = V_{reg(3.3)} - 0.2$ V.

[2] Includes external resistors of 33 Ω ±1 % on both pins D+ and D–.

[3] This voltage is available at pins $V_{reg(3.3)}$ and $V_{pu(3.3)}$.

[4] The minimum voltage is 2.7 V in the suspend mode.

12. Dynamic characteristics

Table 14: Dynamic characteristics: analog I/O pins D+ and D–

$V_{CC(5.0)}$ = 4.0 V to 5.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; see Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
t_{FR}	rise time	C_L = 50 pF to 125 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 4		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF to 125 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 4		4	-	20	ns
FRFM	differential rise/fall time matching (t_{FR}/t_{FF})	excluding the first transition from idle state		90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from idle state; see Figure 5	[1]	1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	driver propagation delay (VPO/VO, VMO/FSE0 to D+, D–)	LOW-to-HIGH; see Figure 5		-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (VPO/VO, VMO/FSE0 to D+, D–)	HIGH-to-LOW; see Figure 5		-	-	18	ns
t_{PHZ}	driver disable delay ($\overline{OE}$ to D+, D–)	HIGH-to-OFF; see Figure 6		-	-	15	ns
t_{PLZ}	driver disable delay ($\overline{OE}$ to D+, D–)	LOW-to-OFF; see Figure 6		-	-	15	ns

Table 14: Dynamic characteristics: analog I/O pins D+ and D–…*continued*

$V_{CC(5.0)}$ = 4.0 V to 5.5 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; see Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}	driver enable delay ($\overline{OE}$ to D+, D–)	OFF-to-HIGH; see Figure 6	-	-	15	ns
t_{PZL}	driver enable delay ($\overline{OE}$ to D+, D–)	OFF-to-LOW; see Figure 6	-	-	15	ns
Receiver timings						
Differential receiver						
$t_{PLH(rcv)}$	propagation delay (D+, D– to RCV)	LOW-to-HIGH; see Figure 7	-	-	15	ns
$t_{PHL(rcv)}$	propagation delay (D+, D– to RCV)	HIGH-to-LOW; see Figure 7	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	propagation delay (D+, D– to VP, VM)	LOW-to-HIGH; see Figure 7	-	-	18	ns
$t_{PHL(se)}$	propagation delay (D+, D– to VP, VM)	HIGH-to-LOW; see Figure 7	-	-	18	ns

[1] Characterized only, not tested. Limits guaranteed by design.

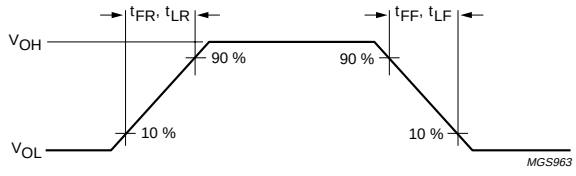


Fig 4. Rise and fall times.

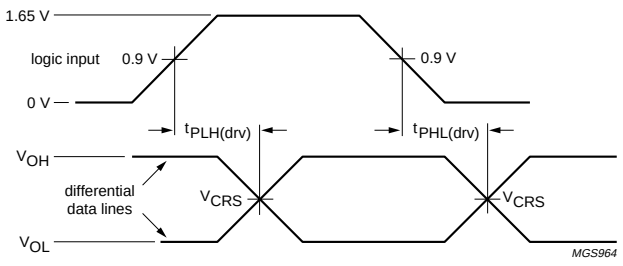


Fig 5. Timing of VPO/VO and VMO/FSE0 to D+ and D–.

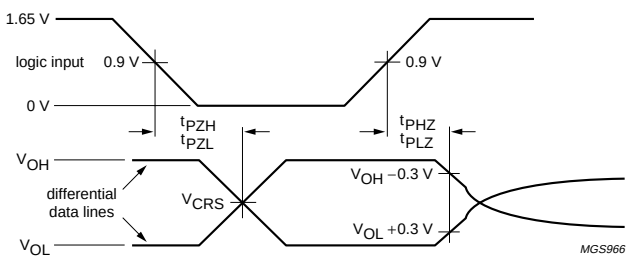


Fig 6. Timing of $\overline{OE}$ to D+ and D–.

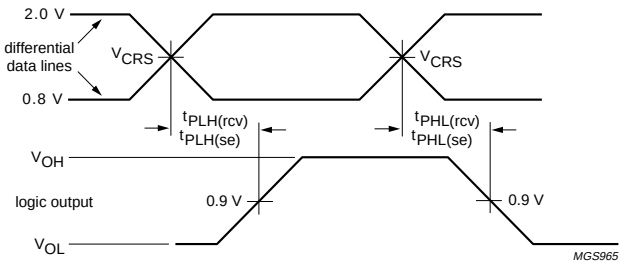
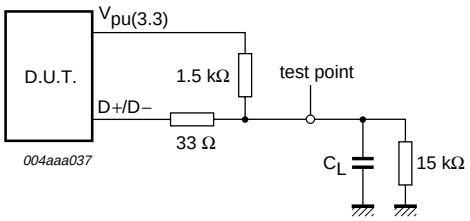


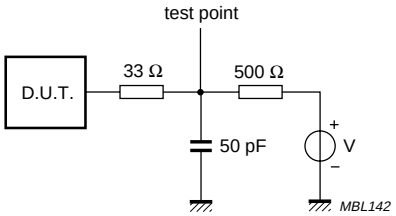
Fig 7. Timing of D+ and D– to RCV, VP and VM.

13. Test information



Load capacitance C_L = 50 pF (minimum or maximum timing).

Fig 8. Load on pins D+ and D−.



V = 0 V for t_{PZH} and t_{PHZ}.

V = $V_{reg(3.3)}$ for t_{PZL} and t_{PLZ}.

Fig 9. Load on pins D+ and D− for enable and disable times.

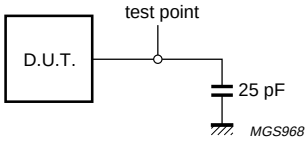
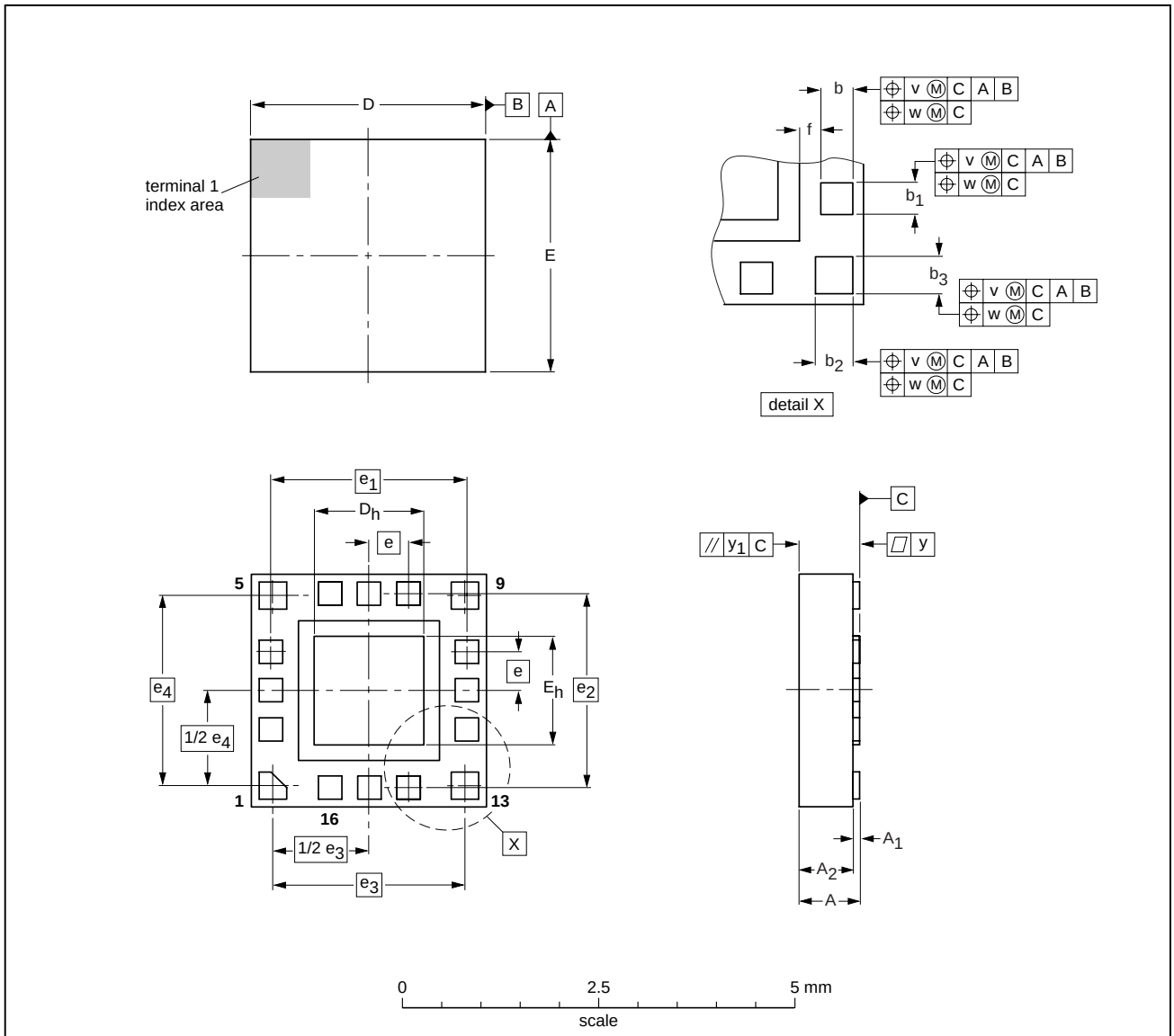


Fig 10. Load on pins VM, VP and RCV.

14. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm **SOT639-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	f	v	w	y	y_1
mm	0.8	0.10 0.05	0.7 0.6	0.33 0.27	0.33 0.27	0.38 0.32	0.38 0.32	3.1 2.9	1.45 1.35	3.1 2.9	1.45 1.35	0.5	2.5	2.5	2.45	2.45	0.23 0.17	0.08	0.1	0.05	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT639-2		MO-217				01-11-13 03-03-12

Fig 11. HBCC16 package outline.

15. Packaging

The ISP1104W (HBCC16 package) is delivered on a type A carrier tape, see Figure 12. The tape dimensions are given in Table 15.

The reel diameter is 330 mm. The reel is made of polystyrene (PS) and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is ±0.02 mm. The camber must not exceed 1 mm in 100 mm.

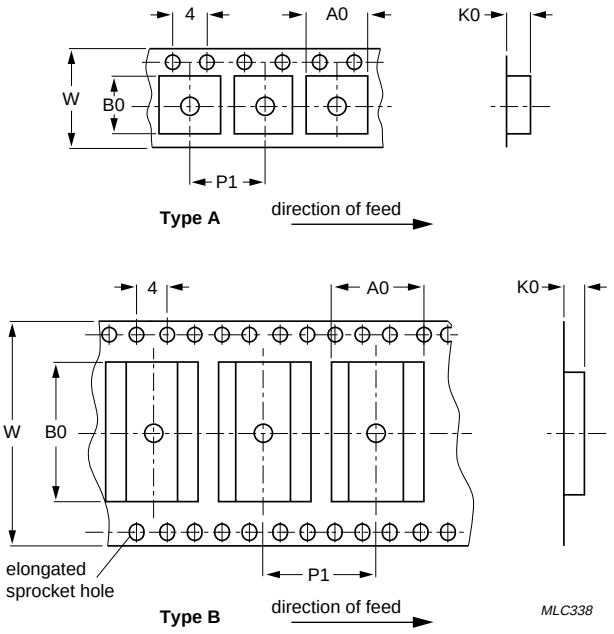


Fig 12. Carrier tape dimensions.

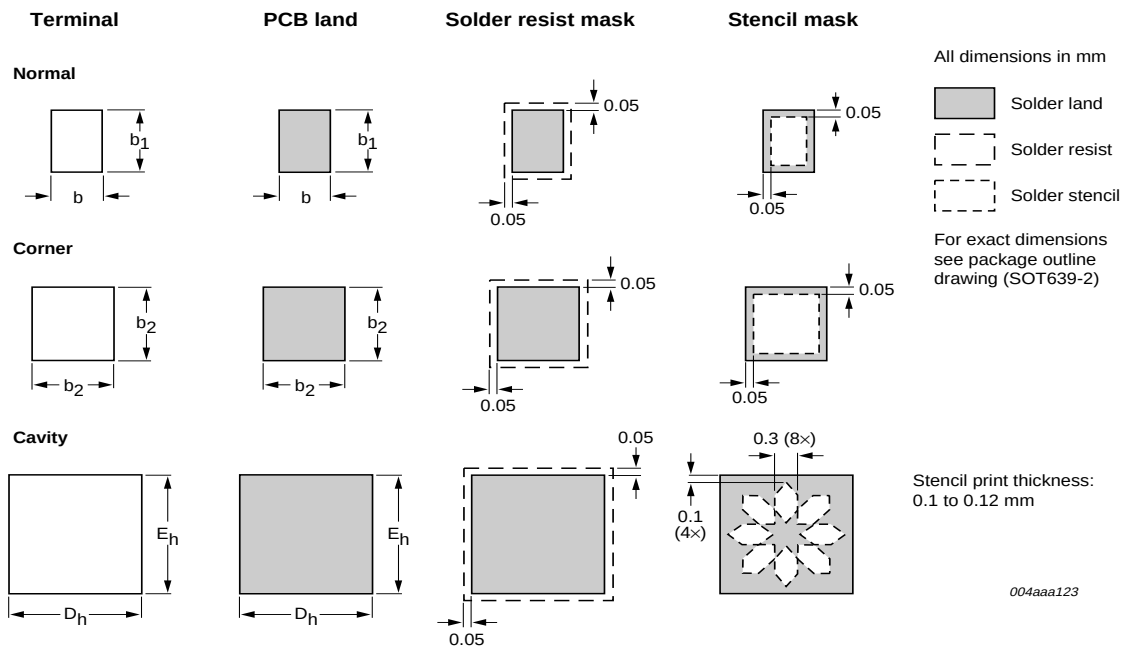
Table 15: Type A carrier tape dimensions for the ISP1104W

Dimension	Value	Unit
A0	3.3	mm
B0	3.3	mm
K0	1.1	mm
P1	8.0	mm
W	12.0 ± 0.3	mm

16. Additional soldering information

16.1 (H)BCC packages: footprint

The surface material of the terminals on the resin protrusion consists of a 4-layer metal structure (Au, Pd, Ni and Pd). The Au + Pd layer (0.1 µm min.) ensures solderability, the Ni layer (5 µm min.) prevents diffusion, and the Pd layer on top (0.5 µm min.) ensures effective wire bonding.



Cavity: exposed die pad, either functioning as heatsink or as ground connection; only for HBCC packages.

Fig 13. (H)BCC footprint and solder resist mask dimensions.

16.2 (H)BCC packages: reflow soldering profile

The conditions for reflow soldering of (H)BCC packages are as follows:

- **Preheating time**: minimum 90 s at T = 145 to 155 °C
- **Soldering time**: minimum 90 s (BCC) or minimum 100 s (HBCC) at T > 183 °C
- **Peak temperature**:
  - Ambient temperature: $T_{amb(max)}$ = 260 °C
  - Device surface temperature: $T_{case(max)}$ = 255 °C.

17. Revision history

Table 16: Revision history

Rev	Date	CPCN	Description
02	20031014	-	**Product data (9397 750 11229)** Modifications: • Changed USB 1.1 reference to USB 2.0; also added data transfer rates • Section 2: updated • Figure 1, Figure 8 and Figure 9: removed the figure note on 33 Ω • Table 2: updated the description for pin 8; added pad details • Section 7.3 sharing mode: updated the first sentence • Table 8: updated • Table 9: added a table note • Table 11: changed $I_{CC(dis)}$ to $I_{CC-I/O(dis)}$; also, changed the description • Table 13: removed Z_{DRV2}, and also the relevant (old) table note 3.
01	20020826	-	**Product data (9397 750 09784)**

18. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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