Pin Description

16XCLK - Positive edge triggered input clock that is set to 16 times the data transmission baud rate. The encode and decode schemes require this signal. The signal is usually tied to a UART's BAUDOUT signal.

TXD - Negative edge triggered input signal; usually tied to a UART's SOUT signal (serial data to be transmitted).

RCV - Output signal which is usually tied to a UART's SIN signal (received serial data).

GND - Chip ground.

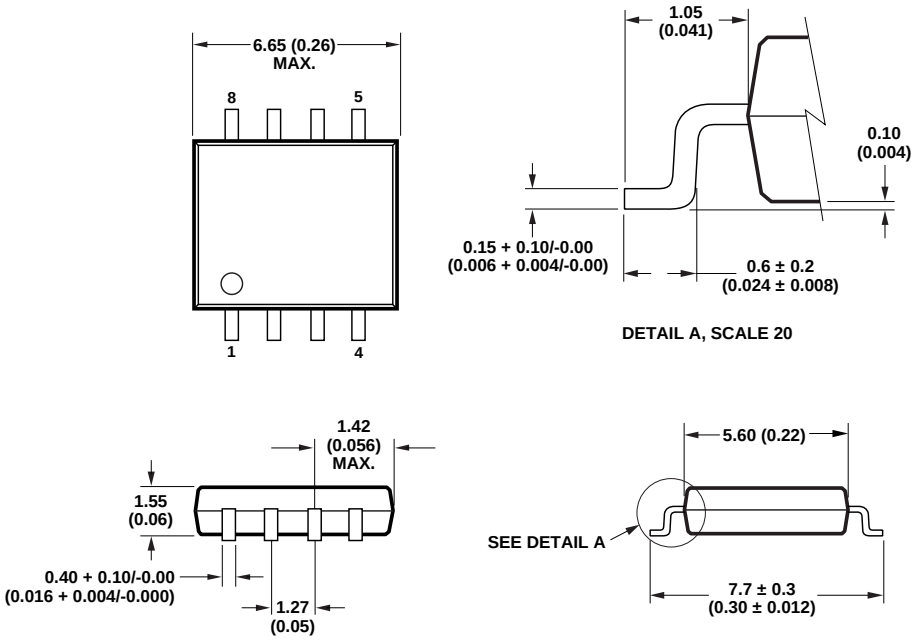
NRST - Active low signal used to reset the decode state machine. This signal can be tied to POR (Power on reset) or V_{CC}. This signal can also be used to disable any data reception.

IR_RCV - A 3/16th pulse width input signal from the infrared transceiver. The signal is a demodulated (pulse stretched) to generate the RCV output signal.

IR_TXD - This signal is the modulated 3/16ths TXD signal which is input to the infrared transceiver.

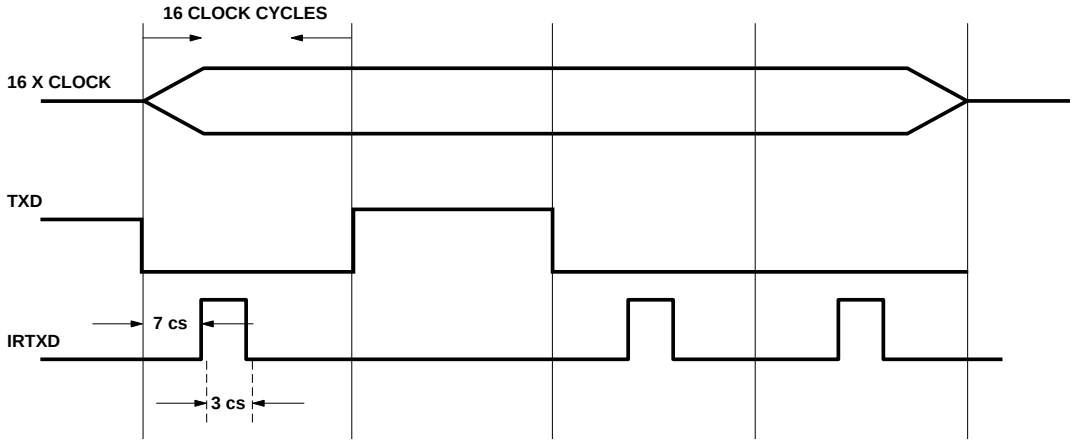
V_{CC} - Power.

Package Dimensions



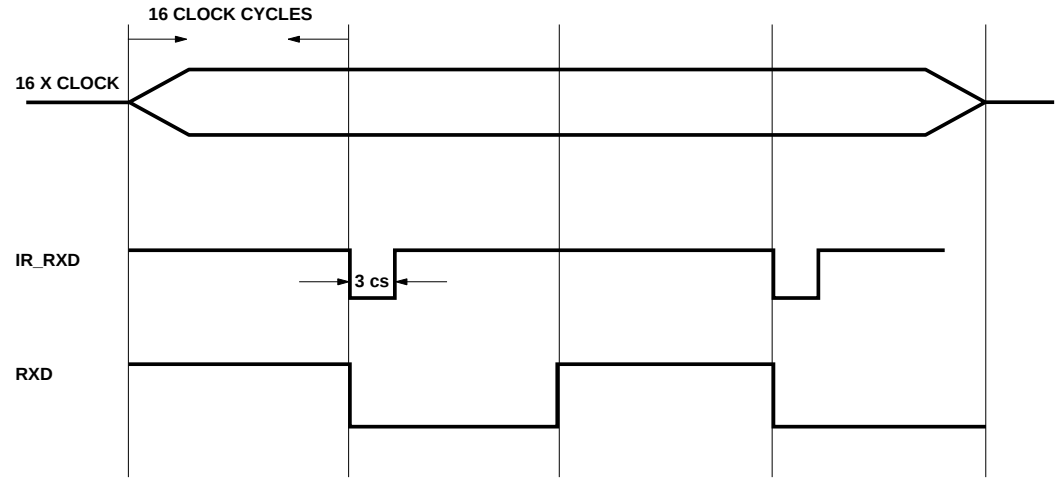
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Encoding Scheme



The encoder sends a pulse for every space or “0” that is sent on the TXD line. On a high to low transition of the TXD line, the generation of the pulse is delayed for 7 clock cycles of the 16XCLK before the pulse is set high for 3 clock cycles (or 3/16th of a bit time) and then subsequently pulled low.

Decoding Scheme



A high to low transition of the IR_RXD line from the infrared transceiver module signifies a 3/16th pulse. This pulse is stretched to accommodate 1 bit time (16 clock cycles). Every pulse that is received is translated into a “0” or space on the RXD line equal to 1 bit time.

Note: The stretched pulse must be at least 3/4 of a bit time in duration to be correctly interpreted by a UART.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	T_S	-65	+150	℃	
Operating Temperature	T_A	-40	+85	℃	
Output Current	I_O		10	mA	
Power Dissipation	P_{MAX}		0.22	W	
Input/Output Voltage	V_I/V_O	-0.5	V_{CC} + 0.5	V	
Power Supply Voltage	V_{CC}	-0.5	+6.5	V	

Switching Specifications

(V_{CC} = 5 Volts ± 10%, T_A= -40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Toggle Frequency	f_{tog}		120		Mhz	
Propagation Delay Time	t_{pd}		0.5 1.0 2.0		ns ns ns	Internal Gate Input Buffer Output Buffer
Output Fall Time	t_f		1.42		ns	Output Buffer (C_L = 15 pF)
Output Rise Time	t_r		1.54		ns	Output Buffer (C_L = 15 pF)

Note: f_{tog} represents the maximum internal D-Type Flip Flop toggle rate

Capacitance

(V_{CC} = 0 Volts, T_A= -40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Capacitance	C_{IN}		10	20	pF	f = 1 MHz - Unmeasured Pins Returned to 0 Volts
Output Capacitance	C_{OUT}		10	20	pF	
Output Fall Time			10	20	pF	

Recommended Operating Conditions

(T_A= -40 to +85°C)

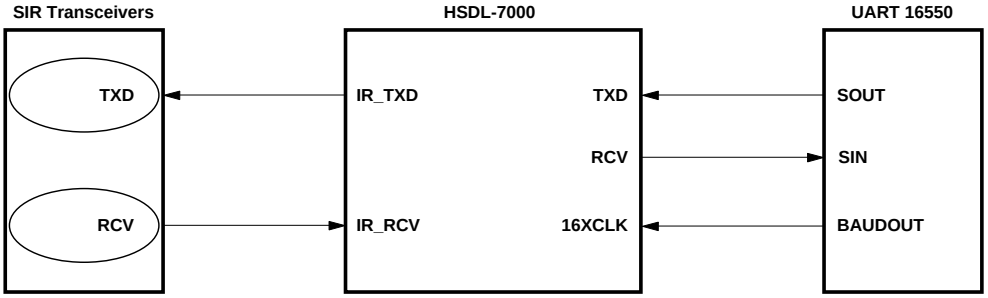
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	CMOS level
Input Voltage	V_I	0.0		V_{CC}	V	CMOS level
Ambient Temperature	T_A	-40		+85	°C	CMOS level
High Level Input Voltage	V_{IH}	0.7 V_{CC}		V_{CC}	V	CMOS level
Low Level Input Voltage	V_{IL}	0.0		0.3 V_{CC}	V	CMOS level
Positive Trigger Voltage	V_P	1.61		4.00	V	CMOS level
Negative Trigger Voltage	V_N	0.55		3.10	V	CMOS level
Hysteresis Voltage	V_H	0.50		2.00	V	CMOS level
Power Dissipation	P_{DISS}		4.9	220	mW	f_{16XCLK} = 2 MHz
Input Rise Time	t_{ri}			200	ns	f_{16XCLK} = 2 MHz
Input Fall Time	t_{fa}			200	ns	f_{16XCLK} = 2 MHz
Max Clk Frequency (16XCLK)	f_{16XCLK}			2	MHz	
Minimum Pulse Width (IR_TXD)*	t_{mpx}	250			ns	f_{16XCLK} = 2 MHz

*IrDA Parameters. The Max Clk Frequency represents the maximum clock frequency to drive the HSDL-7000's internal state machine. Under normal circumstances, this clock input should not exceed 16 * 115.2 Kbp/s or 1.8432 MHz. This product can operate at higher clock rates, but the above is the recommended rate.

The Minimum Pulse Width represents the minimum pulse width of the encoded IR_TXD pulse (and the IR_RCV pulse). As per the IrDA specifications, the minimum pulse width of the IR_TXD and IR_RCV pulses should be 3 * (1/1.8432 MHz) or 1.63 µs. The minimum pulse width specified for the HSDL-7000 is 250 ns, which is within IrDA specification. Under normal circumstances, the pulse width should not be less than 1.63 µs.

Application Circuits

HSDL-7000 Connection to UART



At the time of this publication, Light Emitting Diodes (LEDs) that are contained in this product are regulated for eye safety in Europe by the Commission for European Electrotechnical Standardization (CENELEC) EN60825-1. Please refer to Application Brief I-008 for more information.

For company and product information, please go to our web site: **WWW.liteon.com** or
http://optodatabook.liteon.com/databook/databook.aspx