Application Diagrams

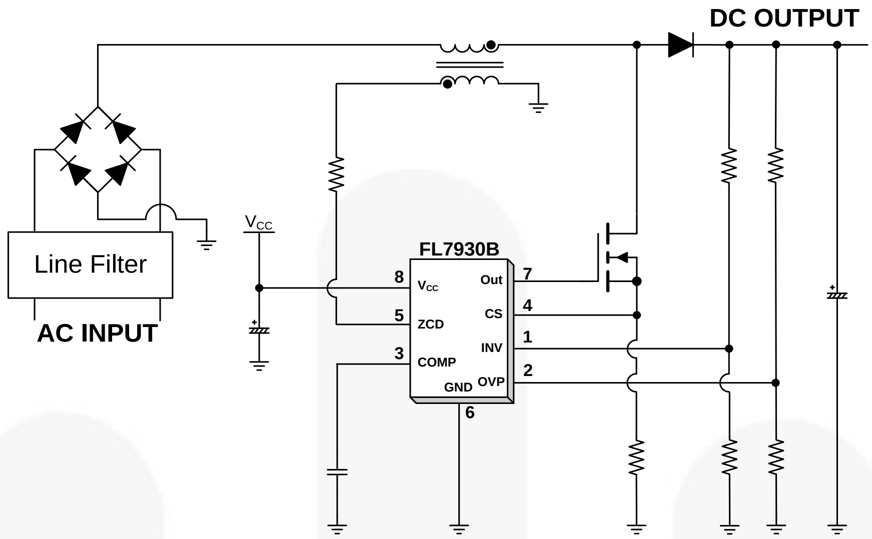

Figure 1. Typical Boost PFC Application for FL7930B

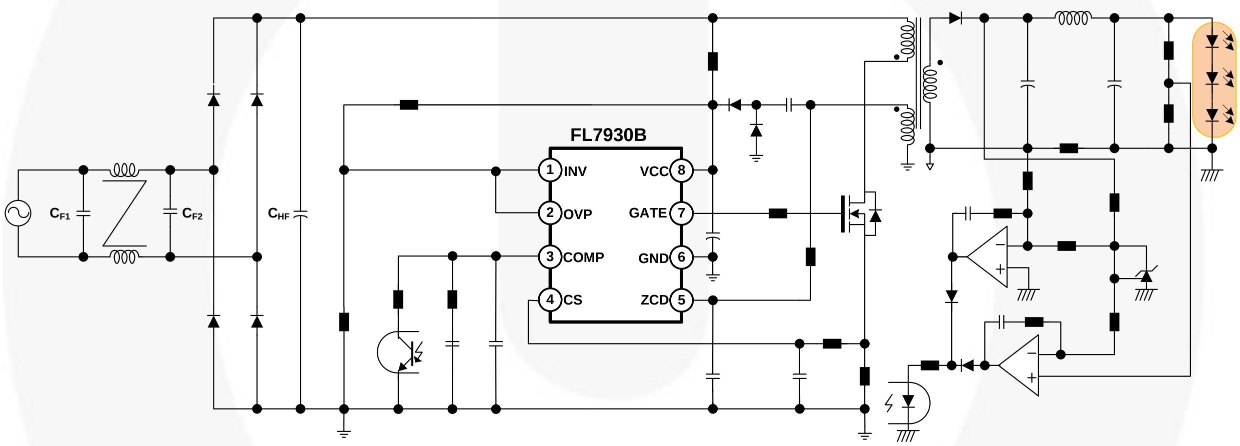

Figure 2. Typical Application of Single-Stage Flyback Converter for FL7930B

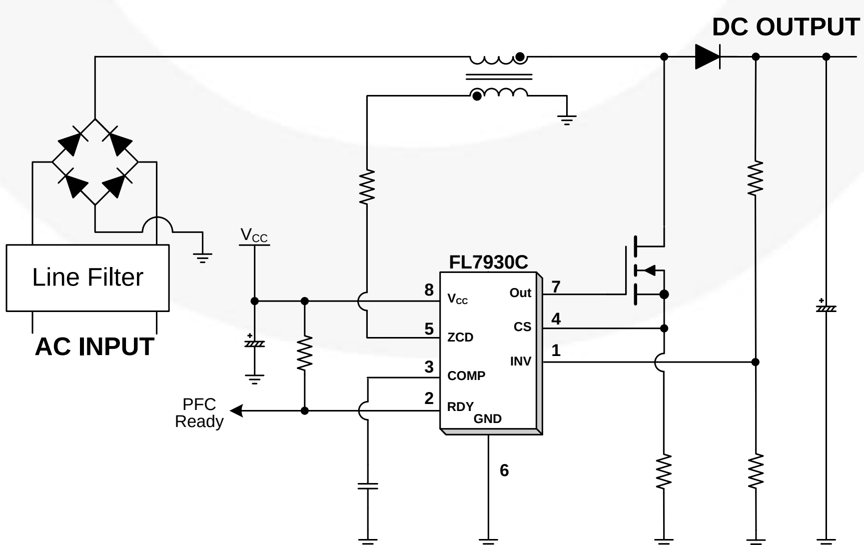

Figure 3. Typical Boost PFC Application for FL7930C

Internal Block Diagram

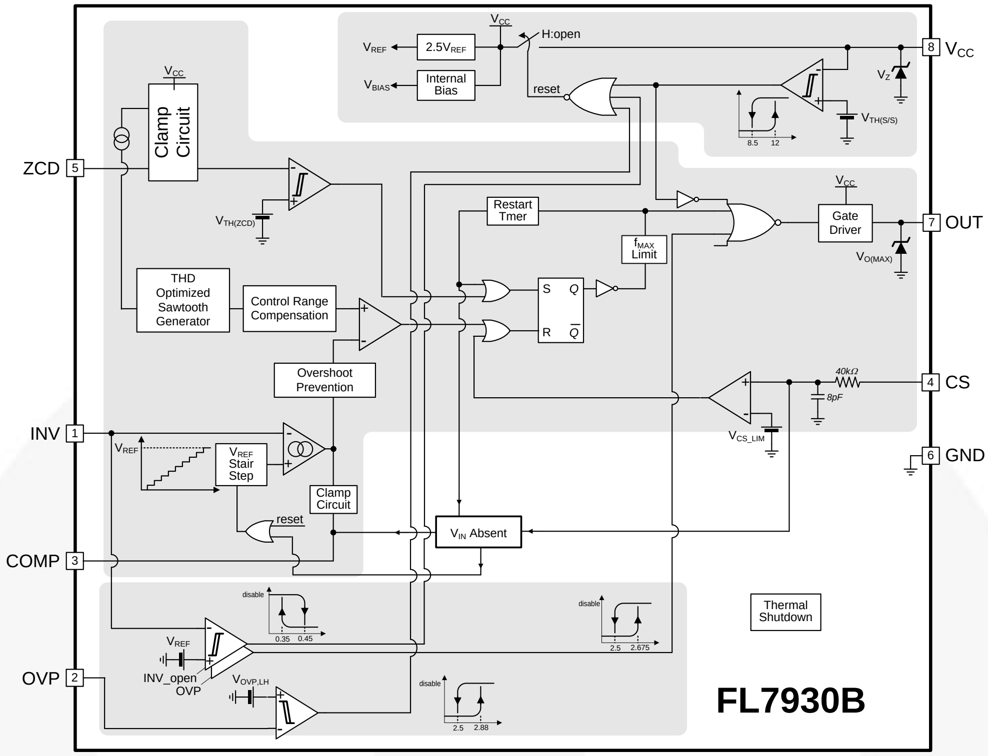

Figure 4. Functional Block Diagram for FL7930B

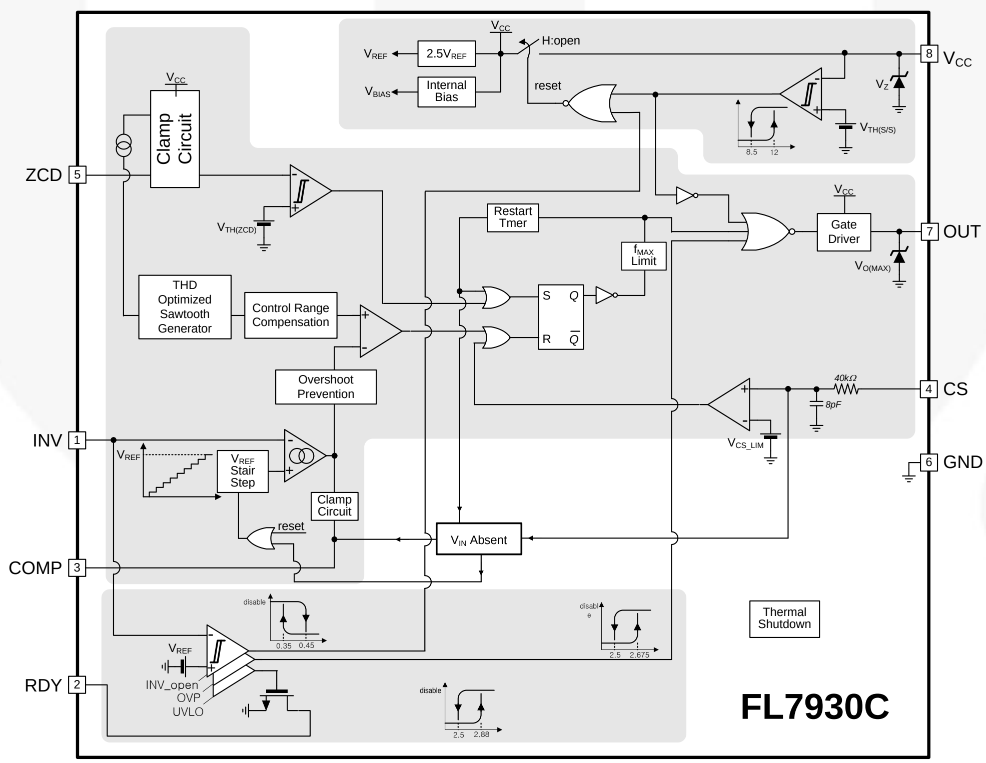

Figure 5. Functional Block Diagram for FL7930C

Pin Configuration

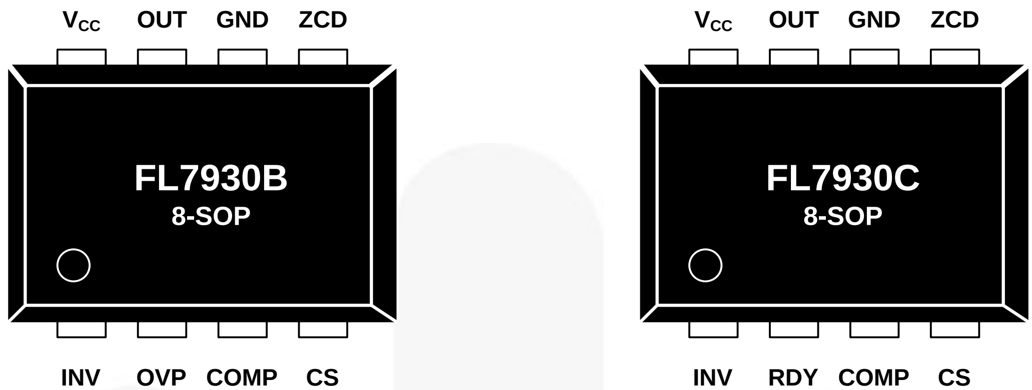

Figure 6. Pin Configurations (Top View)

Pin Definitions

Pin #	Name	Description
1	INV	This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5 V.
2	OVP	**FL7930B**: This pin is used to detect PFC output over-voltage when INV pin information is not correct.
	RDY	**FL7930C**: This pin is used to detect PFC output-voltage reaching a pre-determined value. When output voltage reaches 89% of rated output voltage, this pin is pulled HIGH, which is an (open-drain) output type.
3	COMP	This pin is the output of the transconductance error amplifier. Components for the output voltage compensation should be connected between this pin and GND.
4	CS	This pin is the input of the over-current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise.
5	ZCD	This pin is the input of the zero-current detection block. If the voltage of this pin goes higher than 1.5 V, then goes lower than 1.4 V, the MOSFET is turned on.
6	GND	This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
7	OUT	This pin is the gate drive output. The peak sourcing and sinking current levels are +500 mA and -800mA, respectively. For proper operation, the stray inductance in the gate driving path must be minimized.
8	VCC	This is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage			V_Z	V
I_{OH}, I_{OL}	Peak Drive Output Current		-800	+500	mA
I_{CLAMP}	Driver Output Clamping Diodes V_O>V_{CC} or V_O<-0.3 V		-10	+10	mA
I_{DET}	Detector Clamping Diodes		-10	+10	mA
V_{IN}	Error Amplifier Input, Output, OVP Input, ZCD, RDY, and OVP Pins[1]		-0.3	8.0	V
	CS Input Voltage[2]		-10	6	
T_J	Operating Junction Temperature			+150	°C
T_A	Operating Temperature Range		-40	+125	°C
T_{STG}	Storage Temperature Range		-65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		2.5	kV
		Charged Device Model, JESD22-C101		2.0	

Notes:
1. When this pin is supplied by external power sources by accident, its maximum allowable current is 50 mA.
2. In case of DC input, acceptable input range is -0.3 V~6 V: within 100 ns -10 V~6 V is acceptable, but electrical specifications are not guaranteed during such a short time.

Thermal Impedance

Symbol	Parameter	Min.	Max.	Unit
Θ_{JA}	Thermal Resistance, Junction-to-Ambient[3]	150		°C/W

Note:
3. Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

Electrical Characteristics

V_{CC} = 14 V, T_A = -40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC} Section						
V_{START}	Start Threshold Voltage	V_{CC} Increasing	11	12	13	V
V_{STOP}	Stop Threshold Voltage	V_{CC} Decreasing	7.5	8.5	9.5	V
HY_{UVLO}	UVLO Hysteresis		3.0	3.5	4.0	V
V_Z	Zener Voltage	I_{CC}=20 mA	20	22	24	V
V_{OP}	Recommended Operating Range		13		20	V
Supply Current Section						
I_{START}	Startup Supply Current	V_{CC}=V_{START}-0.2 V		120	190	µA
I_{OP}	Operating Supply Current	Output Not Switching		1.5	3.0	mA
I_{DOP}	Dynamic Operating Supply Current	50 kHZ, C_I=1 nF		2.5	4.0	mA
I_{OPDIS}	Operating Current at Disable	V_{INV}=0 V	90	160	230	µA
Error Amplifier Section						
V_{REF1}	Voltage Feedback Input Threshold1	T_A=25°C	2.465	2.500	2.535	V
ΔV_{REF1}	Line Regulation	V_{CC}=14 V~20 V		0.1	10.0	mV
ΔV_{REF2}	Temperature Stability of V_{REF1}[4]			20		mV
$I_{EA,BS}$	Input Bias Current	V_{INV}=1 V~4 V	-0.5		0.5	µA
$I_{EAS,SR}$	Output Source Current	V_{INV}=V_{REF} -0.1 V		-12		µA
$I_{EAS,SK}$	Output Sink Current	V_{INV}=V_{REF} +0.1 V		12		µA
V_{EAH}	Output Upper Clamp Voltage	V_{INV}=1 V, V_{CS}=0 V	6.0	6.5	7.0	V
V_{EAZ}	Zero Duty Cycle Output Voltage		0.9	1.0	1.1	V
g_m	Transconductance[4]		90	115	140	µmho
Maximum On-Time Section						
$t_{ON,MAX1}$	Maximum On-Time Programming 1	T_A=25°C, V_{ZCD}=1 V	35.5	41.5	47.5	µs
$t_{ON,MAX2}$	Maximum On-Time Programming 2	T_A=25°C, I_{ZCD}=0.469 mA	11.2	13.0	14.8	µs
Current-Sense Section						
V_{CS}	Current-Sense Input Threshold Voltage Limit		0.7	0.8	0.9	V
$I_{CS,BS}$	Input Bias Current	V_{CS}=0 V~1 V	-1.0	-0.1	1.0	µA
$t_{CS,D}$	Current-Sense Delay to Output[4]	dV/dt=1 V/100 ns, from 0 V to 5 V		350	500	ns

Continued on the following page…

Electrical Characteristics

V_{CC} = 14 V, T_A = -40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Zero-Current Detect Section						
V_{ZCD}	Input Voltage Threshold(4)		1.35	1.50	1.65	V
HY_{ZCD}	Detect Hysteresis(4)		0.05	0.10	0.15	V
V_{CLAMPH}	Input High Clamp Voltage	I_{DET}=3 mA	5.5	6.2	7.5	V
V_{CLAMPL}	Input Low Clamp Voltage	I_{DET}= -3 mA	0	0.65	1.00	V
$I_{ZCD,BS}$	Input Bias Current	V_{ZCD}=1 V~5 V	-1.0	-0.1	1.0	µA
$I_{ZCD,SR}$	Source Current Capability(4)	T_A=25°C			-4	mA
$I_{ZCD,SK}$	Sink Current Capability(4)	T_A=25°C			10	mA
$t_{ZCD,D}$	Maximum Delay From ZCD to Output Turn-On(4)	dV/dt=-1 V/100 ns, 5 V to 0 V	100		200	ns
Output Section						
V_{OH}	Output Voltage High	I_O=-100 mA, T_A=25°C	9.2	11.0	12.8	V
V_{OL}	Output Voltage Low	I_O=200 mA, T_A=25°C		1.0	2.5	V
t_{RISE}	Rising Time(4)	C_{IN}=1 nF		50	100	ns
t_{FALL}	Falling Time(4)	C_{IN}=1 nF		50	100	ns
$V_{O,MAX}$	Maximum Output Voltage	V_{CC}=20 V, I_O=100 µA	11.5	13.0	14.5	V
$V_{O,UVLO}$	Output Voltage with UVLO Activated	V_{CC}=5 V, I_O=100 µA			1	V
Restart / Maximum Switching Frequency Limit Section						
t_{RST}	Restart Timer Delay		50	150	300	µs
f_{MAX}	Maximum Switching Frequency(4)		250	300	350	kHz
RDY Pin (FL7930C Only)						
$I_{RDY,SK}$	Output Sink Current		1	2	4	mA
$V_{RDY,SAT}$	Output Saturation Voltage	$I_{RDY,SK}$=2 mA		320	500	mV
$I_{RDY,LK}$	Output Leakage Current	Output High Impedance			1	µA
Soft-Start Timer Section						
t_{SS}	Internal Soft-Soft(4)		3	5	7	ms
Protections						
$V_{OVP,INV}$	OVP Threshold Voltage at INV Pin	T_A=25°C	2.620	2.675	2.730	V
$HY_{OVP,INV}$	OVP Hysteresis at INV Pin	T_A=25°C	0.120	0.175	0.230	V
$V_{OVP,OVP}$	OVP Threshold Voltage at OVP Pin (FL7930B Only)	T_A=25°C	2.740	2.845	2.960	V
$HY_{OVP,OVP}$	OVP Hysteresis at OVP Pin (FL7930B Only)	T_A=25°C		0.345		V
V_{EN}	Enable Threshold Voltage		0.40	0.45	0.50	V
HY_{EN}	Enable Hysteresis		0.05	0.10	0.15	V
T_{SD}	Thermal Shutdown Temperature(4)		125	140	155	°C
T_{HYS}	Hysteresis Temperature of TSD(4)			60		°C

Note:

4. These parameters, although guaranteed by design, are not production tested.

Comparison of FL6961, FL7930B, and FL7930C

Function	FL6961	FL7930B	FL7930C	Advantages
OVP Pin	None	**Integrated**	None	▪ No External Circuit for Additional OVP ▪ Reduced Power Loss and BOM Cost Due to Additional OVP Circuit
PFC Ready Pin	None	None	**Integrated**	▪ No External Circuit for PFC Output UVLO ▪ Reduced Power Loss and BOM Cost Due to PFC Out UVLO Circuit ▪ Versatile Open-Drain Pin
Frequency Limit	None	**Integrated**	**Integrated**	▪ Abnormal CCM Operation Prohibited ▪ Abnormal Inductor Current Accumulation Can Be Prohibited
AC Absent Detection	None	**Integrated**	**Integrated**	▪ Increased System Reliability with AC On-Off Test ▪ Guaranteed Stable Operation at Short Electric Power Failure
Soft-Start and Startup without Overshoot	None	**Integrated**	**Integrated**	▪ Reduced Voltage and Current Stress at Startup ▪ Eliminates Audible Noise due to Unwanted OVP Triggering
Control Range Compensation	None	**Integrated**	**Integrated**	▪ Can Avoid Burst Operation at Light Load and High Input Voltage ▪ Reduced Probability of Audible Noise Due to the Burst Operation
THD Optimizer	External	**Internal**	**Internal**	▪ No External Resistor is Needed
TSD	None	**Integrated**	**Integrated**	▪ Stable and Reliable TSD Operation ▪ Converter Temperature Range Limited Range

Comparison of FL7930B and FL7930C

Function	FL7930B	FL7930C	Remark
RDY Pin	None	Integrated	▪ User Choice for the Use of Pin #2 FL7930B: OVP FL7930C: RDY
OVP Pin	Integrated	None	
Control Range Compensation	Integrated	Integrated	

Typical Performance Characteristics

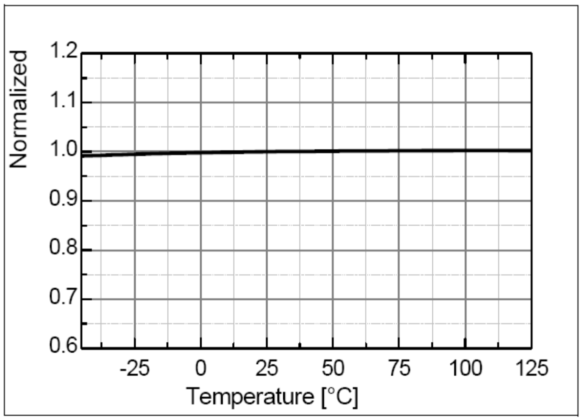

Figure 7. Voltage Feedback Input Threshold 1 (V_{REF1}) vs. T_A

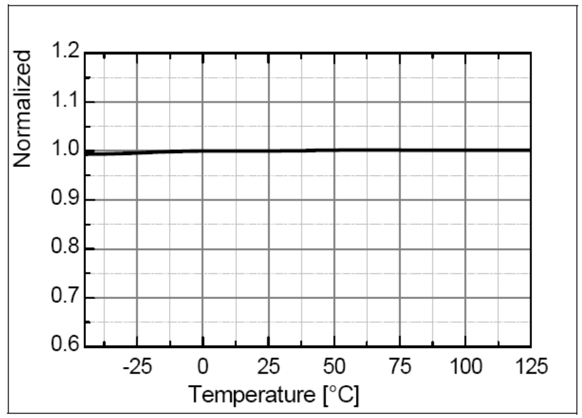

Figure 8. Start Threshold Voltage (V_{START}) vs. T_A

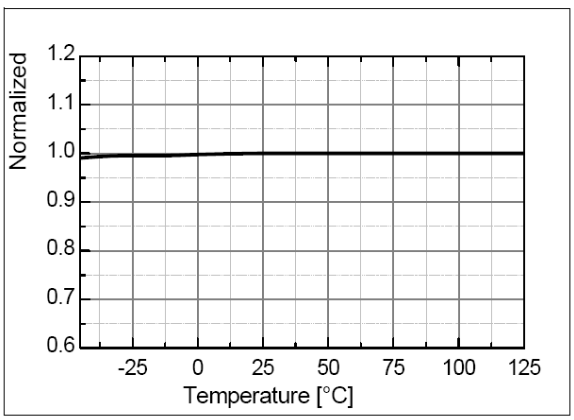

Figure 9. Stop Threshold Voltage (V_{STOP}) vs. T_A

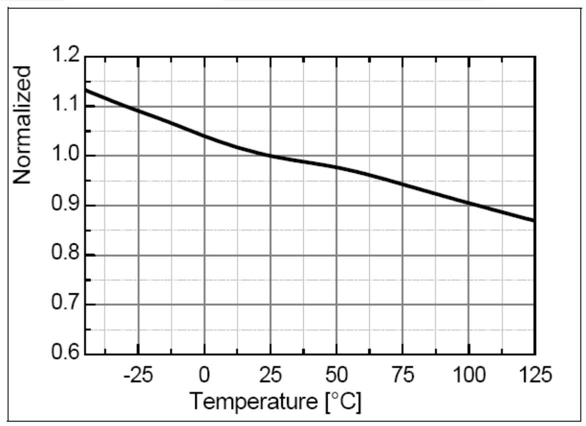

Figure 10. Startup Supply Current (I_{START}) vs. T_A

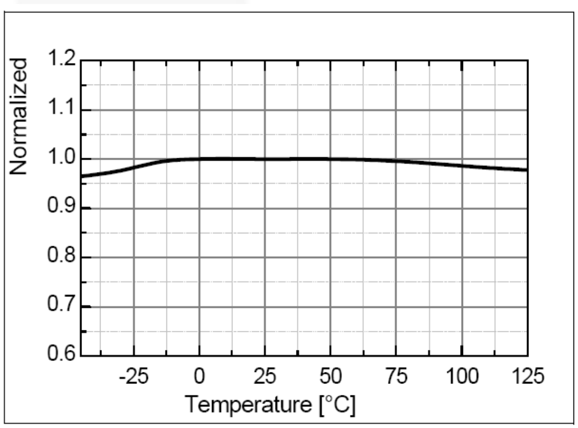

Figure 11. Operating Supply Current (I_{OP}) vs. T_A

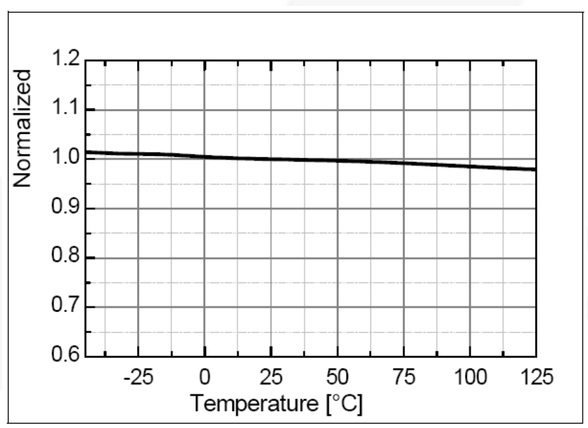

Figure 12. Output Upper Clamp Voltage (V_{EAH}) vs. T_A

Typical Performance Characteristics

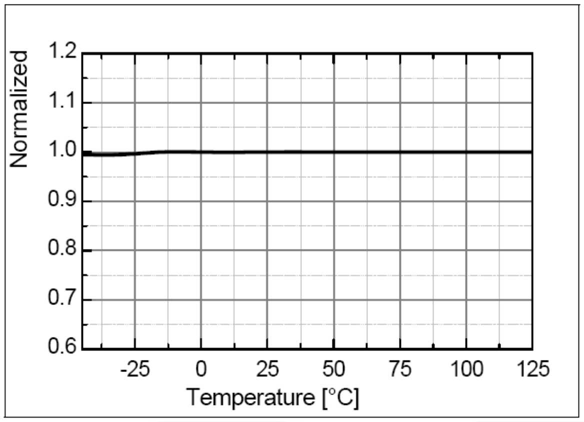

Figure 13. Zero Duty Cycle Output Voltage (V_{EAZ}) vs. T_A

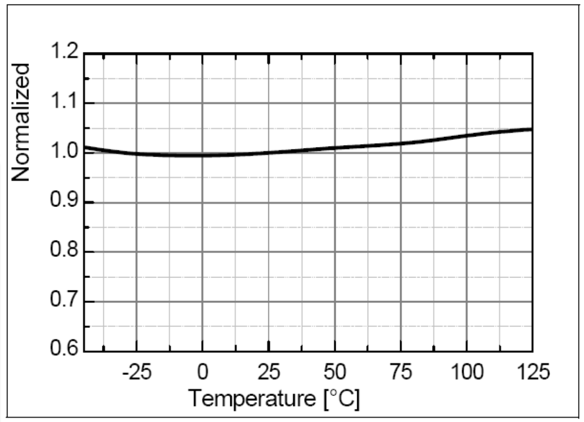

Figure 14. Maximum On-Time Program 1 ($t_{ON,MAX1}$) vs. T_A

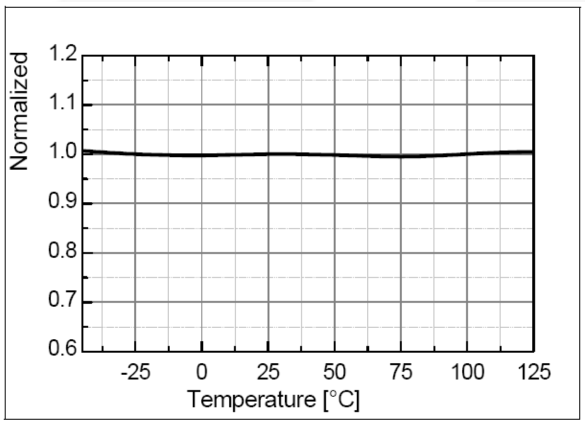

Figure 15. Maximum On-Time Program 2 ($t_{ON,MAX2}$) vs. T_A

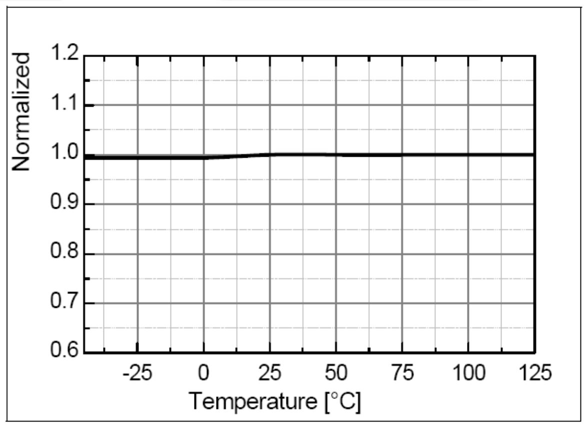

Figure 16. Current Sense Input Threshold Voltage Limit (V_{CS}) vs. T_A

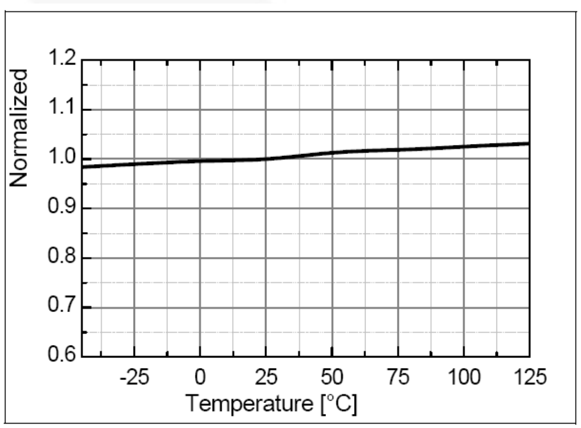

Figure 17. Input High Clamp Voltage (V_{CLAMPH}) vs. T_A

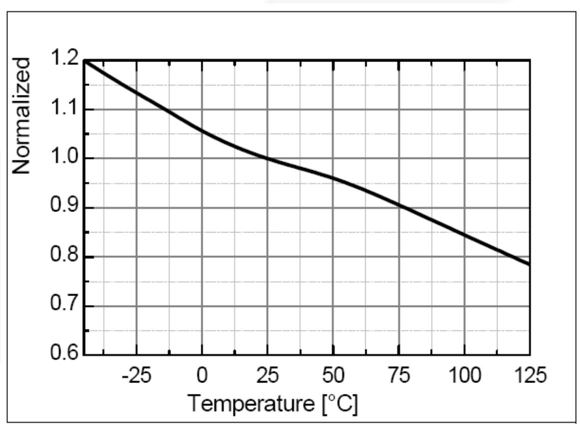

Figure 18. Input Low Clamp Voltage (V_{CLAMPL}) vs. T_A

Typical Performance Characteristics

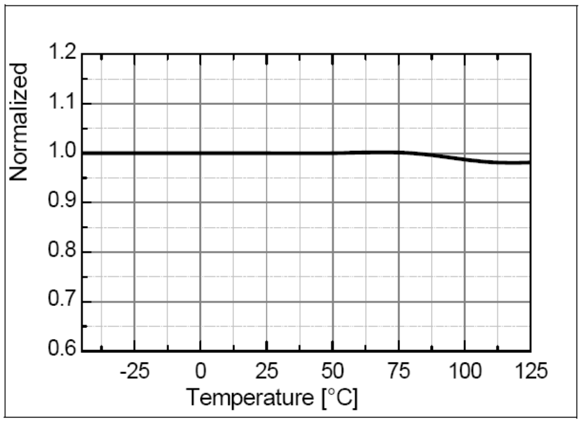

Figure 19. Output Voltage High (V_{OH}) vs. T_A

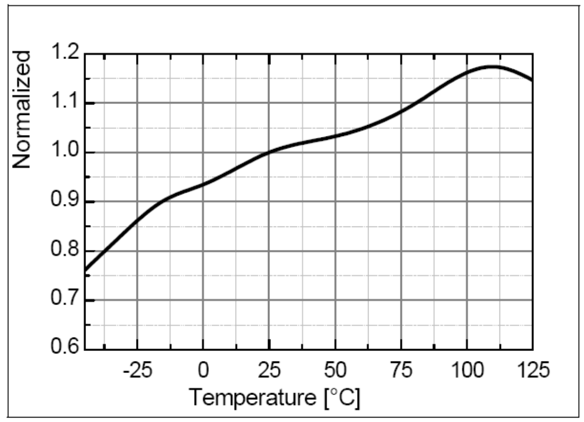

Figure 20. Output Voltage Low (V_{OL}) vs. T_A

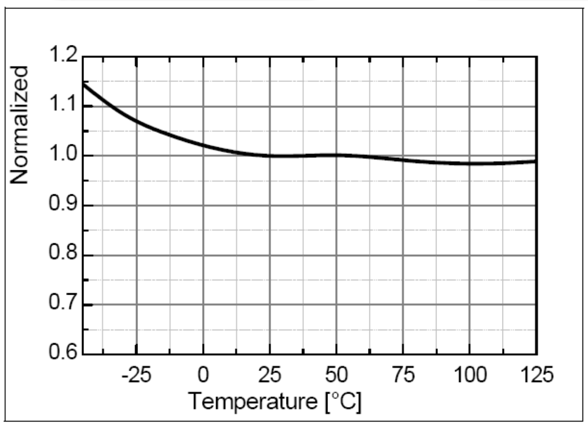

Figure 21. Restart Timer Delay (t_{RST}) vs. T_A

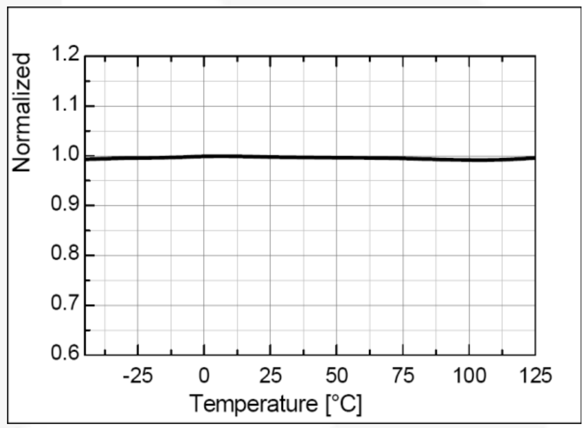

Figure 22. OVP Threshold at OVP Pin ($V_{OVP,OVP}$) vs. T_A

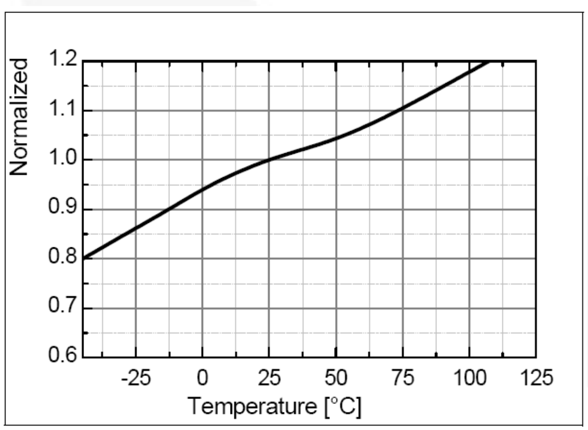

Figure 23. Output Saturation Voltage ($V_{RDY,SAT}$) vs. T_A

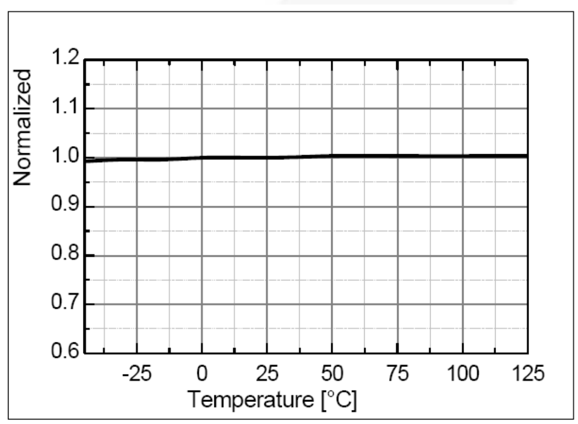

Figure 24. OVP Threshold Voltage (V_{OVP}) vs. T_A

Applications Information

1. Startup: Normally, supply voltage (V_{CC}) of a PFC block is fed from the additional power supply, which can be called standby power. Without this standby power, auxiliary winding for zero current detection can be used as a supply source. Once the supply voltage of the PFC block exceeds 12 V, internal operation is enabled until the voltage drops to 8.5 V. If V_{CC} exceeds V_Z, 20 mA current is sinking from V_{CC}.

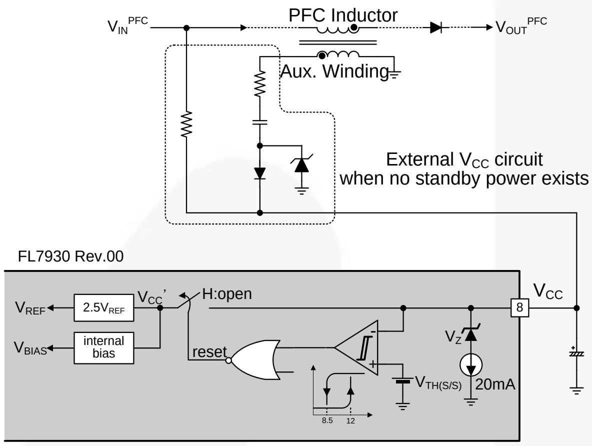

Figure 25. Startup Circuit

2. INV Block: Scaled-down voltage from the output is the input for the INV pin. Many functions are embedded based on the INV pin: transconductance amplifier, output OVP comparator, and disable comparator.

For the output voltage control, a transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage-controlled current source) aids the implementation of OVP and disable functions. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. To cancel down the line input voltage effect on power factor correction, effective control response of PFC block should be slower than the line frequency. This conflicts with the transient response of controller. Two-pole one-zero type compensation may be used to meet both requirements.

The OVP comparator shuts down the output drive block when the voltage of the INV pin is higher than 2.675 V with 0.175 V hysteresis. The disable comparator disables operation when the voltage of the inverting input is lower than 0.35 V with 100 mV hysteresis. An external small-signal MOSFET can be used to disable the IC. The IC operating current decreases to reduce power consumption if the IC is disabled. Figure 27 is the timing chart of the internal circuit near the INV pin when rated-PFC output voltage is assumed at 390 V_{DC} and V_{CC} supply voltage is 15 V.

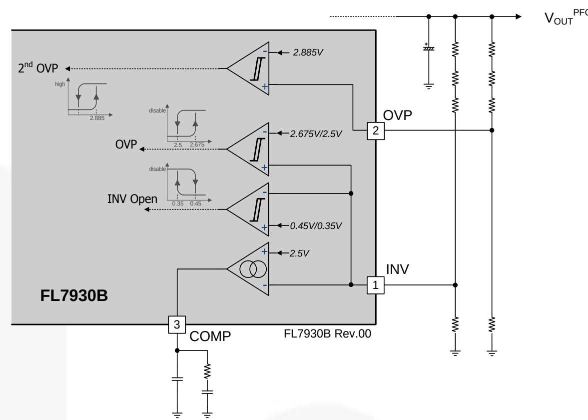

Figure 26. Circuit Around INV Pin

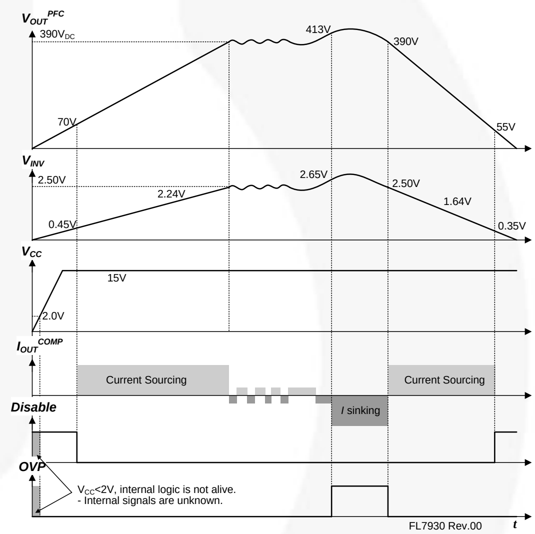

Figure 27. Timing Chart for INV Block

3. OVP Pin: Over-Voltage Protection (OVP) is embedded by the information at the INV pin. That information comes from the output through the voltage dividing resistors. To scale down from high voltage to low voltage, high resistance normally replaced with low resistance. If the resistor of high resistance is damaged and resistance is changed to high, INV pin information is normal, but output voltage exceeds its rated output. Once this occurs, output electrolytic capacitor may be damaged. The FL3930B provides an additional OVP pin that can be used to shut down the boost power stage when output voltage exceeds the OVP level if the resistors connected at the INV pin are damaged. To prevent such a catastrophe, an additional OVP pin is assigned to double check output voltage. The additional OVP may be called second OVP, while INV pin OVP can be called the first OVP. Since the two OVP conditions are quite different, the protection recovery modes are different.

Once the first OVP triggers, switching stops immediately and recovers switching when the output voltage is decreased with a hysteresis. When the second OVP triggers, switching can be recovered only when the V_{CC} supply voltage falls below V_{STOP} and builds up higher than V_{START} again and V_{OVP} is lower than hysteresis. If the second OVP is not used, the OVP pin must be connected to the INV pin or to ground.

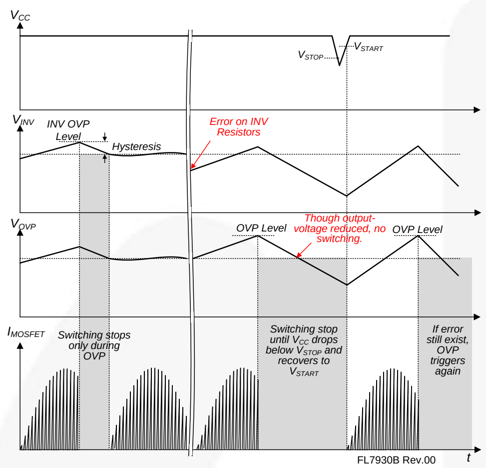

Figure 28. Comparison of First and Second OVP Recovery Modes

4. RDY Output: The FL7930C provides a PFC-ready pin that can be used to trigger other power stages when PFC output voltage reaches the proper level with hysteresis. When the INV voltage is higher than 2.24 V, RDY out is triggered HIGH and lasts until the INV voltage is lower than 2.051 V. When input AC voltage is quite high, for example 240 V_{AC}, PFC output voltage is always higher than RDY threshold, regardless of boost converter operation. In this case, the INV voltage is already higher than 2.24 V before PFC V_{CC} touches V_{START}. After boost converter operation stops, RDY is not pulled LOW because the INV voltage is higher than the RDY threshold. When V_{CC} of the PFC drops below 5 V, RDY is pulled LOW even through PFC output voltage is higher than threshold. The RDY pin output is open-drain, so needs an external pull-up resistor to supply the proper power source. The RDY pin output remains floating until V_{CC} is higher than 2 V.

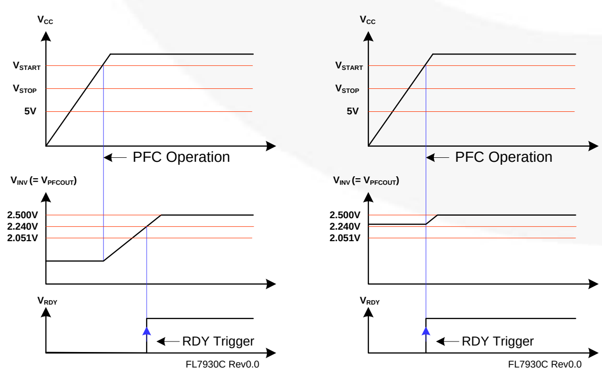

Figure 29. Two Cases of RDY Triggered HIGH

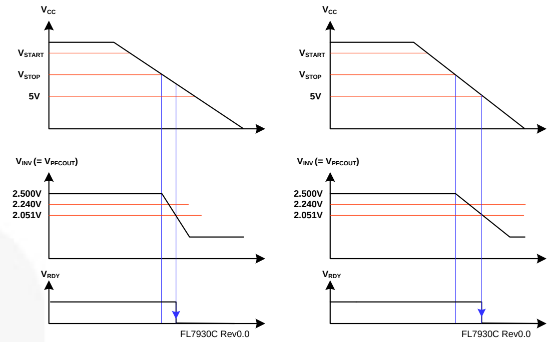

Figure 30. Two Cases of RDY Triggered LOW

5. Control Range Compensation: On time is controlled by the output voltage compensator. When input voltage is high and load is light, the control range becomes narrow compared to when input voltage is low. That control range decrease is anti-proportional to the double square of the input voltage. Thus, at high line, unwanted burst operation can occur at light load and audible noise may be generated from the boost inductor or inductor at input filter. Unlike other converters, burst operation in PFC block is not needed because the PFC block itself is normally disabled in Standby Mode. To reduce unwanted burst operation at light load, internal control range compensation is implemented and no burst operation occurs until 5% load at high line.

6. Zero-Current Detection: Zero-Current Detection (ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. When the power switch turns on, negative voltage is induced at the auxiliary winding due to the opposite winding direction *(see Equation (1))* and positive voltage is induced *(see Equation (2))* when the power switch turns off.

$$V_{AUX} = -\frac{T_{AUX}}{T_{IND}} \cdot V_{AC} \tag{1}$$

$$V_{AUX} = \frac{T_{AUX}}{T_{IND}} \cdot (V_{PFCOUT} - V_{AC}) \tag{2}$$

where V_{AUX} is the auxiliary winding voltage; T_{IND} and T_{AUX} are boost inductor turns and auxiliary winding turns, respectively; V_{AC} is input voltage for PFC converter; and V_{OUT_PFC} is output voltage from the PFC converter.

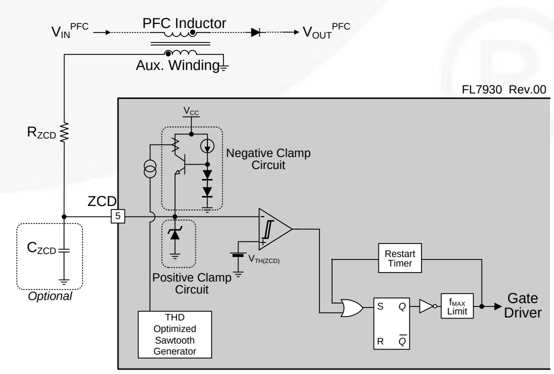

Figure 31. Circuit Near ZCD

Because auxiliary winding voltage can swing from negative voltage to positive voltage, the internal block in the ZCD pin has both positive and negative voltage clamping circuits. When the auxiliary voltage is negative, an internal circuit clamps the negative voltage at the ZCD pin around 0.65 V by sourcing current to the serial resistor between the ZCD pin and the auxiliary winding. When the auxiliary voltage is higher than 6.5 V, the FL7390 sinks current through a resistor from the auxiliary winding to the ZCD pin.

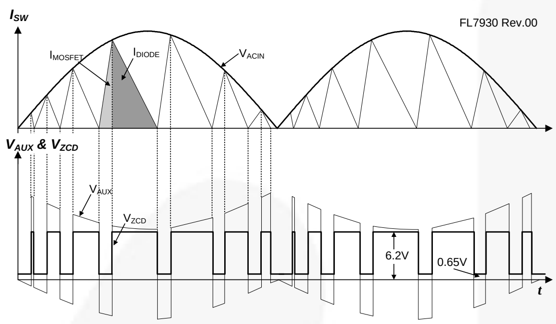

Figure 32. Auxiliary Voltage Depends on MOSFET Switching

To check the boost inductor current zero instance, auxiliary winding voltage is used. When boost inductor current becomes zero, there is a resonance between boost inductor and all capacitors at MOSFET drain pin, including C_{OSS} of the MOSFET; an external capacitor at the D-S pin to reduce the voltage rising and falling slope of the MOSFET; a parasitic capacitor at inductor; and so on to improve performance. Resonated voltage is reflected to the auxiliary winding and can be used for detecting zero current of boost inductor and valley position of MOSFET voltage stress. For valley detection, a minor delay by the resistor and capacitor is needed. A capacitor increases the noise immunity at the ZCD pin. If ZCD voltage is higher than 1.5 V, an internal ZCD comparator output becomes HIGH and LOW when the ZCD goes below 1.4 V. At the falling edge of comparator output, internal logic turns on the MOSFET.

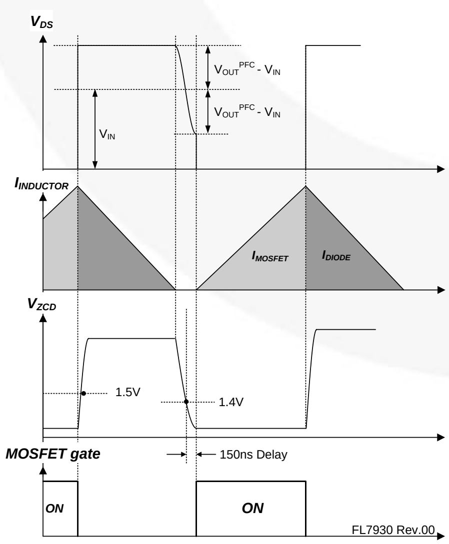

Figure 33. Auxiliary Voltage Threshold

When no ZCD signal is available, the PFC controller cannot turn on the MOSFET, so the controller checks every switching off time and forces MOSFET turn on when the off time is longer than 150 µs. This is called restart timer. The restart timer triggers MOSFET turn-on at startup and may be used at the input voltage-zero cross period.

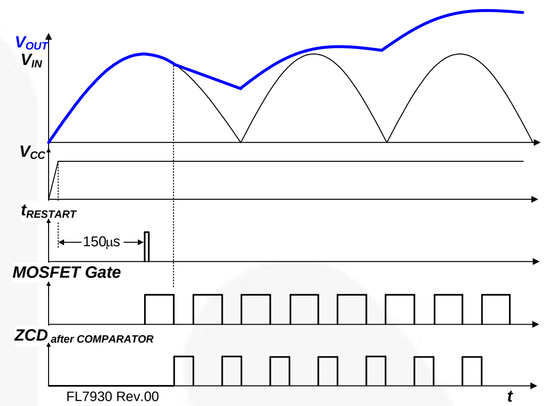

Figure 34. Restart Timer at Startup

Because the MOSFET turn on depends on the ZCD input, switching frequency may increase to higher than several megahertz due to mis-triggering or noise on the nearby ZCD pin. If the switching frequency is higher than needed for critical conduction mode (CRM), operation mode shifts to continuous conduction mode (CCM). In CCM, unlike CRM where the boost inductor current is reset to zero at the next switch on; inductor current builds up at every switching cycle and can be raised to high current that exceeds the current rating of the power switch or diode. This can seriously damage the power switch and result in burn down. To avoid this, maximum switching frequency limitation is embedded. If ZCD signal is applied again within 3.3 µs after the previous rising edge of the gate signal, this signal is ignored internally and FL7930 waits for another ZCD signal. This slightly degrades the power factor performance at light load and high input voltage.

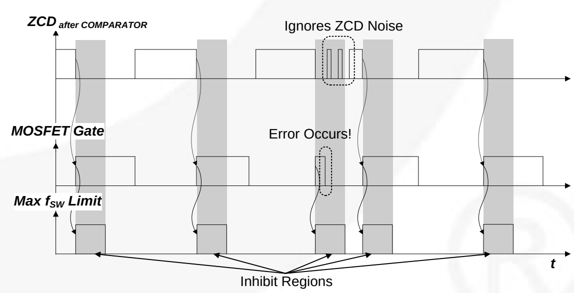

Figure 35. Maximum Switching Frequency Limit Operation

7. Control: The scaled output is compared with the internal reference voltage and sinking or sourcing current is generated from the COMP pin by the transconductance amplifier. The error amplifier output is compared with the internal sawtooth waveform to give proper turn-on time based on the controller.

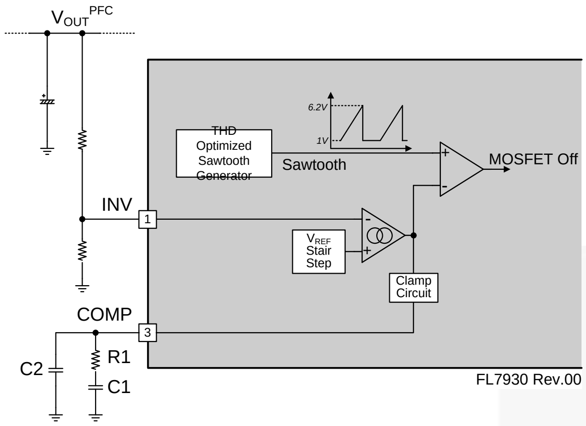

Figure 36. Control Circuit

Unlike a conventional voltage-mode PWM controller, FL7930 turns on the MOSFET at the falling edge of ZCD signal. On instance is decided by the external signal and the turn-on time lasts until the error amplifier output (V_{COMP}) and sawtooth waveform meet. When load is heavy, output voltage decreases, scaled output decreases, COMP voltage increases to compensate low output, turn-on time lengthens to give more inductor turn-on time, and increased inductor current raises the output voltage. This is how PFC negative feedback controller regulates output.

The maximum of V_{COMP} is limited to 6.5 V, which dictates the maximum turn-on time, and switching stops when V_{COMP} is lower than 1.0 V.

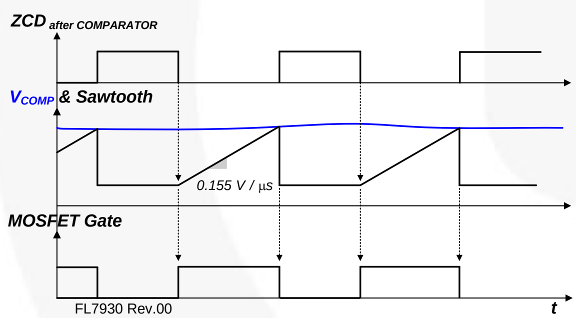

Figure 37. Turn-On Time Determination

The roles of PFC controller are regulating output voltage and input current shaping to increase power factor. Duty control based on the output voltage should be fast enough to compensate output voltage dip or overshoot. For the power factor, however, the control loop must not react to the fluctuating AC input voltage. These two requirements conflict; therefore, when designing a feedback loop, the feedback loop should be least ten times slower than AC line frequency. That slow response is made by C1 at compensator. R1 makes gain boost around operation region and C2 attenuates gain at higher frequency. Boost gain by R1 helps raise the response time and improves phase margin.

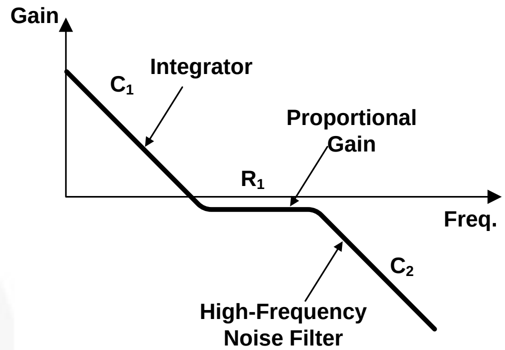

Figure 38. Compensators Gain Curve

For the transconductance error amplifier side, gain changes based on differential input. When the error is large, gain is large to force the output dip or peak to suppress quickly. When the error is small, low gain is used to improve power factor performance.

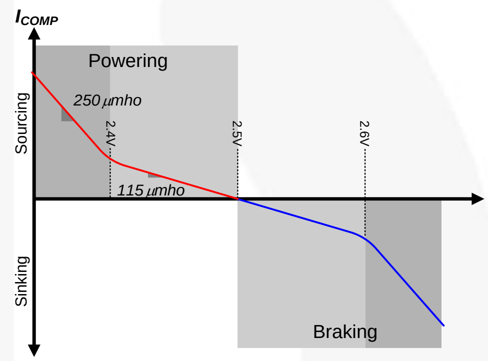

Figure 39. Gain Characteristic

8. Soft-Start: When V_{CC} reaches V_{START}, an internal reference voltage is increased like a stair step for 5 ms. As a result, V_{COMP} is also raised gradually and MOSFET turn-on time increases smoothly. This reduces voltage and current stress on the power switch during startup.

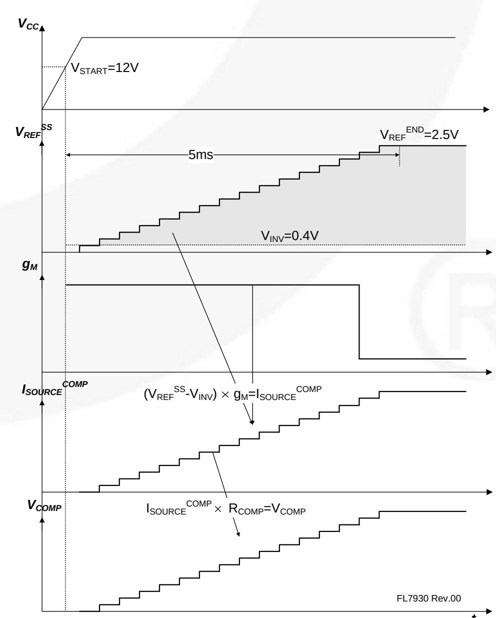

Figure 40. Soft-Start Sequence

9. Startup without Overshoot: Feedback control speed of PFC is quite slow. Due to the slow response, there is a gap between output voltage and feedback control. That is why over-voltage protection (OVP) is critical at the PFC controller and voltage dip caused by fast load changes from light to heavy is diminished by a bulk capacitor. OVP is easily triggered during startup phase. Operation on and off by OVP at startup may cause audible noise and can increase voltage stress at startup, which is normally higher than in normal operation. This operation is better when soft-start time is very long; however, too much startup time enlarges the output voltage building time at light load. FL7930 has less overshoot prevention at startup. During startup, the feedback loop is controlled by an internal proportional gain controller. When the output voltage reaches the rated value, it switches to an external compensator after a transition time of 30 ms. In short, an internal proportional gain controller eliminates overshoot at startup and an external conventional compensator takes over successfully afterward.

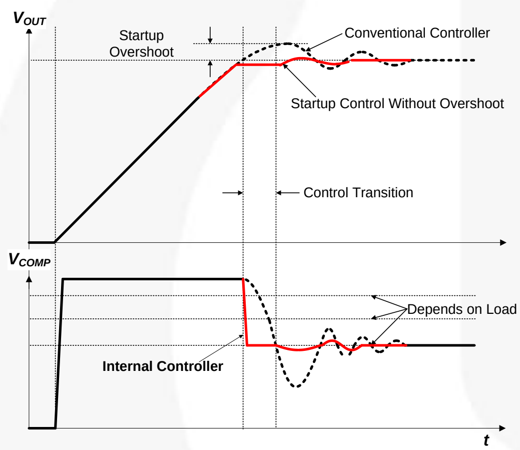

Figure 41. Startup with Overshoot Prevention

10. THD Optimization: Total Harmonic Distortion (THD) is the factor that dictates how closely the input current shape matches sinusoidal form. The turn-on time of the PFC controller is almost constant over one AC line period due to the extremely low feedback control response. The turn-off time is determined by the current decrease slope of the boost inductor made by the input voltage and output voltage. Once inductor current becomes zero, resonance between C_{OSS} and the boost inductor makes oscillating waveforms at the drain pin and auxiliary winding. By checking the auxiliary winding voltage through the ZCD pin, the controller can check the zero current of the boost inductor. At the same time, a minor delay is inserted to determine the valley position of drain voltage. The input and output voltage difference is at its maximum at the zero-cross point of the AC input voltage. The current decrease slope is steep near the zero-cross region and more negative inductor current flows during a drain voltage valley-detection time. Such a negative inductor current cancels down the positive current flows and input current becomes zero, called "zero-cross distortion" in PFC.

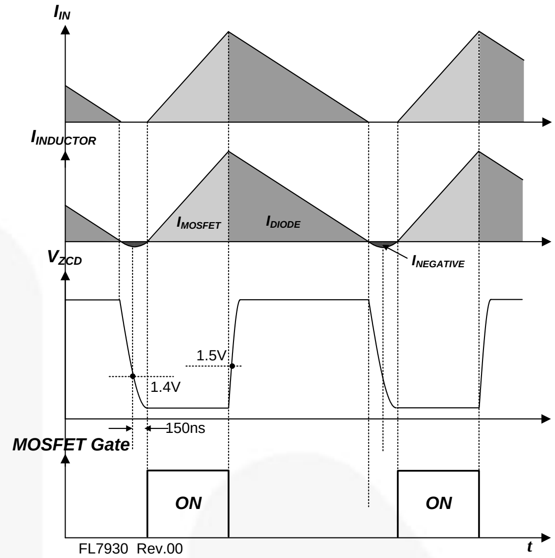

Figure 42. Input and Output Current Near Input Voltage Peak

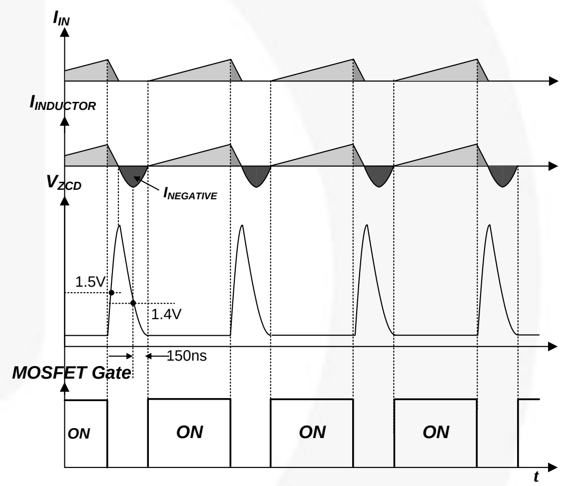

Figure 43. Input and Output Current Near Input Voltage Peak Zero Cross

To improve this, lengthened turn-on time near the zero-cross region is a well-known technique, though the method may be different from company to company and may be proprietary. FL7930 accomplishes this by sourcing current through the ZCD pin. Auxiliary winding voltage becomes negative when the MOSFET turns on and is proportional to input voltage. The negative clamping circuit of ZCD outputs the current to maintain the ZCD voltage at a fixed value. The sourcing current from the ZCD is directly proportional to the input voltage. Some portion of this current is applied to the internal sawtooth generator, together with a fixed-current source. Theoretically, the fixed-current source and the capacitor at sawtooth generator decide the maximum turn-on time when no current is sourcing at ZCD clamp circuit and available turn-on time gets shorter proportional to the ZCD sourcing current.

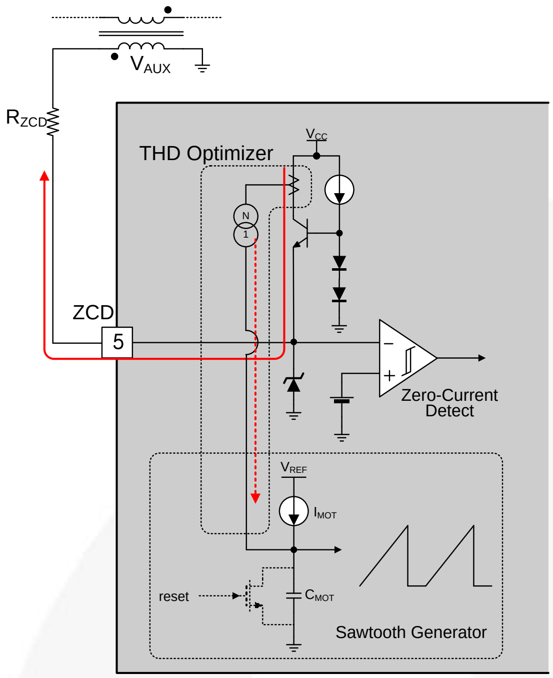

Figure 44. Circuit of THD Optimizer

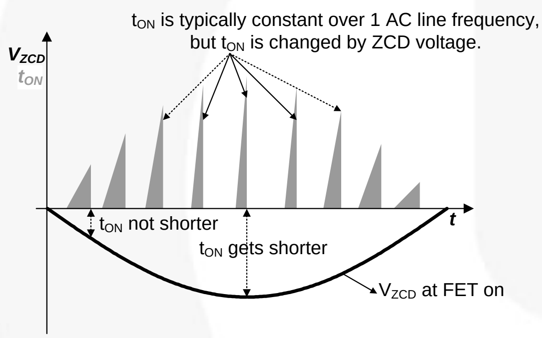

Figure 45. Effect of THD Optimizer

By THD optimizer, turn-on time over one AC line period is proportionally changed, depending on input voltage. Near the zero cross, lengthened turn-on time improves THD performance.

11. Input Voltage Absent Detection: To save power loss caused by input voltage-sensing resistors and to optimize THD, FL7930 omits AC input voltage detection. Therefore, no information about AC input is available from the internal controller. In many cases, the V_{CC} of PFC controller is supplied by an independent power source, like standby power. In this scheme, some mismatch may exist. For example, when the electric power is suddenly interrupted during two or three AC line periods; V_{CC} is still alive during that time, but output voltage drops because there is no input power source. Consequently, the control loop tries to compensate for the output voltage drop and V_{COMP} reaches its maximum. This lasts until AC input voltage is live again. When AC input voltage is live again, high V_{COMP} allows high switching current and more stress is put on the MOSFET and diode. To protect against this, FL7930 internally checks if the input AC voltage exists. If input does not exist, soft-start is reset and waits until AC input is live again. Soft-start manages the turn-on time for smooth operation when it detects AC input is applied, which applies less voltage and current stress on startup.

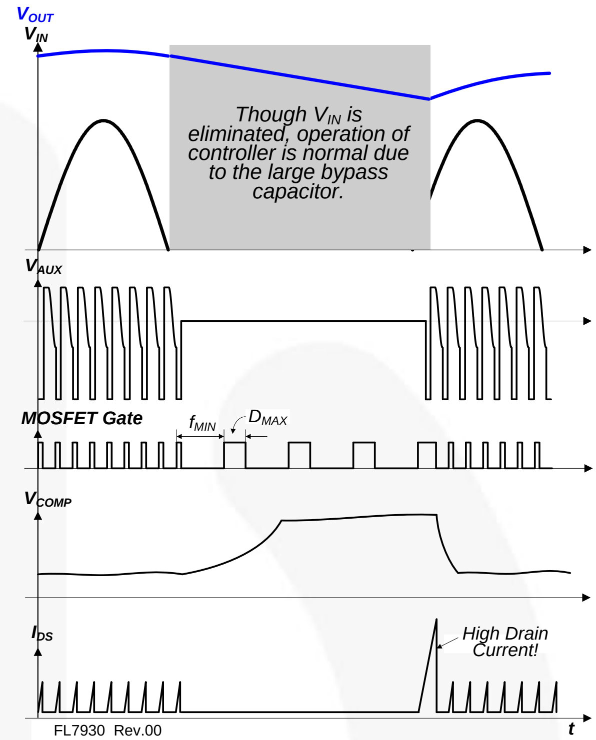

Figure 46. Operation without Input Voltage Absent Circuit

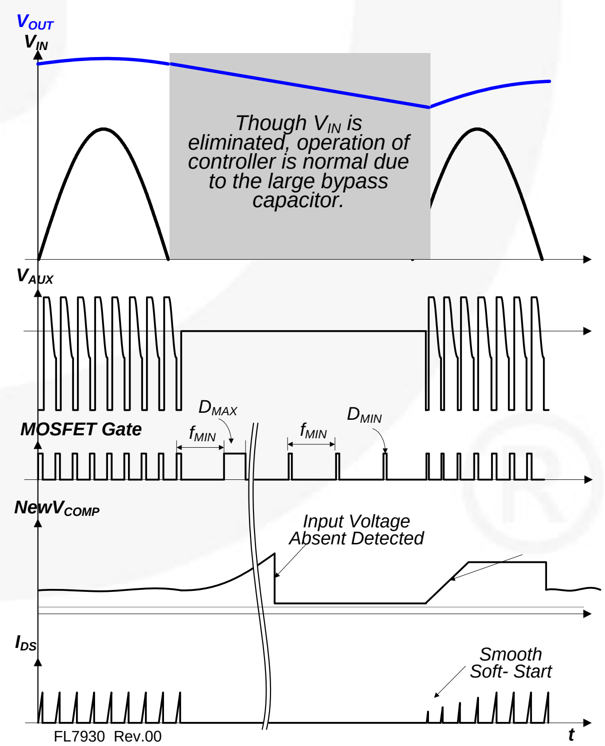

Figure 47. Operation with Input Voltage Absent Circuit

12. Current Sense: The MOSFET current is sensed using an external sensing resistor for the over-current protection. If the CS pin voltage is higher than 0.8 V, the over-current protection comparator generates a protection signal. An internal RC filter of 40 kΩ and 8 pF is included to filter switching noise.

13. Gate Driver Output: FL7930 contains a single totem-pole output stage designed for a direct drive of the power MOSFET. The drive output is capable of up to +500/-800 mA peak current with a typical rise and fall time of 50 ns with 1 nF load. The output voltage is clamped to 13 V to protect the MOSFET gate even if the V_{CC} voltage is higher than 13 V.

14. PCB Layout

PFC block normally handles high switching current and the voltage low-energy signal path can be affected by the high-energy path. Cautious PCB layout is mandatory for stable operation.

- The gate drive path should be as short as possible. The closed-loop that starts from the gate driver, MOSFET gate, and MOSFET source to ground of PFC controller is recommended as close as possible. This is also the crossing point between power ground and signal ground. Power ground path from the bridge diode to the output bulk capacitor should be short and wide. The sharing position between power ground and signal ground should be only at one position to avoid ground loop noise. Signal path of PFC controller should be short and wide for external components to contact.
- PFC output voltage sensing resistor is normally high to reduce current consumption. This path can be affected by external noise. To reduce noise possibility at the INV pin, a shorter path for output sensing is recommended. If a shorter path is not possible, place some dividing resistors between PFC output and the INV pin — closer to the INV pin is better. Relative high voltage close to the INV pin can be helpful.
- ZCD path is recommended close to auxiliary winding from boost inductor and to the ZCD pin. If that is difficult, place a small capacitor (below 50 pF) to reduce noise.
- Switching current-sense path should not share with any other path to avoid interference. Some additional components may be needed to reduce the noise level applied to the CS pin.
- A stabilizing capacitor for V_{CC} is recommended as close as possible to the V_{CC} and ground pins. If it is difficult, place the SMD capacitor as close to the corresponding pins as possible.

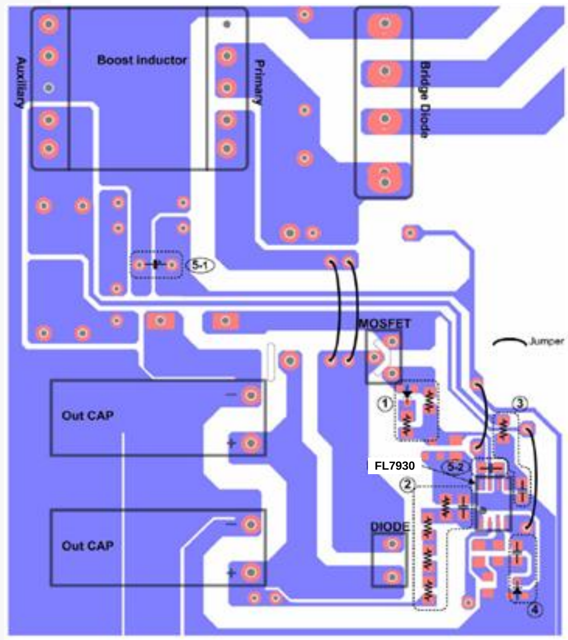

Figure 48. Recommended PCB Layout

Physical Dimensions

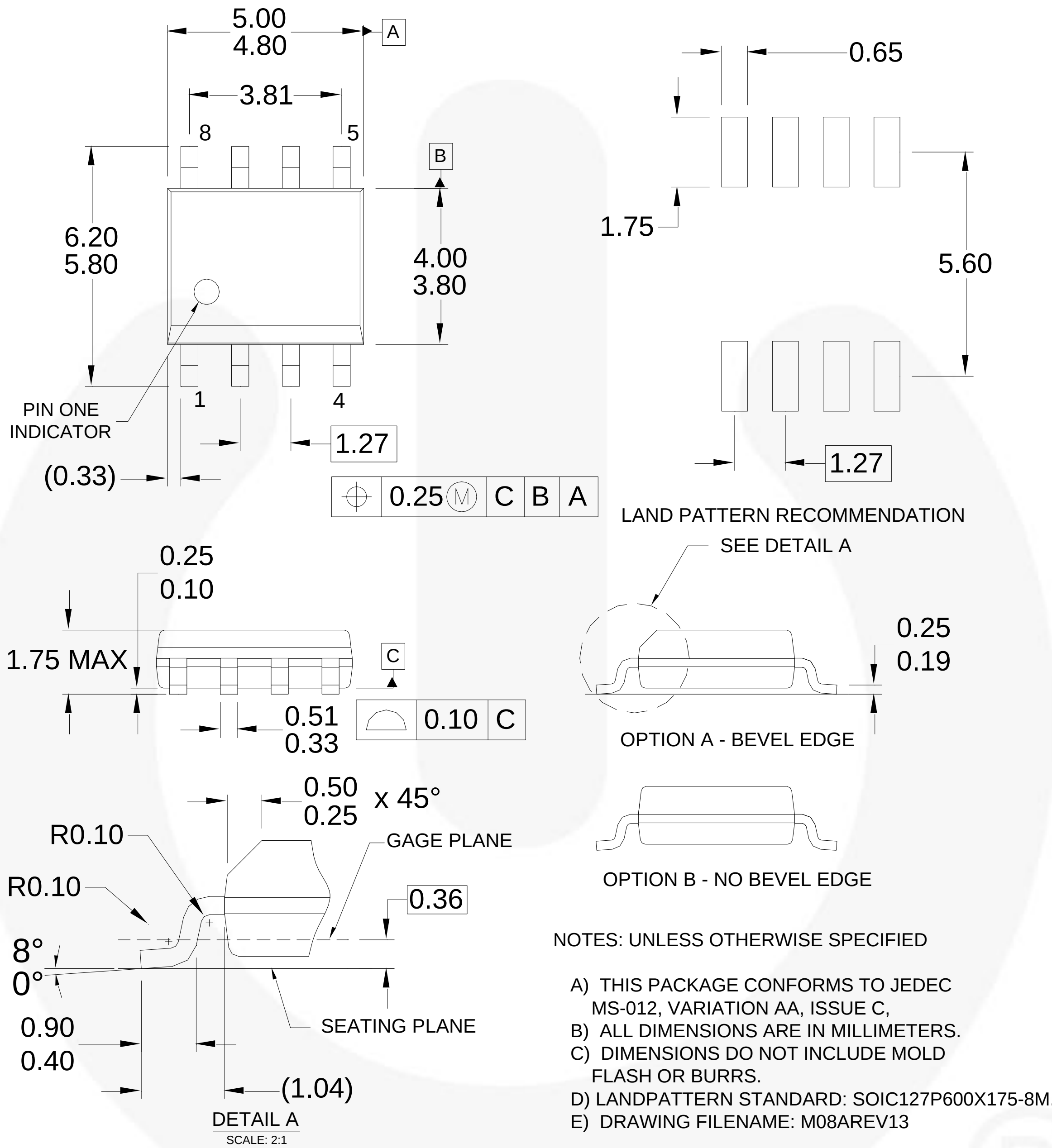

Figure 49. 8-Lead Small Outline Package (SOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
SerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64