

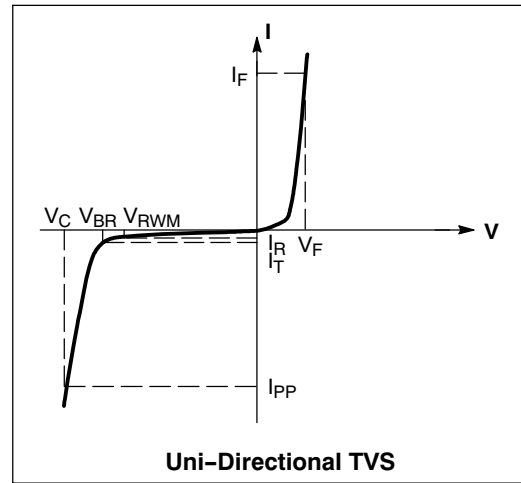
ESD5Z2.5T1 SERIES

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
I _F	Forward Current
V _F	Forward Voltage @ I _F
P _{pk}	Peak Power Dissipation
C	Max. Capacitance @V _R = 0 and f = 1 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.1 V Max. @ I_F = 10 mA for all types)

Device**	Device Marking	V _{RWM} (V)	I _R (μA) @ V _{RWM}	V _{BR} (V) @ I _T (Note 2)	I _T	V _C (V) @ I _{pp} = 5.0 A†	V _C (V) @ Max I _{pp} †	I _{pp} (A)†	P _{pk} (W)†	C (pF)	V _C
		Max	Max	Min	mA	Typ	Max	Max	Max	Typ	Per IEC61000-4-2 (Note 3)
ESD5Z2.5T1, G*	ZD	2.5	6.0	4.0	1.0	6.5	10.9	11.0	120	145	Figures 1 and 2 See Below (Note 4)
ESD5Z3.3T1, G*	ZE	3.3	0.05	5.0	1.0	8.4	14.1	11.2	158	105	
ESD5Z5.0T1, G*	ZF	5.0	0.05	6.2	1.0	11.6	18.6	9.4	174	80	
ESD5Z6.0T1, G*	ZG	6.0	0.01	6.8	1.0	12.4	20.5	8.8	181	70	
ESD5Z7.0T1, G*	ZH	7.0	0.01	7.5	1.0	13.5	22.7	8.8	200	65	
ESD5Z12T1, G*	ZM	12	0.01	14.1	1.0	17	25	9.6	240	55	

*The "G" suffix indicates Pb-Free package available.

**Other voltages available upon request.

†Surge current waveform per Figure 5.

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.

3. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

4. ESD5Z5.0T1G shown below. Other voltages available upon request.

Tek Run: 1.25GS/s Sample 1102

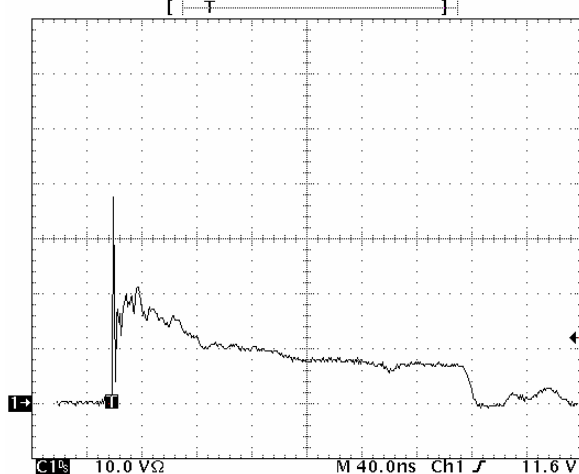


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000-4-2

Tek Run: 1.25GS/s Sample 1102

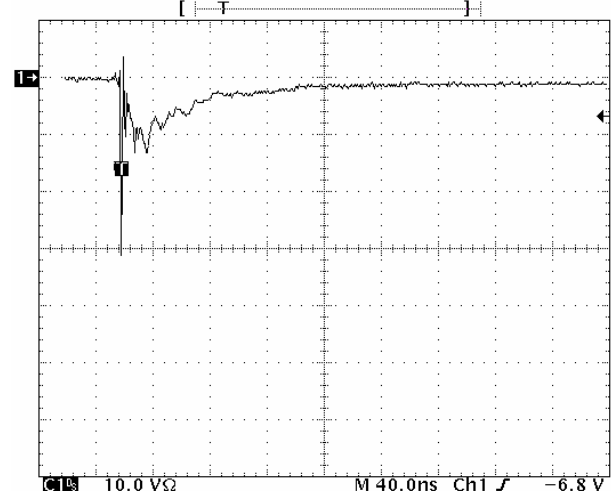


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000-4-2

ESD5Z2.5T1 SERIES

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

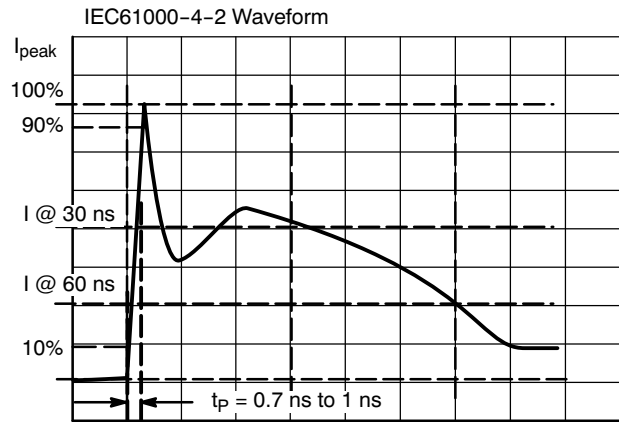


Figure 3. IEC61000-4-2 Spec

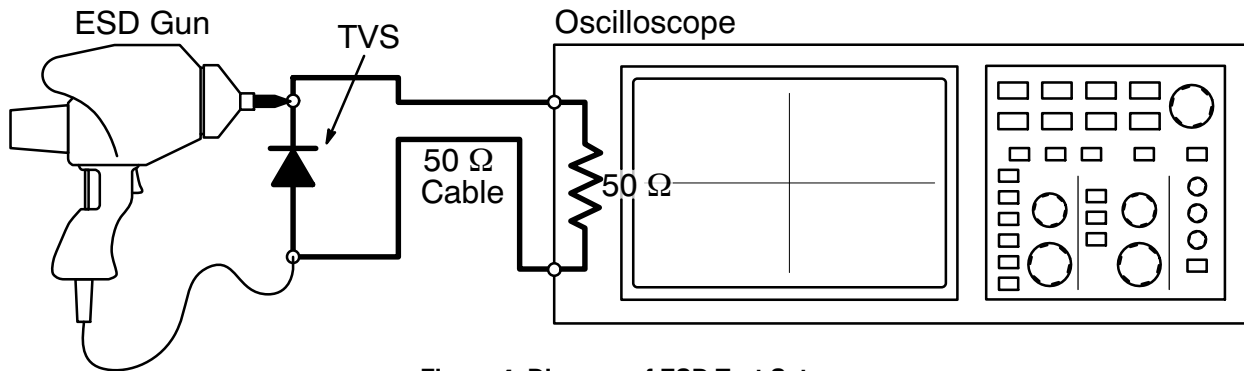


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

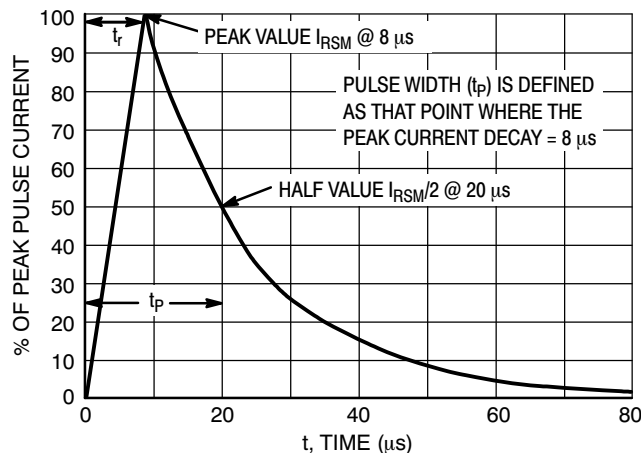
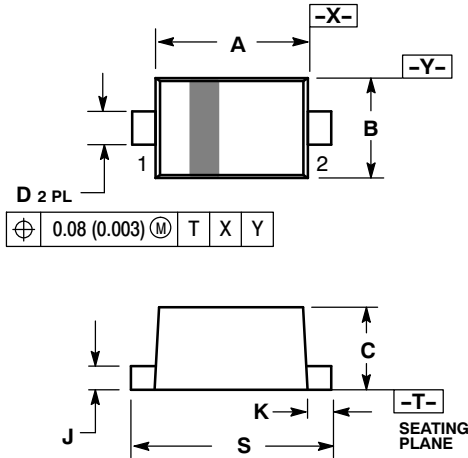


Figure 5. 8 X 20 μ s Pulse Waveform

ESD5Z2.5T1 SERIES

PACKAGE DIMENSIONS

SOD-523
CASE 502-01
ISSUE C

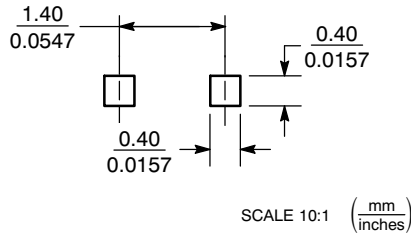


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.20	1.30	0.043	0.047	0.051
B	0.70	0.80	0.90	0.028	0.032	0.035
C	0.50	0.60	0.70	0.020	0.024	0.028
D	0.25	0.30	0.35	0.010	0.012	0.014
J	0.07	0.14	0.20	0.0028	0.0055	0.0079
K	0.15	0.20	0.25	0.006	0.008	0.010
S	1.50	1.60	1.70	0.059	0.063	0.067

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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